ALIGNMENT DETAILS

A. Idle current.
It is best to reset the idle current when any component is changed in one of the power amplifiers. It is ESSENTIAL to reset the idle current if any of the output or driver or other critical transistors is replaced. When devices have been replaced, always set the idle current to minimum (VR301 fully counter-clockwise on the channel(s) affected) before switching the amplifier on.

A.1 Switch on and allow 5 minutes for the amplifier to warm up. No signal source or load should be connected.

A.2 On the left hand amplifier: Connect a digital voltmeter switched to its 200mV range across R393, 0.1Ω (clip on to the resistor's leads). TAKE GREAT CARE - high voltages are present.

A.3 Adjust the multi-turn trimmer VR301 to give a reading between 11mV and 13mV.

A.4 Repeat A.2 and A.3 for the right hand amplifier.

B. Common Mode Rejection Ratio (CMRR).
Only make this adjustment if you have reason to believe that the CMRR is below specification, or if you have replaced components in the input amplifier.

B.1 Switch to STEREO mode and BALANCED input. No load resistors are necessary.

B.2 Connect a sine-wave generator to the left XLR input, with the "+" and "-" pins connected together. Set the generator amplitude to about 1 volt RMS and the frequency to 1kHz. Connect an AC voltmeter or oscilloscope to the left channel output terminals.

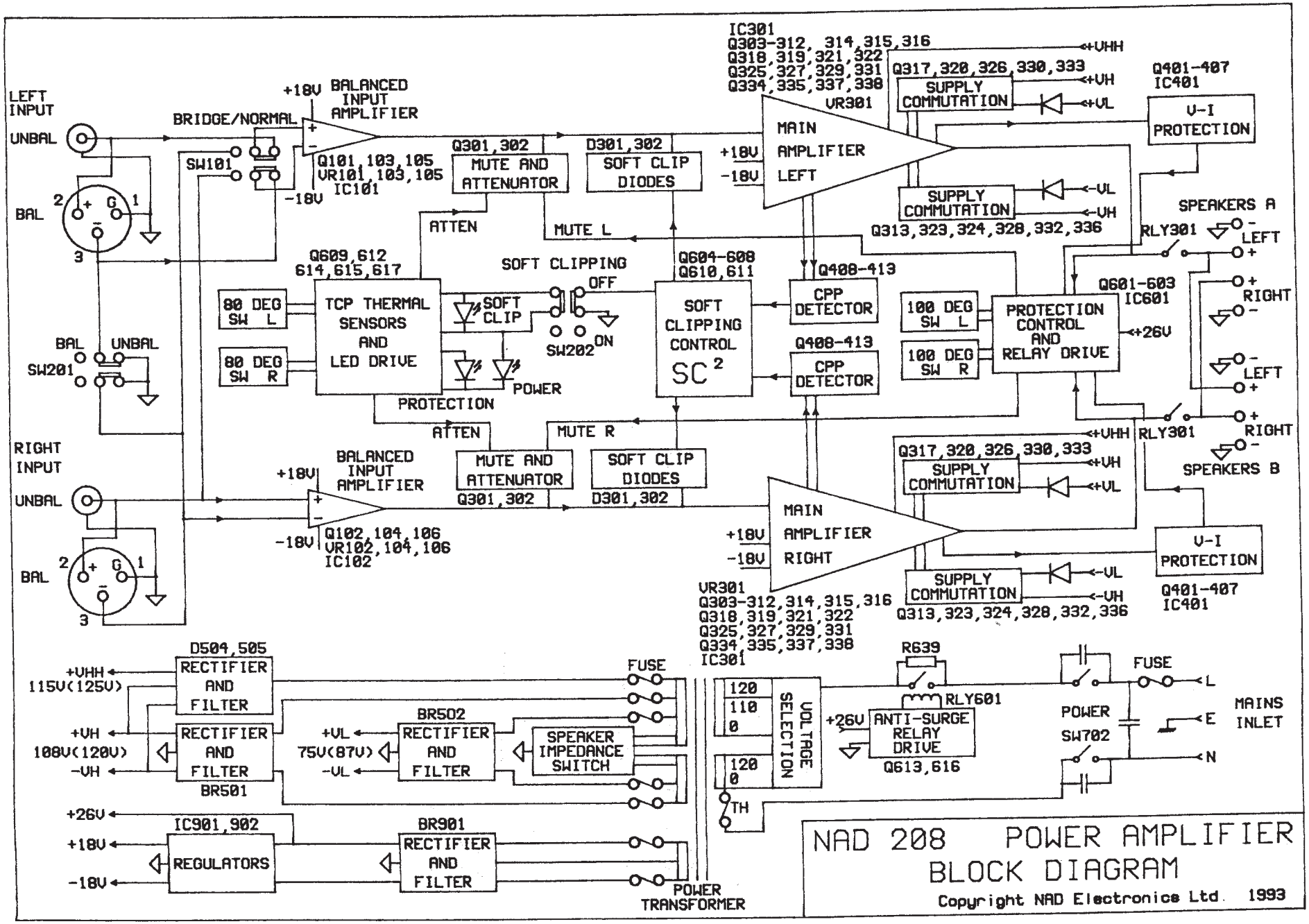
B.3 Adjust trimmer VR105 for minimum output.

B.4 Change the generator frequency to 50Hz and adjust VR101 for minimum output.

B.5 Change the generator frequency to 20kHz and adjust VR103 for minimum output.

B.6 Change the generator frequency to 1kHz and repeat B.3, B.4 and B.5 until no further reduction can be achieved.

B.7 Repeat B.2 through to B.6 for the right channel. The trimmers are VR106, VR102 and VR104 for 1kHz, 50Hz and 20kHz respectively.



NAD 208 POWER AMPLIFIER BLOCK DIAGRAM

CIRCUIT DESCRIPTION

The NAD 208 is a 250 watt power amplifier which uses EDP techniques to achieve an IHF dynamic power output of 600 watts into 8Ω. It has electronically balanced inputs and comprehensive protection systems to guard against abuse while remaining transparent to music signals.

The following circuit description should be read with reference to the accompanying block diagram and schematics.

For the input PCB circuitry only the left hand channel component references will be mentioned (odd numbers). The balanced input signals are fed via coupling capacitors C103, C107 to the differential input stage Q101, Q105. Their collectors drive the output op-amp IC101B, and are supplied from the constant current source Q103. The servo amplifier IC101A controls the DC levels around the input stage using common mode feedback. Overall differential feedback is provided by the network R133, R129, R117, R111, R121 and VR105, which fixes the input stage gain at exactly 2.0. The Common Mode Rejection Ratio (CMRR) is trimmed by three preset resistors. VR105 sets the mid-band CMRR (around 1kHz), VR101 the low frequency CMRR (50-60Hz) and VR103 the high frequency CMRR (20kHz). Clipping diodes D101, D103 protect against excessive common mode input signals.

The inputs can be unbalanced with SW201, which grounds the inverting inputs to minimize noise. In bridge mode SW101 disconnects the left channel input amplifier and re-connects it, in reverse phase, to the right channel input connectors. Thus in bridge mode the input impedance is halved, but the voltage gain is doubled.

R206 and C206 provide a low impedance return from signal ground to the amplifier chassis. The chassis is taken to mains earth via the third wire of the three-core power cord.

The left and right signals are taken from the input PCB via two screened cables, to each of the main power amplifier PCBs. These two PCBs are *identical* and so have the same component reference numbering.

The input resistors R303 and R307 act with C305 to provide RF filtering. R303 also contributes a suitable source impedance against which the soft clip diodes D301 and D302, the input mute transistor Q301 and input attenuator Q302 and R304, can work. The signal splits through C306, C307 to feed the input transistors Q304, Q305 which form a complementary current- mode feedback pair. The output signals from their collectors pass via the cascode transistors Q303, Q306 to the twin current mirrors R319, D306, Q308, R334 and R322, D307, Q311, R335, R336 which form the push-pull class A gain stage.

A temperature-compensated DC bias voltage for the output stage is produced by the network Q309, Q310, D308, R330-R333, VR301. Q309 is thermally coupled to the pre-drivers Q314, Q316 and the distortion correction transistor Q315 to compensate for their temperature drift. Q310 is mounted on the main heatsink to compensate for Vgs drift in the output MOSFETs.

The positive pre-driver Q314 feeds via R340 and D313 to the positive push-pull drivers Q321, Q322. These in turn drive the four paralleled main positive output MOSFETs Q327, Q331, Q335, Q338. Resistors R370, R378, R386, R394 force the output current to be shared equally between the output MOSFETs (**). D317 clamps the MOSFET gate drive to limit the positive peak current output to a safe level.

** Although current sharing resistors are used, each set of paralleled MOSFETs (output and EDP) must be matched very closely in order to achieve accurate current sharing. It is therefore MOST IMPORTANT that only matched sets of spare parts supplied by NAD are used for replacing these MOSFETs. If a single MOSFET fails, then the whole parallel set of three or four MUST be replaced.