±18V OPERATION HIGH QUALITY AUDIO VOLUME

■FEATURES

- Operating Voltage — Analog ±10 to ±18V, Digital +3.0 to +5.5V
- 3-Wired Serial Control
- Selectable Chip Address
  Available for using four chips on same serial bus line
- Low Output Noise
  * It conforms to the characteristics of an external operational amplifier.
- Low Distortion
  * It conforms to the characteristics of an external operational amplifier.
- Volume — 0 to -111.75dB /0.25dB step, +21 to 0dB /3dB step, Mute
- Soft-Step Circuit
- Zero Cross Detection Circuit
- Package Outline — SSOP32

■GENERAL DESCRIPTION

The MUSES72323 is a ±18V operation high quality audio volume. It provides low output noise and low distortion characteristics, 0.25dB step volume. In addition, employing external op-amps as output signal buffers, it offers designer's variety of circuit design.

All of functions are controlled via three-wired serial bus. Selectable chip address is available for using two chips on same serial bus line.

The MUSES72323 is suitable for High-end audio equipment and professional audio equipment.

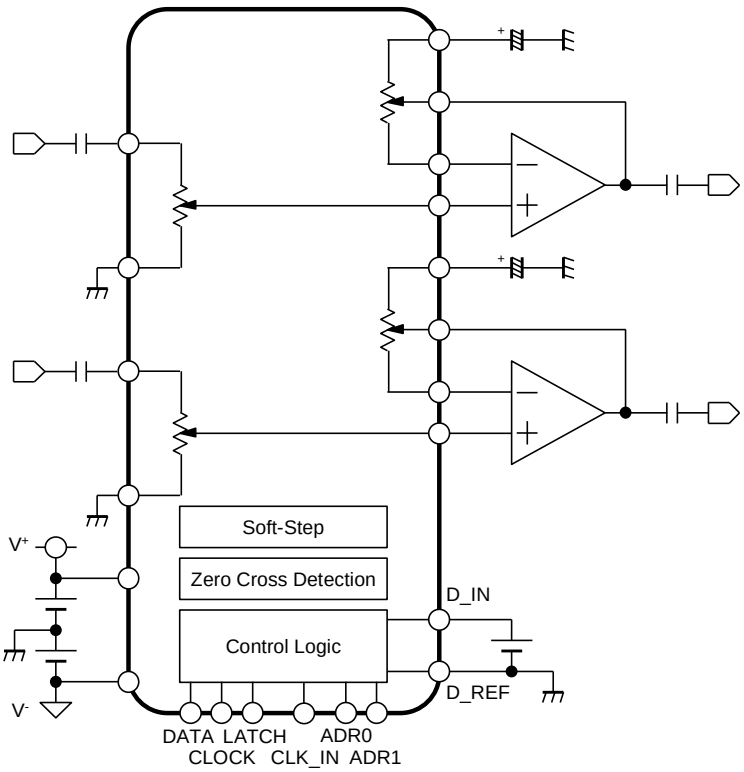
■APPLICATION

- Hi-Fi Audio Application
- Professional Audio Application

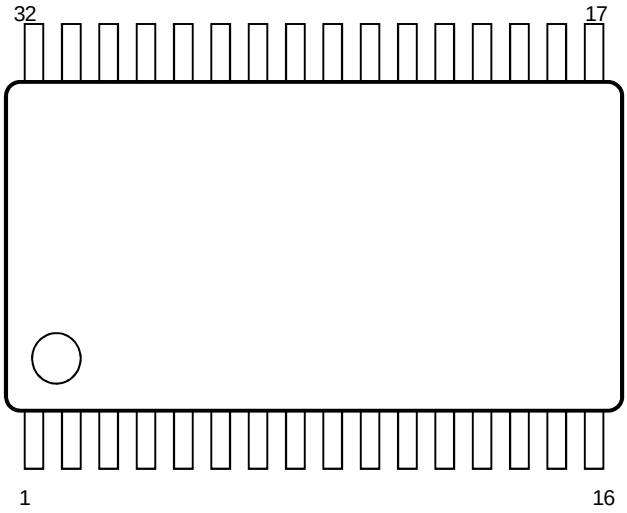
■±18V OPERATION AUDIO VOLUME VARIATION

OPERATING VOLTAGE	PRODUCT NAME
±8.5 to ±18V	MUSES72320
±10 to ±18V	NJU72322

■BLOCK DIAGRAM

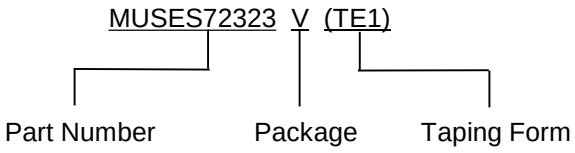


■PIN CONFIGURATION



No.	Symbol	Function	No.	Symbol	Function
1	NC	No connection	17	CLK_IN	External clock signal input for soft-step
2	L_CAP	Lch switching noise rejection capacitor connection terminal	18	DATA	Control data signal input
3	OUTL	Lch output	19	CLOCK	Clock signal input
4	L-	Lch Op-amp inverting input connection terminal	20	LATCH	Latch signal input
5	L_REF	Lch reference voltage	21	D_V+	Power supply (+) [digital block] (+10V to +18V)
6	L+	Lch Op-amp non-inverting input connection terminal	22	INR	Rch input
7	L_REF	Lch reference voltage	23	AR_V+	Power supply (+) [Rch] (+10V to +18V)
8	L_REF	Lch reference voltage	24	AL_V+	Power supply (+) [Lch] (+10V to +18V)
9	R_REF	Rch reference voltage	25	AR_V-	Power supply (-) [Rch] (-10V to -18V)
10	R_REF	Rch reference voltage	26	AL_V-	Power supply (-) [Lch] (-10V to -18V)
11	R+	Rch Op-amp non-inverting input connection terminal	27	INL	Lch Input
12	R_REF	Rch reference voltage	28	D_V-	Power supply (-) [digital block] (-10V to -18V)
13	R-	Rch Op-amp inverting input connection terminal	29	D_CAP	Digital block noise rejection capacitor connection terminal
14	OUTR	Rch output	30	ADR0	Chip address setting terminal 0
15	R_CAP	Rch switching noise rejection capacitor connection terminal	31	ADR1	Chip address setting terminal 1
16	D_IN	Digital block power supply (+3.0V to +5.5V)	32	D_REF	Digital block reference voltage

■PRODUCT NAME INFORMATION



■ORDERING INFORMATION

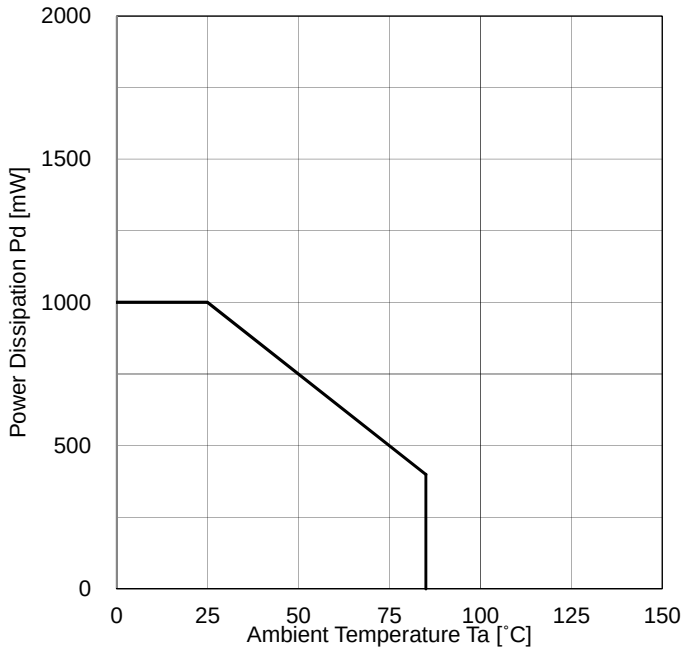
PART NUMBER	PACKAGE OUTLINE	RoHS	HALOGEN-FREE	TERMINAL FINISH	MARKING	WEIGHT (mg)	MOQ(pcs)
MUSES72323V (TE1)	SSOP32	yes	yes	Sn-2Bi	MUSES72323	185	100

■ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+/V^-	+20/-20	V
Digital Block Voltage	V_{D_CAP}	V^- +6 *1)	V
Digital Input Voltage	V_{ID}	6 *2)	V
Analog Input Voltage	V_{IA}	V^+/V^- *3)	V
Power Dissipation	P_D	1000 *4)	mW
Junction Temperature	T_{jmax}	+125	°C
Storage Temperature Range	Tstg	-40 to +125	°C

*1) D_CAP terminal.
*2) D_IN, CLK_IN, DATA, CLOCK, LATCH terminals.
*3) INL, INR terminals.
*4) EIA/JEDEC STANDARD Test board (76.2 * 114.3 * 1.6mm, 2layers, FR-4) mounting.

■POWER DISSIPATION vs. AMBIENT TEMPERATURE



■RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V^+/V^-	-	±10	±15	±18	V
Digital Block Control Voltage	D_IN	D_REF(32pin)=0V	3.0	5.0	5.5	V
Operating Temperature Range	Topr	-	-40	-	85	°C

■ELECTRICAL CHARACTERISTICS

♦DC CHARACTERISTICS (Ta=25°C, V^+/V^-=±15V)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Current 1	I_{CC}	No Signal, No Load	-	2	10	mA
Supply Current 2	I_{EE}	No Signal, No Load	-	2	10	mA
Input Impedance	R_{IN}	INR(22pin), INL(27pin) terminals	14	20	-	kΩ

♦AC CHARACTERISTICS

(Ta= 25°C, V^+/V^-= ±15V, f= 1kHz, V_{IN}= 2Vrms, Volume= 0dB, Gain= 0dB, V_{OUT} with MUSES8920, R_L= 47kΩ, unless otherwise specified)

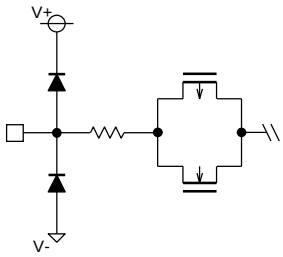
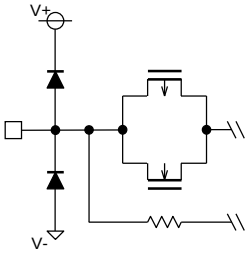
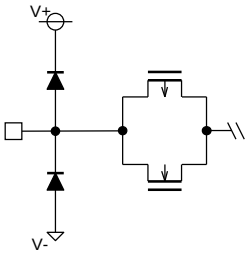
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Maximum Input Voltage	V_{IM}	THD=1%, Volume=-20dB	11	-	-	Vrms
Maximum Output Voltage	V_{OM}	THD=1%	-	10.3	-	Vrms
Voltage Gain 1	G_{V1}	-	-0.5	0	+0.5	dB
Voltage Gain 2	G_{V2}	V_{IN}=0.5Vrms, Gain=+12dB	+11	+12	+13	dB
Voltage Gain Error 1	ΔG_{V1}	-	-0.5	0	+0.5	dB
Voltage Gain Error 2	ΔG_{V2}	Volume=-60dB	-1.0	0	+1.0	dB
Maximum Attenuation	A_{TT}	Volume=-111.75dB, A-weight	-	-111.75	-	dB
Mute Level	Mute	Volume=Mute, A-weight	-	-120	-	dB
Total Harmonic Distortion 1	THD1	V_{IN}=1.6Vrms BW=400 to 22kHz	-	0.00024	-	%
Total Harmonic Distortion 2	THD2	f=10kHz, V_{IN}=1Vrms BW=400 to 30kHz	-	0.0007	-	%
Output Noise	V_{NO}	Rg=0Ω, A-weight, R_L=100kΩ	-	-124 (0.63μ)	-	dBV (Vrms)
Channel Separation 1	CS1	Rg=0Ω	-	-110	-90	dB
Channel Separation 2	CS2	f=20kHz, Rg=0Ω	-	-90	-	dB

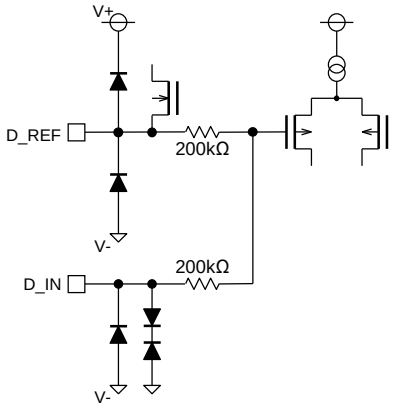
♦LOGIC CONTROL CHARACTERISTICS

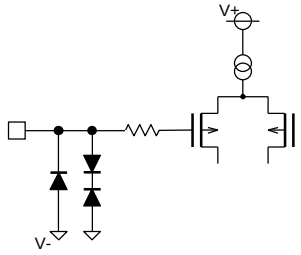
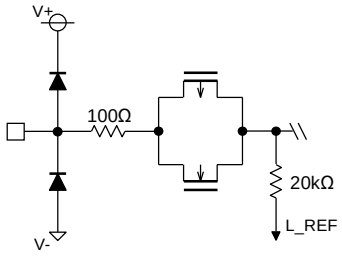
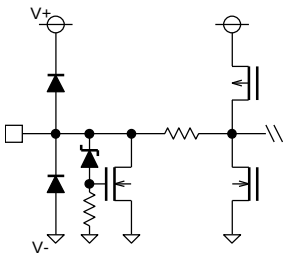
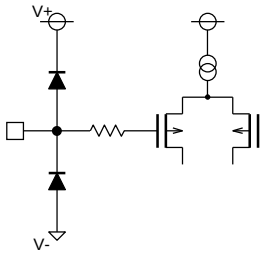
(Ta=25°C, V^+/V^-=±15V, D_{VDD}="D_IN"-"D_REF", unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
High Level Input Voltage 1	V_{IH1}	DATA, CLOCK, LATCH, CLK_IN terminals	0.7*D_{VDD}	-	5.5	V
Low Level Input Voltage 1	V_{IL1}		0	-	0.3*D_{VDD}	V
High Level Input Voltage 2	V_{IH2}	ADR0, ADR1 terminals	0.7*D_{VDD}	-	V^+	V
Low Level Input Voltage 2	V_{IL2}		0	-	0.3*D_{VDD}	V

■TERMINAL DESCRIPTION

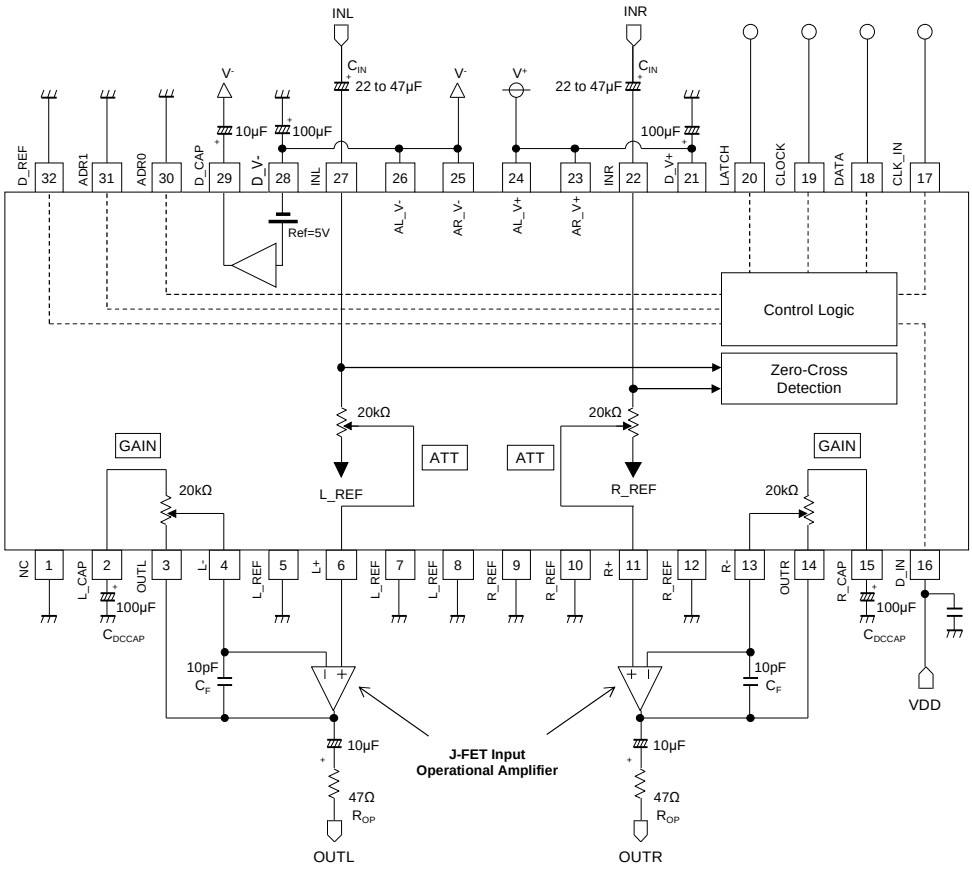
PIN NO.	SYMBOL	FUNCTION	EQUIVALENT CIRCUIT	TERMINAL VOLTAGE
2	L_CAP	Lch switching noise rejection capacitor connection terminal		0V
15	R_CAP	Rch switching noise rejection capacitor connection terminal		
3	OUTL	Lch output		0V
5	L_REF	Lch Reference Voltage		
7	L_REF	Lch Reference Voltage		
8	L_REF	Lch Reference Voltage		
9	R_REF	Rch Reference Voltage		
10	R_REF	Rch Reference Voltage		
12	R_REF	Rch Reference Voltage		
14	OUTR	Rch output		
4	L-	Lch Op-amp inverting input connection terminal		0V
6	L+	Lch Op-amp non-inverting input connection terminal		
11	R+	Rch Op-amp non-inverting input connection terminal		
13	R-	Rch Op-amp inverting input connection terminal		

16 32	D_IN D_REF	Digital block power supply Digital block reference voltage		0V

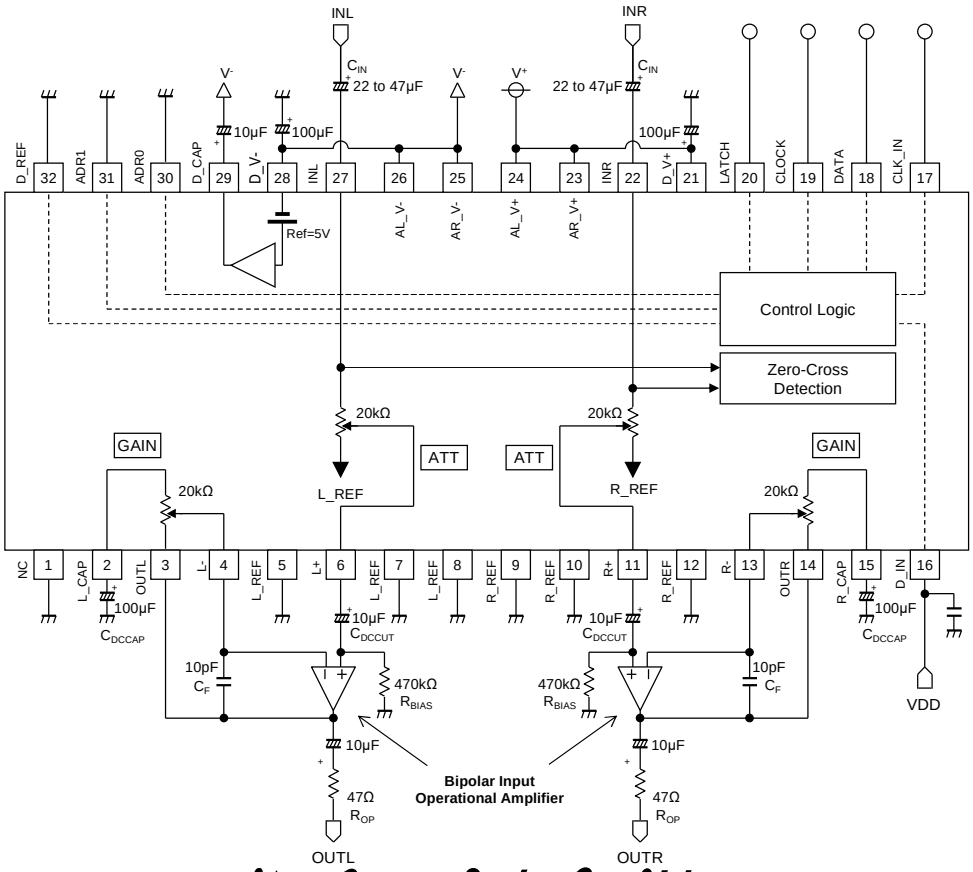
PIN NO.	SYMBOL	FUNCTION	EQUIVALENT CIRCUIT	TERMINAL VOLTAGE
17 18 19 20	CLK_IN DATA CLOCK LATCH	External clock signal input for soft-step Control data signal input Clock signal input Latch signal input		-
22 27	INR INL	Rch input Lch input		0V
29	D_CAP	Digital block noise rejection capacitor connection terminal		V^- + 5V
30	ADR0 ADR1	Chip address setting terminal		-

■APPLICATION CIRCUIT

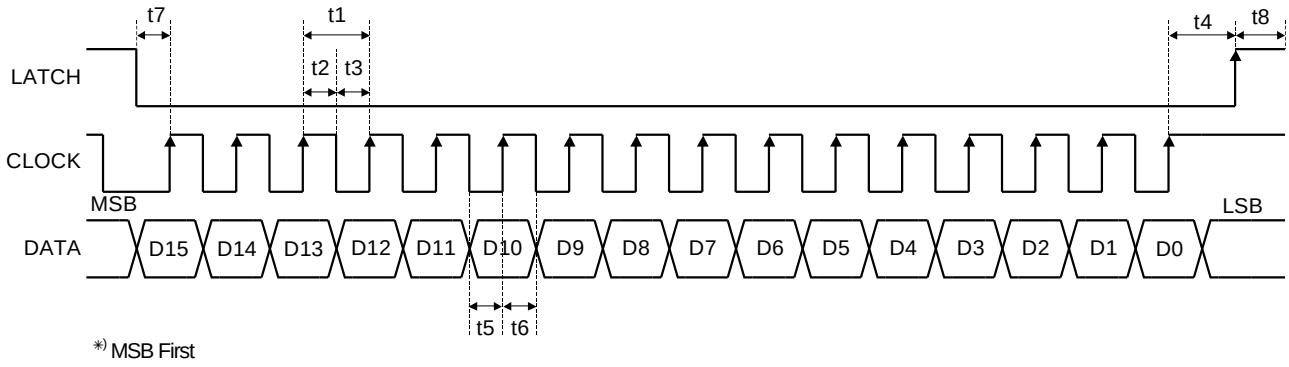
♦Application circuit with J-FET input type Op-Amp.



♦Application circuit with Bipolar input type Op-Amp.



■TIMING ON 3-wired BUS (DATA, CLOCK, LATCH)



■CHARACTERISTICS OF BUS LINES (DATA, CLOCK, LATCH) FOR 3-wired BUS DEVICES

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
t1	CLOCK Clock Width	1	-	-	µsec
t2	CLOCK Pulse Width(High)	0.4	-	-	µsec
t3	CLOCK Pulse Width(Low)	0.4	-	-	µsec
t4	LATCH Rise Hold Time	1	-	-	µsec
t5	DATA Setup Time	0.4	-	-	µsec
t6	DATA Hold Time	0.4	-	-	µsec
t7	CLOCK Setup Time	0.4	-	-	µsec
t8	LATCH Pulse Width(High)	0.4	-	-	µsec

■SOFT-STEP OPERATION

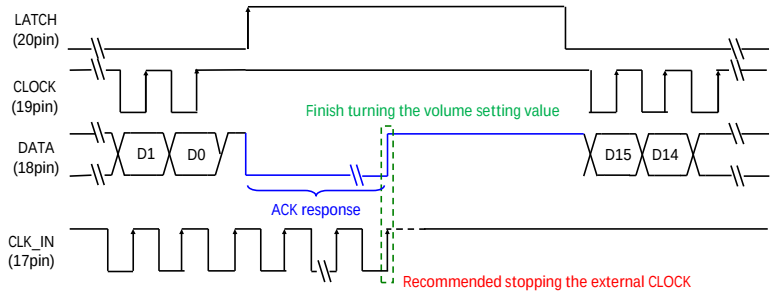
♦Clock for Soft-Step

The clock for soft-step can select the internal clock or the external clock (CLK_IN: 17 pin). The internal clock is automatically stopped when the volume gain reaches the setting value in the case of the internal clock operation. It is recommended to stop the external clock when the volume gain reaches the setting value in the case of the external clock operation.

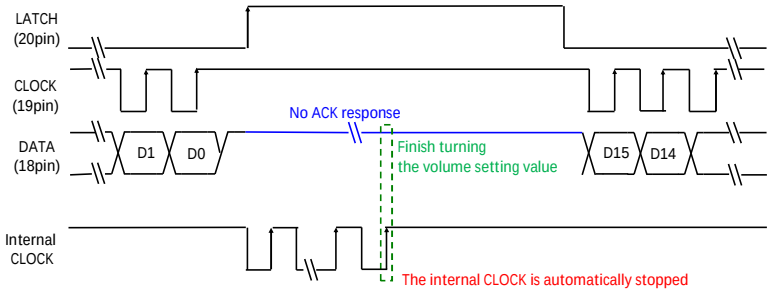
♦ACK Response for Soft-Step

Control device can detect that the volume gain reaches the setting value by the ACK response. It is necessary to wait DATA="H" at LATCH="H" for the ACK response. The DATA terminal is the ACK response (Low level) at LATCH="H" during turning the setting value. The ACK response stops (the data terminal is High level) when the volume gain reaches the setting value. This ACK response function operates in the external clock operation. It does not operate in the case that it operates in internal clock operation or soft-step function is OFF.

External clock operation

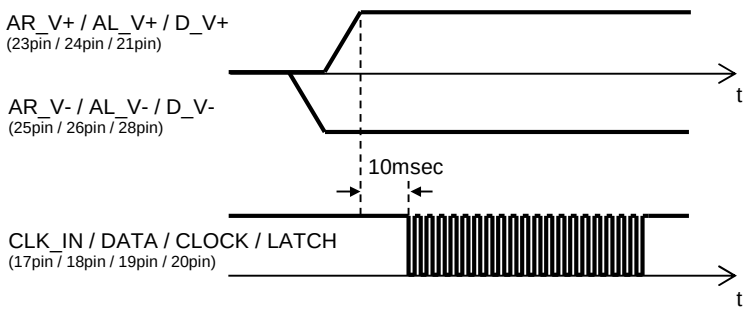


Internal clock operation



■RECOMMENDED POWER-UP SEQUENCE

The MUSES72323 should be used under the condition that potential V- terminals are always the lowest potential.
It is recommended that V- power supply turns on before or just same time that V+ power supply turns on.



■DEFINITION OF 3-wired REGISTER

Note) Please don't send except specified data for avoiding an incorrect operation.

♦3-wired BUS FORMAT / CONTROL RESISTER TABLE

The MUSES72323 control data is constructed with 16bits.

MSB LSB

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Data												Select Address		Chip Address	

MSB LSB

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
L channel Volume									0	0	SS_L	0	0	*	*
R channel Volume									0	0	SS_R	0	1	*	*
L/R Cont	L channel Gain			R channel Gain			Z/C	0	0	0	0	1	0	*	*
0	Zero Window		CLK_Div			SS_CLK	0	0	0	0	0	1	1	*	*

♦CHIP ADDRESS

Chip address is set by the ADR0 and the ADR1 (chip address setting terminal) status.

Chip address setting terminal		Chip Address	
ADR1 (31pin)	ADR0 (30pin)	D1	D0
Low	Low	0	0
Low	High	0	1
High	Low	1	0
High	High	1	1

♦CONTROL REGISTER DEFAULT VALUE

MSB LSB

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	*
0	0	0	0	0	0	0	0	0	0	0	0	0	1	*	*
0	0	0	0	0	0	0	0	0	0	0	0	1	0	*	*
0	0	0	0	0	0	0	0	0	0	0	0	1	1	*	*

Note) This product starts up by MUTE setting in power “ON”. Use it after removing MUTE of each setting.

If any audio signal is inputted in input signal terminal before power “ON”, it may cause initial condition abnormality. In conditions of using such as the above, it prevents that abnormality by setting MUTE before power “OFF".

■DEFINITION OF RESISTOR

♦Volume : 0 to -111.75dB / 0.25dB step.
Each volume is controlled independently when L/RCont="0".

♦SS_L/R : Soft-Step circuit ON/OFF setting.
Soft step function reduces zipper noise during gain adjustment.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
L channel Volume									0	0	SS_L	0	0	*	*
R channel Volume									0	0	SS_R	0	1	*	*

< L channel Volume / R channel Volume Setting >

Data									Setting
D15	D14	D13	D12	D11	D10	D9	D8	D7	
0	0	0	0	0	0	0	0	0	Mute(*)
0	0	0	1	0	0	0	0	0	0dB
0	0	0	1	0	0	0	0	1	-0.25dB
0	0	0	1	0	0	0	1	0	-0.5dB
0	0	0	1	0	0	0	1	1	-0.75dB
0	0	0	1	0	0	1	0	0	-1dB
0	0	0	1	0	0	1	0	1	-1.25dB
0	0	0	1	0	0	1	1	0	-1.5dB
0	0	0	1	0	0	1	1	1	-1.75dB
0	0	0	1	0	1	0	0	0	-2dB
0	0	0	1	0	1	0	0	1	-2.25dB
0	0	0	1	0	1	0	1	0	-2.5dB
0	0	0	1	0	1	0	1	1	-2.75dB
0	0	0	1	0	1	1	0	0	-3dB
0	0	0	1	0	1	1	0	1	-3.25dB
0	0	0	1	0	1	1	1	0	-3.5dB
0	0	0	1	0	1	1	1	1	-3.75dB
0	0	0	1	1	0	0	0	0	-4dB
0	0	0	1	1	0	0	0	1	-4.25dB
0	0	0	1	1	0	0	1	0	-4.5dB
0	0	0	1	1	0	0	1	1	-4.75dB
0	0	0	1	1	0	1	0	0	-5dB
0	0	0	1	1	0	1	0	1	-5.25dB
0	0	0	1	1	0	1	1	0	-5.5dB
0	0	0	1	1	0	1	1	1	-5.75dB
0	0	0	1	1	1	0	0	0	-6dB
0	0	0	1	1	1	0	0	1	-6.25dB
0	0	0	1	1	1	0	1	0	-6.5dB
0	0	0	1	1	1	0	1	1	-6.75dB
0	0	0	1	1	1	1	0	0	-7dB
0	0	0	1	1	1	1	0	1	-7.25dB
0	0	0	1	1	1	1	1	0	-7.5dB
0	0	0	1	1	1	1	1	1	-7.75dB
0	0	1	0	0	0	0	0	0	-8dB

1	1	1	0	0	0	0	0	0	-104dB
1	1	1	0	0	0	0	0	1	-104.25dB
1	1	1	0	0	0	0	1	0	-104.5dB
1	1	1	0	0	0	0	1	1	-104.75dB
1	1	1	0	0	0	1	0	0	-105dB
1	1	1	0	0	0	1	0	1	-105.25dB
1	1	1	0	0	0	1	1	0	-105.5dB
1	1	1	0	0	0	1	1	1	-105.75dB
1	1	1	0	0	1	0	0	0	-106dB
1	1	1	0	0	1	0	0	1	-106.25dB
1	1	1	0	0	1	0	1	0	-106.5dB
1	1	1	0	0	1	0	1	1	-106.75dB
1	1	1	0	0	1	1	0	0	-107dB
1	1	1	0	0	1	1	0	1	-107.25dB
1	1	1	0	0	1	1	1	0	-107.5dB
1	1	1	0	0	1	1	1	1	-107.75dB
1	1	1	0	1	0	0	0	0	-108dB
1	1	1	0	1	0	0	0	1	-108.25dB
1	1	1	0	1	0	0	1	0	-108.5dB
1	1	1	0	1	0	0	1	1	-108.75dB
1	1	1	0	1	0	1	0	0	-109dB
1	1	1	0	1	0	1	0	1	-109.25dB
1	1	1	0	1	0	1	1	0	-109.5dB
1	1	1	0	1	0	1	1	1	-109.75dB
1	1	1	0	1	1	0	0	0	-110dB
1	1	1	0	1	1	0	0	1	-110.25dB
1	1	1	0	1	1	0	1	0	-110.5dB
1	1	1	0	1	1	0	1	1	-110.75dB
1	1	1	0	1	1	1	0	0	-111dB
1	1	1	0	1	1	1	0	1	-111.25dB
1	1	1	0	1	1	1	1	0	-111.5dB
1	1	1	0	1	1	1	1	1	-111.75dB
1	1	1	1	1	1	1	1	*	Mute

(*)Default Setting

< SS_L / SS_R Setting >

Data	Setting
D4	
0	Soft-Step OFF(*)
1	Soft-Step ON

(*)Default Setting

Note) Set the SS_L/SS_R setting after a power-up immediately. Set SS_L/SS_R when volume setting sets Mute in other cases.

♦**L/R Cont :** Select “L channel Volume, R channel Volume independent control” or “L channel Volume, R channel Volume link control” of method of volume control.

♦**Gain :** 0 to +21dB / 3dB step. Each gain is controlled independently.

♦**Z/C :** Zero Cross Detection circuit ON/OFF setting.
Zero cross function changes the gain setting when the input signal is near 0 V and reduces audible noise generated during gain adjustment.
When the zero-crossing detection circuit is ON, new gain setting is not reflected until the input signal is within the range of ± 25 mV.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
L/R Cont	L channel Gain			R channel Gain			Z/C	0	0	0	0	1	0	*	*

<L/R Cont Setting>

Data	Setting
D15	
0	L channel Volume, R channel Volume independent control(*)
1	L channel Volume, R channel Volume link control

(*)Default Setting

Command table when L channel Volume and R channel Volume are linked

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
L /R channel Volume								0	0	0	SS_L	0	0	*	*
No Acceptable								0	0	0	SS_R	0	1	*	*

<L channel Gain / R channel Gain Setting>

Data			Setting
D14	D13	D12	
D11	D10	D9	
0	0	0	0dB(*)
0	0	1	+3dB
0	1	0	+6dB
0	1	1	+9dB
1	0	0	+12dB
1	0	1	+15dB
1	1	0	+18dB
1	1	1	+21dB

(*)Default Setting

<Z/C Setting>

Data	Setting
D8	
0	Zero Cross Detection Circuit ON(*)
1	Zero Cross Detection Circuit OFF

(*)Default Setting

♦**Zero Window :** Select Zero Cross Detection range setting.
♦**CLK_Div :** Select clock frequency dividing for Soft-Step.
♦**SS_CLK :** Select clock operation for Soft-Step.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	Zero Window		CLK_Div			SS_ CLK	0	0	0	0	0	1	1	*	*

<Zero Window Setting>

Data		Setting
D14	D13	
0	0	Default (*)
0	1	Default *2
1	0	Default *4
1	1	Default *8

(*)Default Setting

<CLK_Div Setting>

Data			Setting
D12	D11	D10	
0	0	0	Default (*)
0	0	1	Default /4
0	1	0	Default /8
0	1	1	Default /16
1	0	0	Default /32
1	0	1	Default /64
1	1	0	Default /128
1	1	1	Default /256

(*)Default Setting

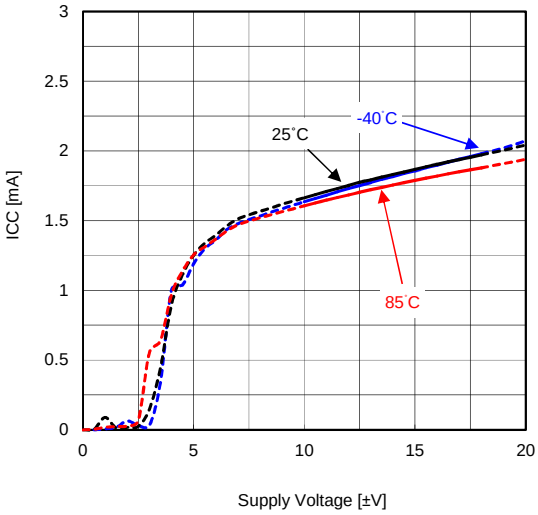
<SS_CLK Setting>

Data	Setting
D9	
0	External clock operation (*)
1	Internal clock operation

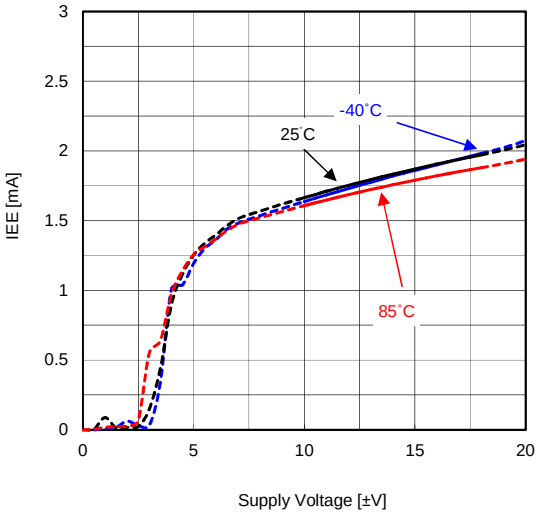
(*)Default Setting

■ TYPICAL CHARACTERISTICS

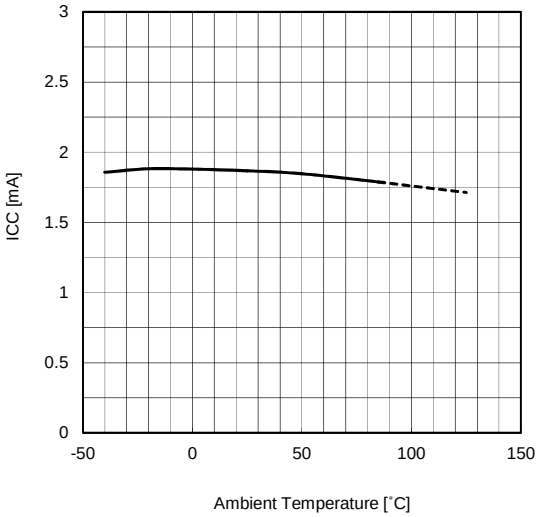
ICC vs Supply Voltage
No Signal



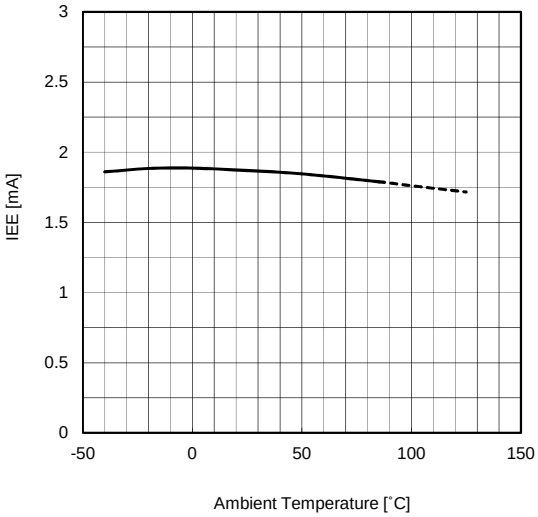
IEE vs Supply Voltage
No Signal



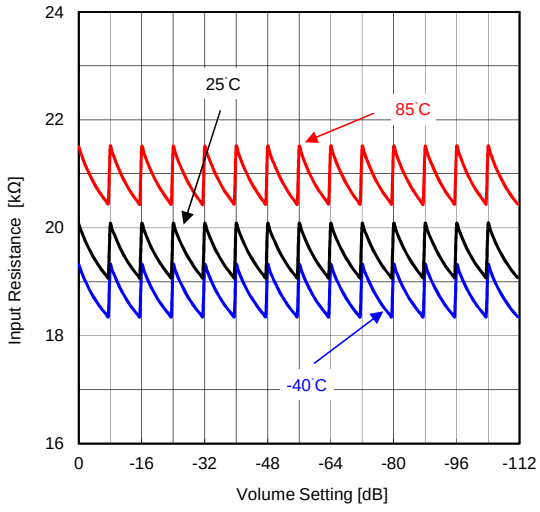
ICC vs Ambient Temperature
V=±15V, No Signal



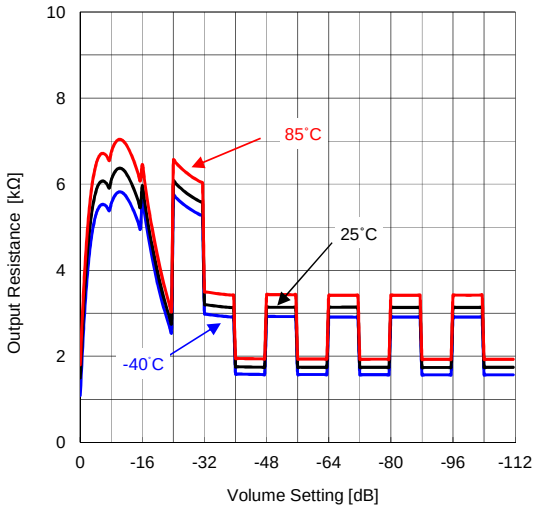
IEE vs Ambient Temperature
V=±15V, No Signal



Input Resistance vs Volume Setting
V=±15V, No signal

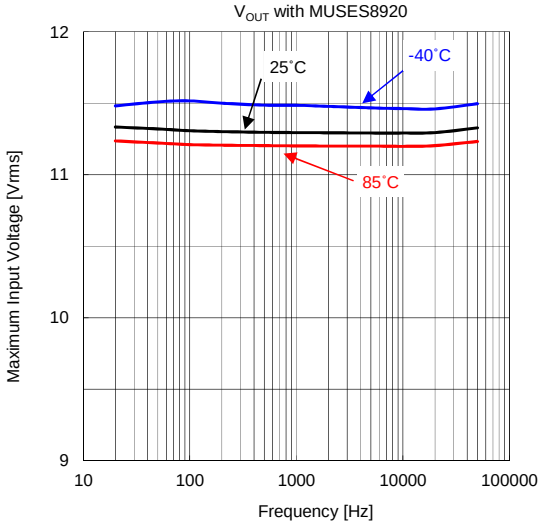


Output Resistance vs Volume Setting
V=±15V, No signal

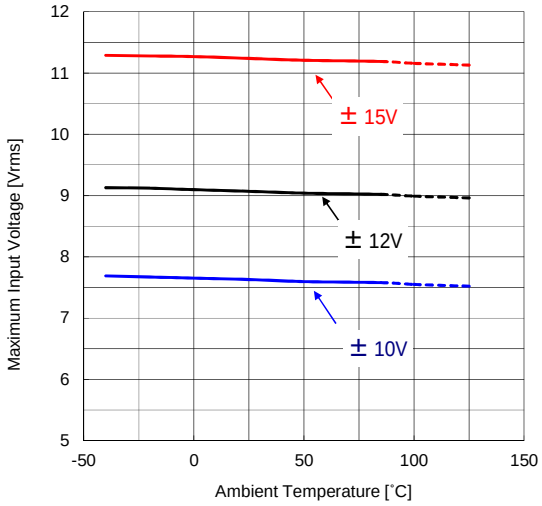


■ TYPICAL CHARACTERISTICS

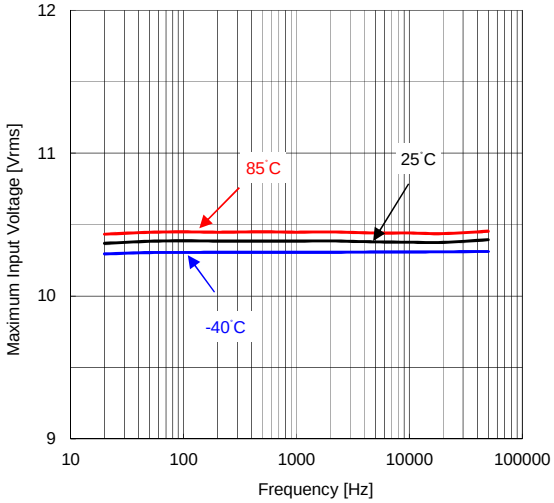
Maximum Input Voltage vs Frequency
V=±15V, THD=1%, Volume=-20dB, Gain=0dB,
V_{OUT} with MUSES8920



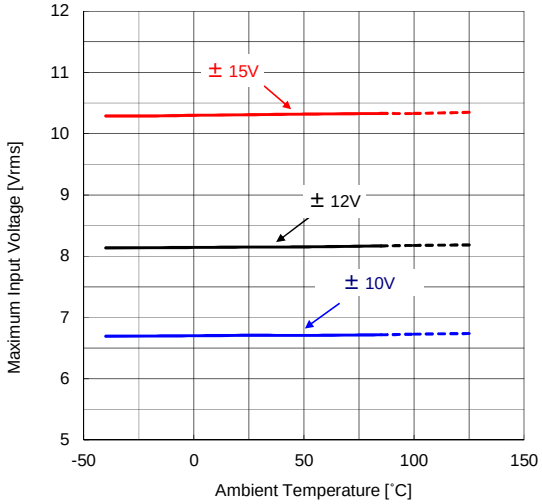
Maximum Input Voltage vs Ambient Temperature
f=1kHz, THD=1%, Volume=-20dB, Gain=0dB,
V_{OUT} with MUSES8920



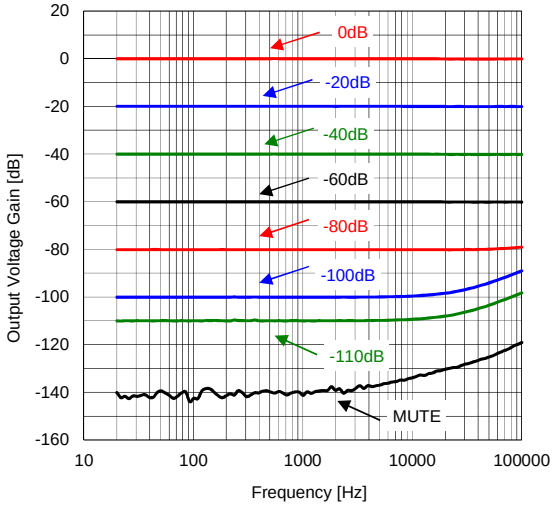
Maximum Output Voltage vs Frequency
V=±15V, THD=1%, V_{OUT} with MUSES8920



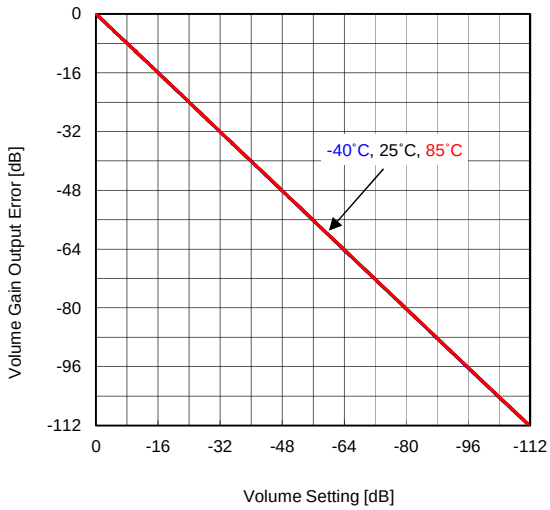
Maximum Output Voltage vs Ambient Temperature
f=1kHz, THD=1%, V_{OUT} with MUSES8920



Output Voltage Gain vs Frequency
V=±15V, Vin=4Vrms, Bandpass

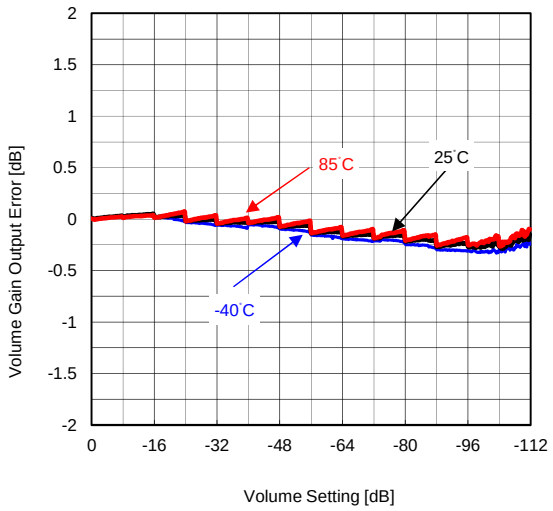


Volume Gain Output vs Volume Setting
V=±15V, f=1kHz, Vin=4Vrms, Gain=0dB, Bandpass

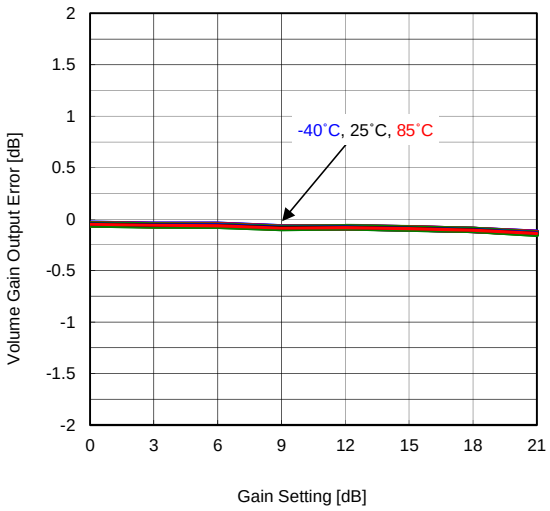


■ TYPICAL CHARACTERISTICS

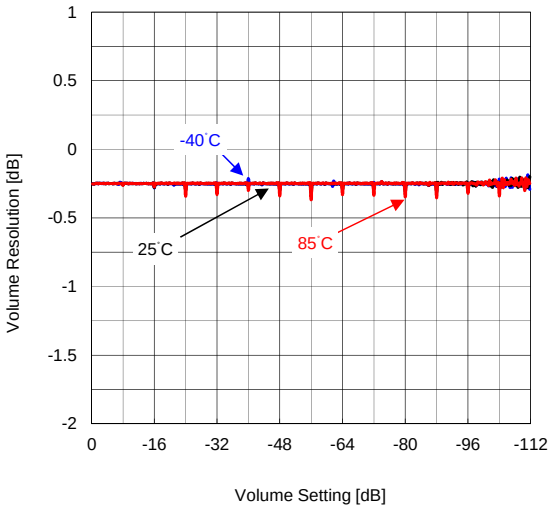
Volume Gain Output Error vs Volume Setting
V=±15V, f=1kHz, Vin=4Vrms, Gain=0dB, Bandpass



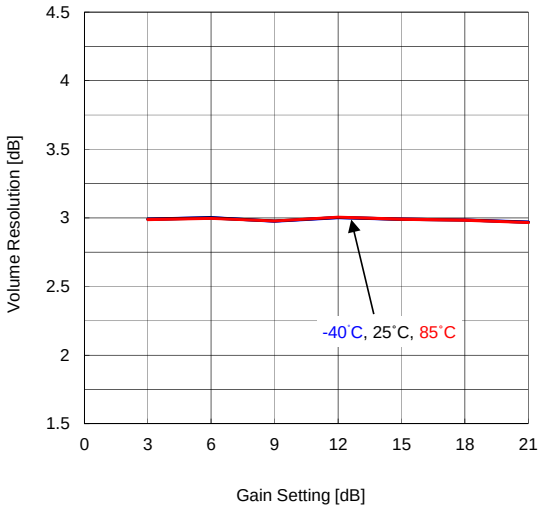
Volume Gain Output Error vs Volume Setting
V=±15V, f=1kHz, Vin=200mVrms, Volume=0dB, Bandpass



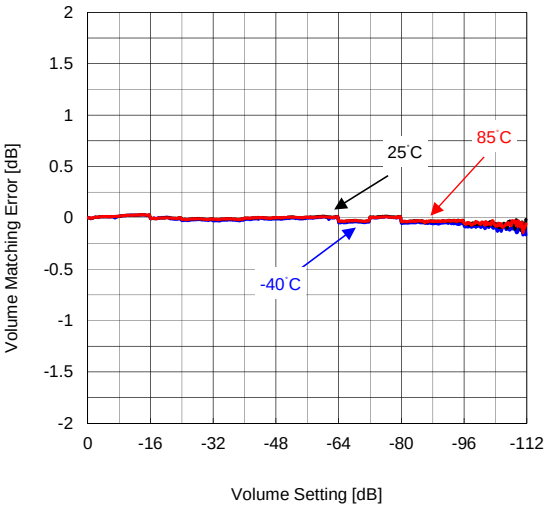
Volume Resolution vs Volume Setting
V=±15V, f=1kHz, Vin=4Vrms, Gain=0dB, Bandpass



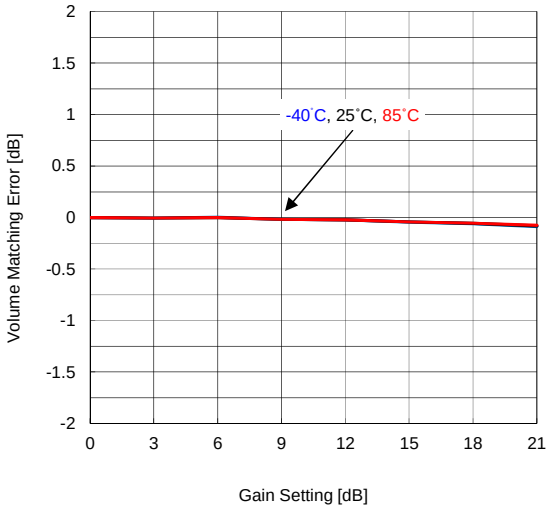
Volume Resolution vs Volume Setting
V=±15V, f=1kHz, Vin=200mVrms, Volume=0dB, Bandpass



Volume Matching Error vs Volume Setting
V=±15V, f=1kHz, Vin=4Vrms, Gain=0dB, Bandpass

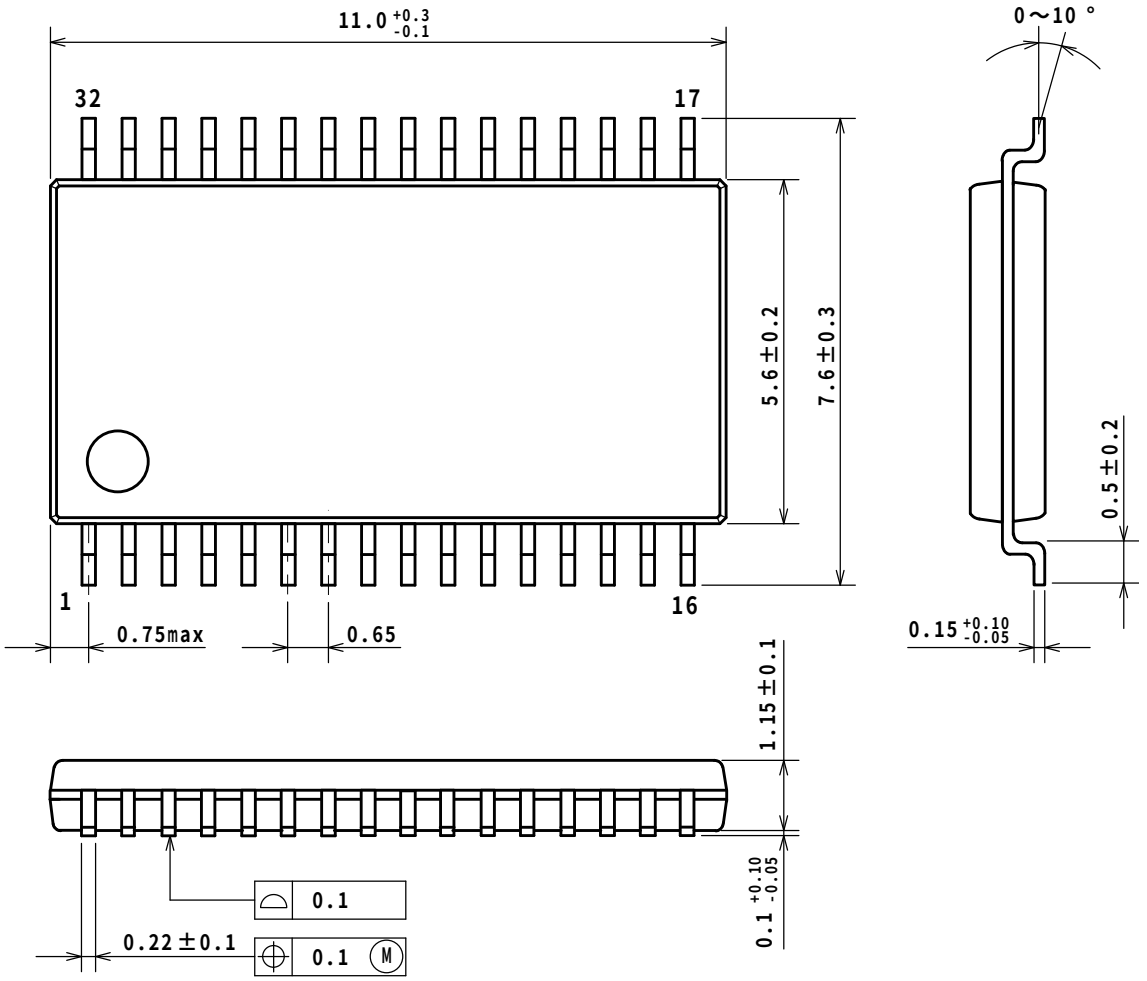


Volume Matching Error vs Volume Setting
V=±15V, f=1kHz, Vin=200mVrms, Volume=0dB, Bandpass

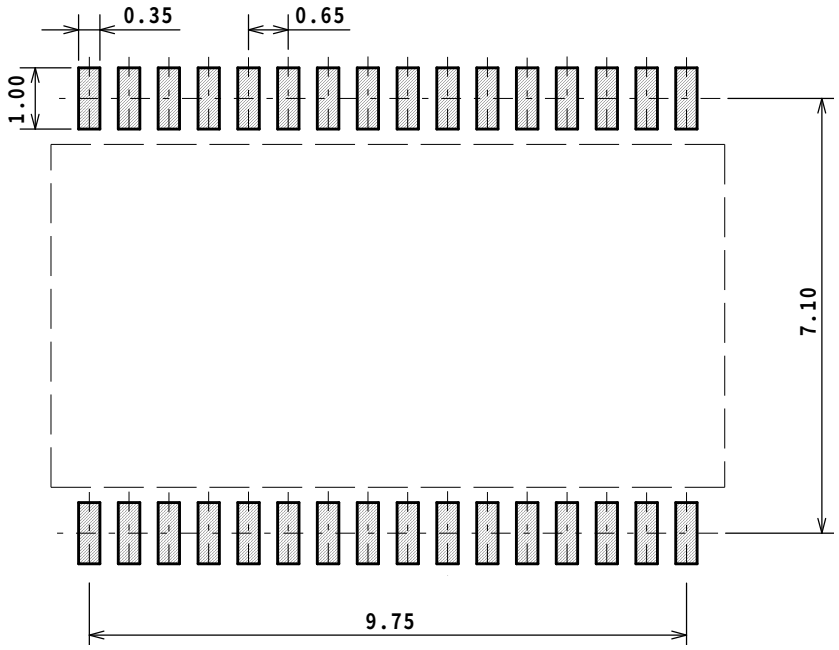


■PACKAGE DIMENSIONS

Unit: mm



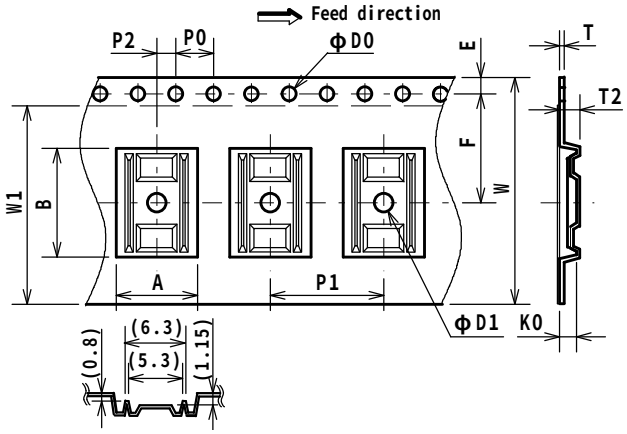
■EXAMPLE OF SOLDER PADS DIMENSIONS



■PACKING SPEC

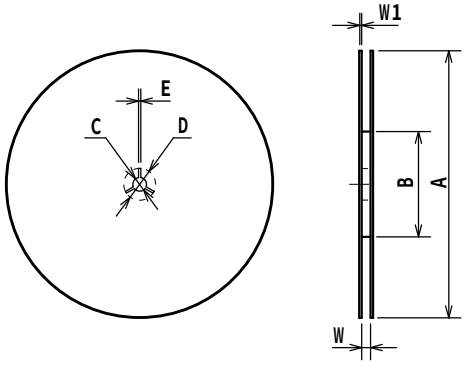
Unit: mm

TAPING DIMENSIONS



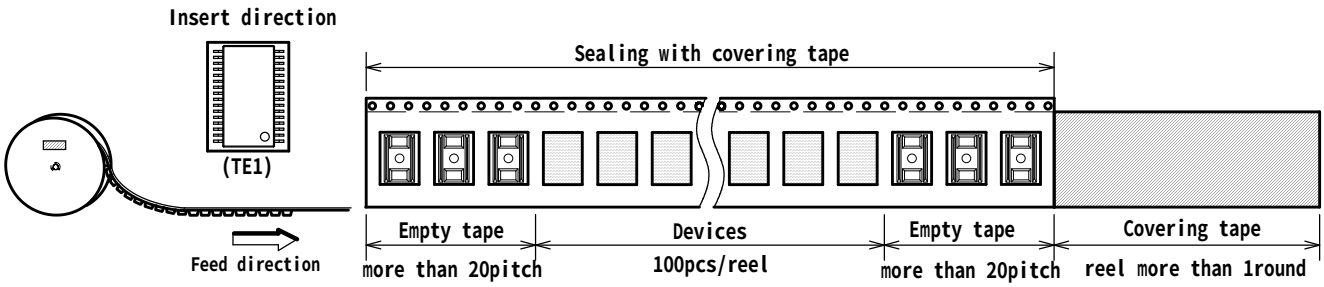
SYMBOL	DIMENSION	REMARKS
A	8.4±0.1	BOTTOM DIMENSION
B	11.35±0.1	BOTTOM DIMENSION
D0	$1.5^{+0.1}_{0}$	
D1	$2.0^{+0.1}_{0}$	
E	1.75±0.1	
F	11.5±0.1	
P0	4.0±0.1	
P1	12.0±0.1	
P2	2.0±0.1	
T	0.3±0.05	
T2	2.15	
K0	1.8±0.1	
W	24.0±0.3	
W1	21.0±0.1	

REEL DIMENSIONS

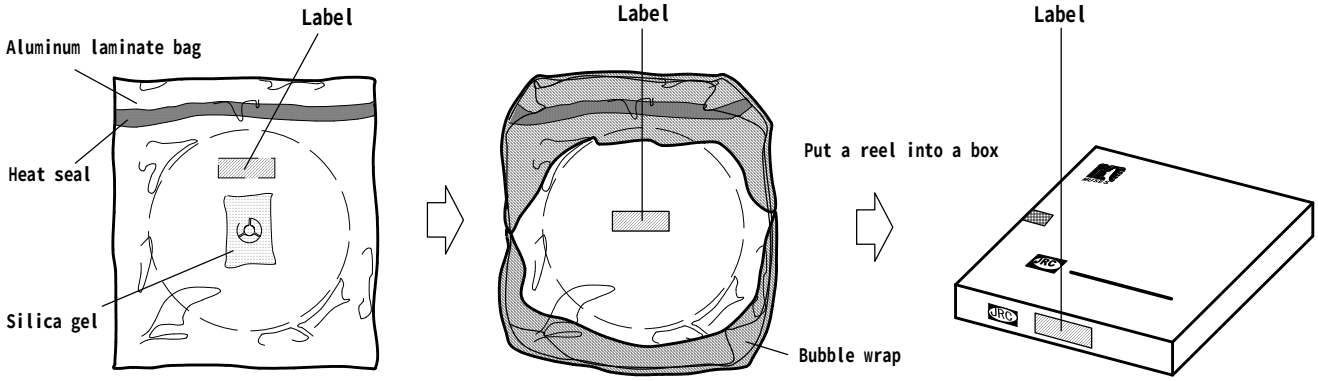


SYMBOL	DIMENSION
A	φ254±2
B	φ100±1
C	φ 13±0.2
D	φ 21±0.8
E	2±0.5
W	25.5±1.0
W1	2

TAPING STATE



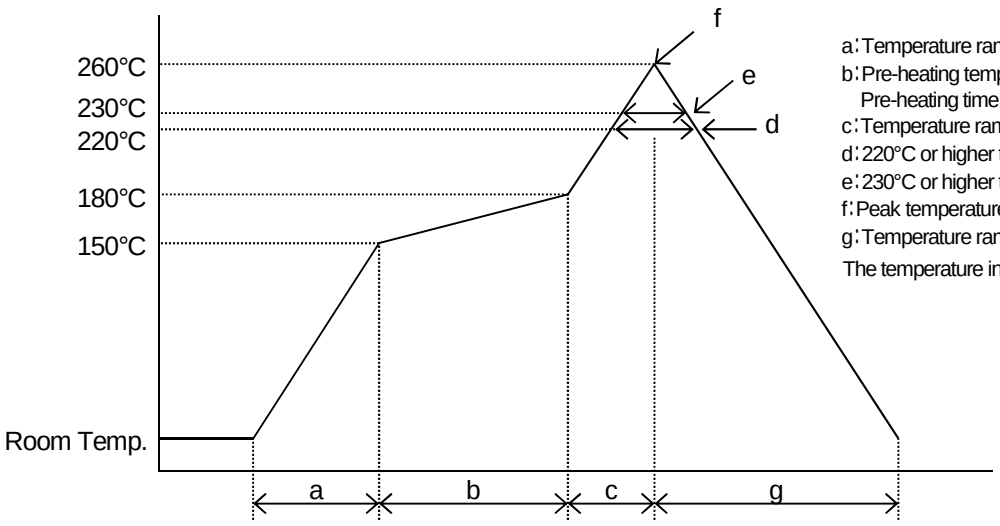
PACKING STATE



■RECOMMENDED MOUNTING METHOD

INFRARED REFLOW SOLDERING METHOD

Recommended reflow soldering procedure



a: Temperature ramping rate	: 1 to 4°C/s
b: Pre-heating temperature	: 150 to 180°C
Pre-heating time	: 60 to 120s
c: Temperature ramp rate	: 1 to 4°C/s
d: 220°C or higher time	: Shorter than 60s
e: 230°C or higher time	: Shorter than 40s
f: Peak temperature	: Lower than 260°C
g: Temperature ramping rate	: 1 to 6°C/s

The temperature indicates at the surface of mold package.

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