

SECTION 4 — TRANSISTOR CONSTRUCTIONS

P-N-P Alloy Junction Transistors

The earliest transistors were made by the point contact method but this technique was soon superseded by the alloy-junction construction. The point-contact fabrication is now used only for certain diodes. For the first decade or so after the invention of the transistor in 1948, nearly all the devices available were of the alloy-junction type illustrated in fig. 26. Most alloy-junction devices are p-n-p and are made from germanium. Two pellets of trivalent material, usually indium, are placed in a jig on each side of an n-type germanium wafer (often called a die, plural dice). Typical dimensions for the wafer are $3 \times 15 \times 0.3$ mm and its resistivity is about $5\Omega \cdot \text{cm}$. The collector pellet is about three times larger than the emitter pellet, fig. 26(i). These components and the nickel tab are heated up in the jig to about 500°C . The indium melts and dissolves some germanium from the wafer. After cooling and recrystallisation, regions of p-type material form as shown in fig. 26(ii). During the heating the nickel base tab also bonds to the base wafer. The electrodes are then wired to the connecting leads, fig. 26(iii), and the device encapsulated.

Note: The shapes of the various p and n regions in the diagrams of this section have been simplified in the interests of clarity.

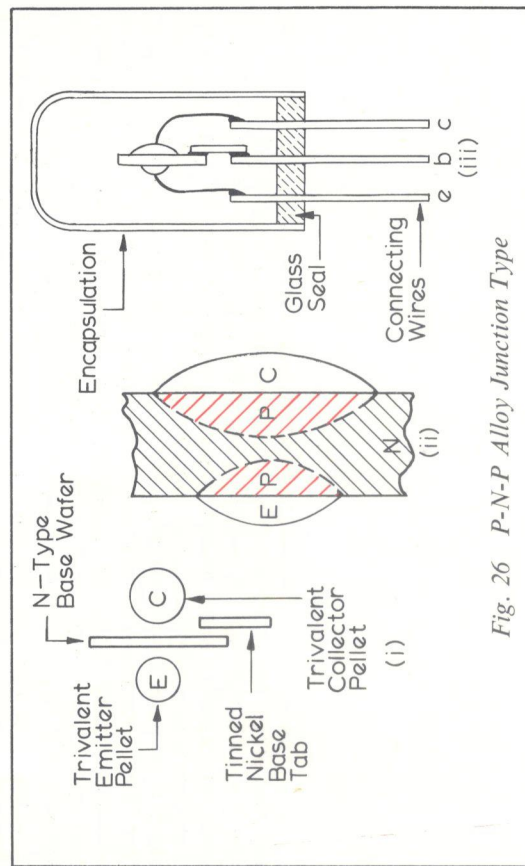


Fig. 26 P-N-P Alloy Junction Type

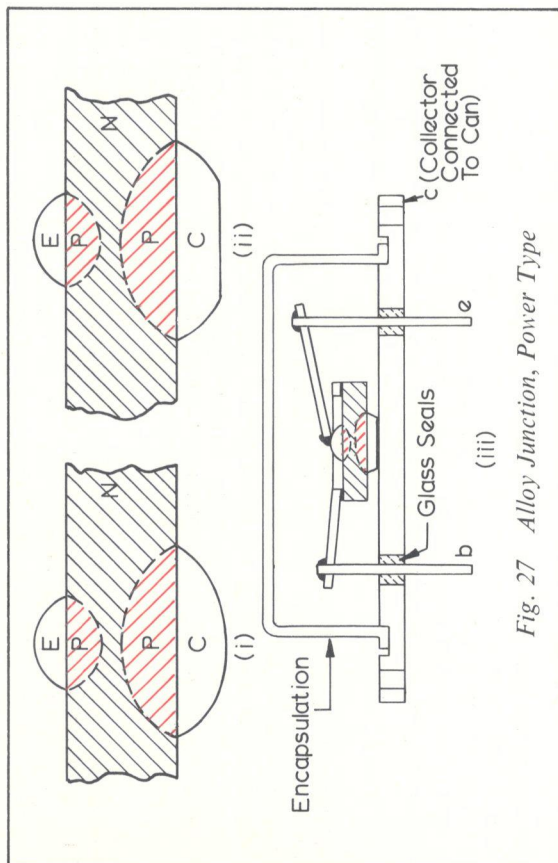


Fig. 27 Alloy Junction, Power Type

Alloy-Junction Power Transistors

Where more power dissipation is required than would be possible from an ordinary alloy-junction type, a different construction is used, fig. 27. The alloying process for the high power type is identical to that of fig. 26 except that the materials used have larger dimensions. Before encapsulation the collector is cut flat as indicated in fig. 27(ii) and bonded to the header fig. 27(iii). Finally the base and emitter tabs are soldered in position and the encapsulation completed. The transistor can be bolted flat on to a heatsink which becomes the collector connection.

Alloy-Diffused Transistors

The transistor is built on a wafer of p-type germanium which is later used as the collector. Two metal pellets, one (B) for the base and the other (E) for the emitter are placed close together on one side of the wafer, fig. 28(i). Pellet E contains both trivalent and pentavalent impurities whereas pellet B contains only pentavalent impurities. The whole assembly is heated in an atmosphere containing the vapour of a pentavalent element. The trivalent material in pellet E penetrates only a negligible amount into the wafer but the pentavalent impurity in both pellets penetrates the wafer as shown in fig. 28(ii). At the same time pentavalent impurity atoms diffuse into the wafer from the vapour and join the two n regions underneath pellets E and B together. The assembly

is now cooled and during recrystallisation a layer of p-type germanium forms under pellet E. This is because the trivalent element present in pellet E is more soluble in recrystallised germanium than the pentavalent element. The recrystallised layer under pellet B is richly doped with pentavalent impurities and is therefore indicated as N^+ .

The thickness of the diffused base region can be limited to only a few micrometres and this results in high frequency characteristics which are far superior to those of an ordinary alloy transistor. The high frequency characteristics are also improved because the impurities in the base layer are graduated between emitter and collector and this gradient produces an accelerating field. The maximum useful frequency obtainable with mass produced alloy-junction types is about 1MHz. Alloy-diffused types can be used up to about 800MHz.

Silicon-Planar Transistors

The development of the planar technique has enabled the useful working frequency of mass produced transistors to be extended well above 1GHz. It also enables thousands of transistors or diodes to be made together on a thin slice of silicon about 5cm in diameter. The method of manufacture is illustrated in fig. 29. The word 'planar' indicates that the electrodes can be brought out to the same plane.

A polished and etched slice of n-type silicon about 5cm in diameter and 0.3mm thick (i) is placed in a furnace of temperature 1200°C for several hours and steam is passed over it. This causes the formation of a thin layer of oxide on the exposed surface (ii). Windows are then cut in the oxide layer. There are up to 3000 windows on the slice but in fig. 29(iii) only one transistor is shown. The windows are cut by a photolithographic process involving the use of photographic negatives called 'photo-masks'. A trivalent impurity is then diffused through the windows resulting in the formation of a plane of p-type material which will be the base, as shown in (iv). A new layer of oxide is then formed, another window cut and the emitter plane diffused into the base, fig. 29(v). The whole of the top surface of the slice is again oxidised and windows cut for access to the electrodes. Then a thin layer of metal is deposited on the top of the slice and the areas not required for electrode connections are etched away. The slice is broken up into individual transistor dice which are encapsulated. Each die is bonded to a metal header which acts as the collector connection and the base and emitter wires are welded on. The finished device is illustrated in fig. 29(vi).

Planar devices are extremely reliable. Their surface is covered by a protective layer of silicon oxide which prevents the ingress of dirt or moisture which would spoil their long term specifications. Production tolerances can be controlled to a fraction of a micrometre and working frequencies well above 1GHz are possible.

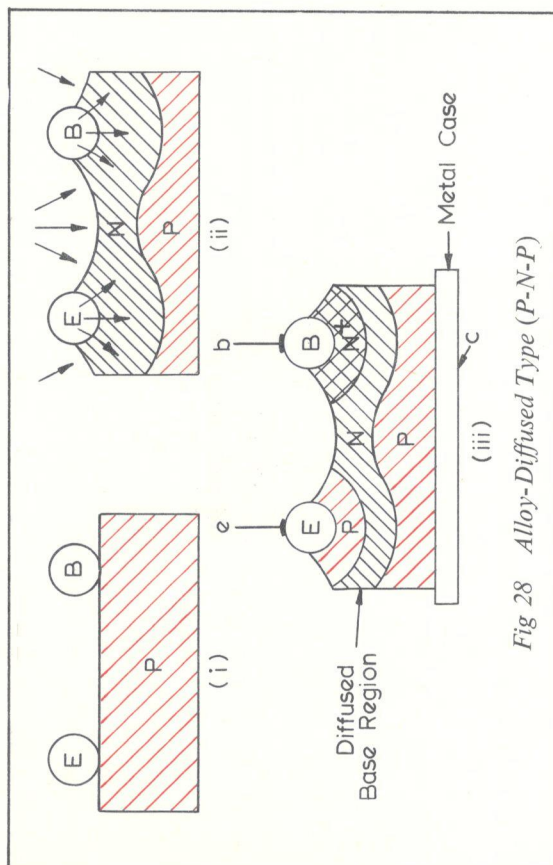


Fig 28 Alloy-Diffused Type (P-N-P)

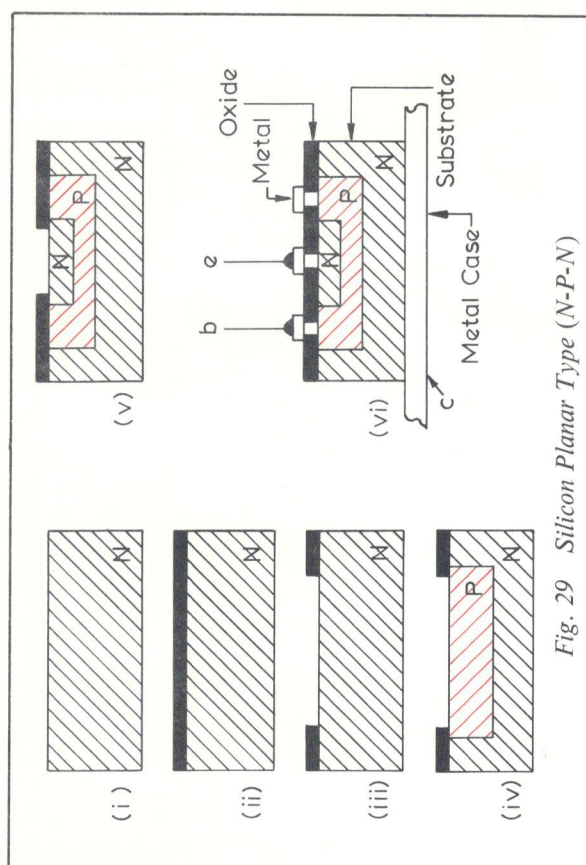


Fig. 29 Silicon Planar Type (N-P-N)

Planar Epitaxial Transistors

In practice very few ordinary planar transistors are made: most modern transistors have the further refinement of an additional plane of n-type silicon called the 'epitaxial' layer. (The word 'epitaxial' is derived from a combination of the Greek words 'epi' meaning 'upon' and 'taxos' meaning 'arranged'). A planar epitaxial transistor is illustrated in fig. 30.

The n^+ silicon slice acts simply as a low-resistance foundation (called the 'substrate'). The epitaxial layer is a crystal formation grown on the substrate in a special reactor. The base and emitter planes are diffused into the epitaxial layer by the method illustrated in fig. 29. The epitaxial layer makes possible two normally conflicting requirements. The collector resistivity must be high to obtain a high breakdown voltage but at the same time the overall resistance of the collector must be as low as possible to obtain a low saturation voltage. A compromise is achieved by using a very high resistivity collector material but keeping it very thin. In epitaxial transistors the collector plane may be made as narrow as desired without weakening the structure since the mechanical stress is borne by the substrate.

The Point Contact Diode

The above methods of fabrication also apply to junction diodes. Fig. 31 illustrates the point contact construction once used for transistors but now employed only for some diodes. Several different explanations have been put forward for the theory of operation of point contact devices. Perhaps the simplest is as follows. It is thought that the carriers in the piece of semiconductor tend to congregate near the point contact. This results in a charged area near the contact. Thus there is a virtual battery just as there is in the junction diode and the device can be used as a rectifier.

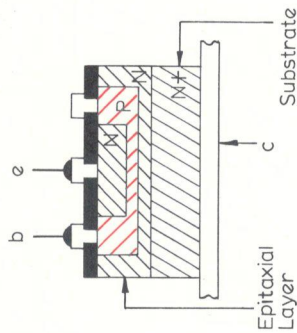


Fig. 30 Planar-Epitaxial Type

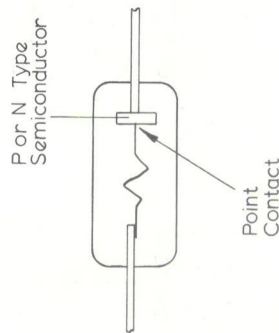


Fig. 31 Point-Contact Diode

SECTION 5 — TRANSISTOR CHARACTERISTICS AND PARAMETERS

Output Characteristics

Many characteristics and parameters are included in manufacturers' data sheets and here we shall consider only the basic ones. The characteristics given here as examples are those of the BC107. The BC107 is a modern silicon planar epitaxial device.

The graphs in figures 32, 33, 34 and 35 apply to the common emitter mode of connection. The graphs of collector current against collector voltage are called 'output characteristics'. These are usually given for constant values of I_B (fig. 32) and for constant values of V_{BE} (fig. 33). In fig. 32 two sets of graphs are given—fig. 32(a) is for low values of I_C and fig. 32(b) is for high values of I_C . The data is provided in this manner to give the circuit designer adequate information for a wide range of amplification levels. A very important feature of the curves in fig. 32 is that the characteristics tend to become almost parallel to the V_{CE} axis, indicating a high value of output resistance (due to the reverse biased base-collector junction). The output resistance is numerically equal to the reciprocal of the slope of the characteristic, the value decreases as I_C increases. It should be noted that the voltage V_{CE} is that between collector and emitter which will be less than the collector supply voltage when a load is added.

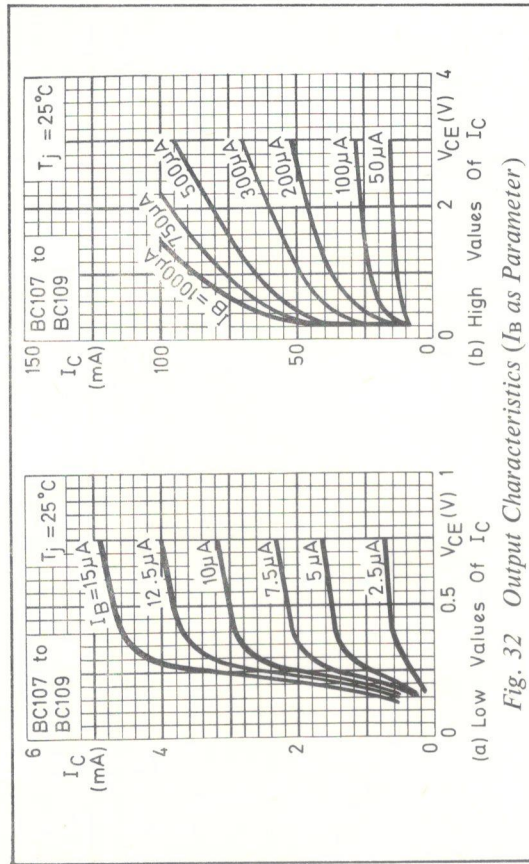


Fig. 32 Output Characteristics (I_B as Parameter)

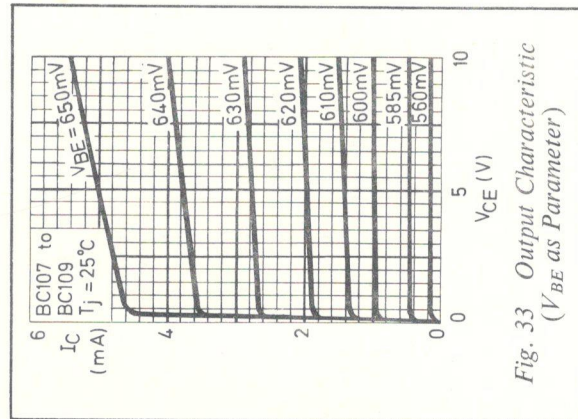


Fig. 33 Output Characteristic (V_{BE} as Parameter)

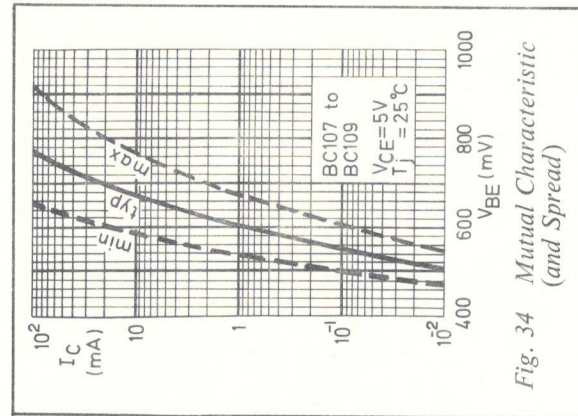


Fig. 34 Mutual Characteristic (and Spread)

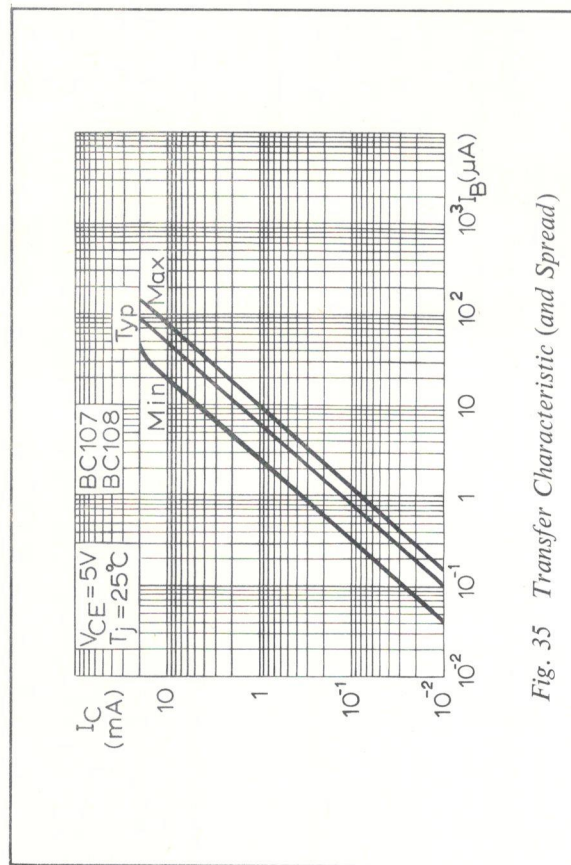


Fig. 35 Transfer Characteristic (and Spread)