A Quad CMOS Single-Supply Op Amp with Rail-to-Rail Output Swing

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Abstract—**The realization of a commercially viable, general-purpose quad CMOS amplifier will be presented along with discussions of the trade-offs involved in such a design. The amplifier features an output swing that extends to either supply rail. Together with an input common-mode range that includes ground, the device is especially well suited for single-supply operation and is fully specified for operation from 5 to 15 V over a temperature range of −55 to +125°C. Unlike earlier designs that sacrificed performance in the areas of input offset voltage, offset voltage drift, input noise voltage, voltage gain, and load driving capability, this implementation offers performance that equals or exceeds that of popular general-purpose quads of bipolar or BI-FET[1] construction. On a 5-V supply the typical V_{os} is 1 mV, V_{os} drift is 1.3 μV/°C, 1-kHz noise is 36 nV/√Hz, and gain is one million into a 600-Ω load. This device achieves its performance through both circuit design and layout techniques as opposed to special analog CMOS processing, thus lending itself to use on system chips built with the latest digital CMOS technology.**

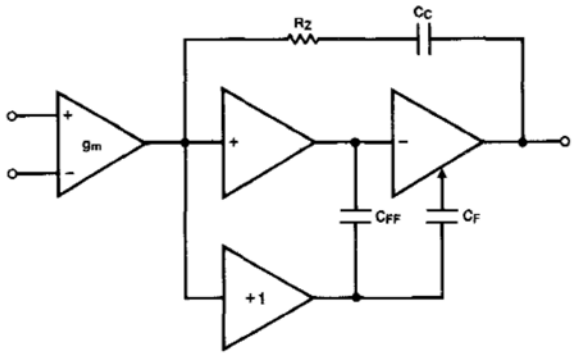

Fig. 1. Circuit topology of the amplifier.

I. Introduction

ALTHOUGH special-purpose CMOS amplifiers are an accepted part of mixed analog/digital chips where their ability to be integrated outweighs their existing weaknesses, penetration into stand-alone applications has been limited to niches such as low voltage, low power, and chopper stabilization. Unfortunately, shortcomings in the input stage relating to input offset voltage, drift and noise, shortcomings in the output stage in driving realistic loads, and latch-up sensitivity have prevented CMOS from making a strong contribution to the mainstream amplifier arena. This paper will describe a new CMOS amplifier design with overall performance on a +5-V supply that is equal to or better than most commercially available bipolar, BI-FET, or CMOS quad amplifiers. It is significant that this has been achieved on a conventional 4-μm, double-polysilicon, P-well process optimized for digital chips. This ability to share a common process with advanced digital CMOS circuits has important ramifications in realizing the large mixed analog/digital chips of the future that are the dream of the system designer.

II. Amplifier Topology

The amplifier topology chosen (Fig. 1) departs somewhat from the convention for general-purpose operational amplifiers in that the traditional unity-gain buffer is absent and the output is taken instead directly from the output of the integrator. Designing the buffer would not have been straightforward due to requirements for a stable stage with a gain of between one and two and an output that swings rail to rail. This remains a viable approach. However, eliminating the buffer has the advantage of simplicity and potential power savings, but places greater demands upon the integrator to deliver power, high gain, and rail-to-rail swing, to withstand shorts to either rail, and to remain stable in the presence of a wide range of loads. As a result of these demands, the integrator is a compound affair with an embedded gain stage that is doubly fed forward (via C_F and C_{FF}) by a dedicated unity-gain compensation driver. In addition, the output portion of the integrator is a robust push–pull configuration. While sinking current the whole amplifier path consists of three gain stages with one stage fed forward, whereas while sourcing the path contains four gain stages with two fed forward.

III. The Input Stage

The input stage (Fig. 2) is a conventional configuration that has been very carefully optimized for best performance. The physical layout of this circuit block has as much to do with good performance as does the actual circuit design. The most critical elements are the input devices $M1$ and $M2$, and considerable thought went into their choice, geometry, and placement on the die.

Noise measurements on test structures revealed that the Native p-channels ($V_T = -1.5$ V) were the quietest of the four MOSFET types available on the process. The second quietest device is the Native n-channel ($V_T = 0.7$ V) followed in order by the implant adjusted p-channel ($V_T =$

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[1]BI-FET is a trademark of National Semiconductor Corporation.

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