TRANSPARENT V-I PROTECTION IN AUDIO POWER AMPLIFIERS.

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Introduction.

The desirability or lack thereof, of over-voltage and over-current protection for power semiconductors in audio power amplifiers remains a point of contention in the field[1]. For example, Nelson Pass[2] appears to recommend multiple-transistor complementary output stages, as mandated by class-A operation, to circumvent the need for V-I protection of bipolar devices, while Rod Elliot[3] suggests that V-I limiter's can be dispensed with altogether by adopting e-MOSFETs.

These views appear to be rather more widely accepted than they should, and constitute a charter for near heroic unreliability in amplifiers so designed. The zener diode-clamping of gate-source voltage for e-MOSFETs is thought by some[4,5], to be all that is required in regard to protection. While the zener diodes are mandatory, (ideally with $10V < V_{zener} < 20V$, to prevent premature clamping), they only serve to protect the e-MOSFET gate oxide insulation from over-voltage destruction[6], and do nothing whatever to protect the device from accidental short circuits, and forbidden voltage-current combinations that may occur when the amplifier is called upon to drive reactive loads.

The positive temperature coefficient of on-resistance[7], (and therefore *negative* temperature coefficient of drain current), enjoyed by e-MOSFETs eliminates the secondary breakdown phenomenon which is the bane of bipolar transistors, but does not constitute licence for wilful violation of power dissipation limits in linear, audio-frequency applications. This is in contrast to ultrasonic switching usage, where e-MOSFET dissipation bounds can be blissfully ignored, and adherence to drain current, and drain-source voltage limits will suffice.

All output stage semiconductors used in complementary, or quasi-complementary, (full or half bridge), linear audio power amplifiers, without exception, require V-I protection for reliable operation. However, such circuitry must be carefully designed to prevent premature activation during normal amplifier operation.

Single slope, linear foldback limiting.

Many low to medium-power, (sub-100W), commercial audio amplifiers incorporate a single slope, linear foldback, voltage-current protection circuit, (fig. 1), attributed to S.G.S. Fairchild Ltd. by Dr A.R. Bailey[8]. In practice the complimentary output transistors, T_{o1} and T_{o2}, may each consist of a compound arrangement of at least two transistors in series. The collector-emitter voltage, Vce, across T_{o1} is sensed by R_1, and R_3, while the output current, in the guise of a voltage developed across emitter resistor Re, is simultaneously monitored by R_3, and R_2. The voltages are thus summed algebraically at the base of the protection transistor, T_{p1}, which is driven into conduction, shunting voltage drive to T_{o1}, in the event of an over-voltage, over-current, or simultaneous occurrence of both conditions in the output device.

The series resistor, Rs, (typically $100R \le R_s \le 2K2$), expedites this process by limiting the current required by T_{p1} to shunt voltage drive to T_{o1}. The freewheeling diode, D_F, protects the output device from excessive base-emitter reverse bias[9], due to over-rail voltage spikes generated by inductive loads, while D_P performs the same function for the small-signal protection transistor, by preventing its base-collector junction from being forward biased[5].

If the output approaches the negative supply rail while driving a sufficiently low impedance, the current sunk by T_{o2} generates an appreciable voltage drop across its emitter resistor, placing the output at a significantly higher potential than the common input to the complementary output stage. Thus transistor T_{o1} is reverse biased, and T_{p1}'s base-collector junction, in the absence of its collector diode D_P, would be forward biased, resulting in current flow from emitter to collector.

Diode D_P, (preferably a schottky device for its relatively low forward voltage drop), prevents this form of spurious, inverse-active mode limiter activation by decoupling T_{p1}'s collector as T_{o1}'s base-emitter junction is reverse biased. The potential at T_{o1}'s emitter is then equal to the output voltage since, contrary to Duncan[10], T_{o1} is non-conducting and no current, except negligible leakage, flows through its emitter resistor. By symmetry, the explanation above also applies to the negative half of the circuit.

A small-value capacitor is sometimes connected across the base-collector junction of each protection transistor[1], with a view to eliminating benign parasitic oscillation[11] that may occur sporadically in the network during the limiting process. These capacitors appear in parallel at A.C., and are entirely unsatisfactory, as they create an ill-defined and therefore undesirable feedfoward path around the output stage, shunting it out of the global feedback loop at high audio frequencies, precisely where the amplifier is most vulnerable with respect to non-linearity. Such vulnerability is due to a necessarily diminished feedback factor at high audio frequencies in the interest of Nyquist stability. Connecting the capacitor across the base-emitter junction of each protection transistor is the preferred solution. A series base resistor, (of the order of 2K2~4K7), for each protection transistor is also recommended.

The single pole low-pass filter comprised of the series resistor and the shunt capacitor prevents activation of the protection transistor at ultra-sonic frequencies where such protection is unnecessary. For typical values, the source impedance of the protection circuit referred to the base of the protection BJT can be considered negligible compared to the value of the base resistor. A low-pass time constant no greater than $40\mu s$ is recommended here, as the filter is required to partially damp the oscillation and not completely eliminate it. This is because the oscillation is intrinsic to the circuits operation.

If for instance, the output is required to swing positive In the presence of a persistent overload condition, such as a continuous short-circuit to ground or opposite supply rail, protection transistor T_{p1} is driven forward-active, cutting off output transistor T_{o1}. The fault condition is therefore removed with respect to T_{o1}, and protection transistor T_{p1} is summarily disabled. This in turn causes the instantaneous recurrence of the overload condition, and attendant reactivation of T_{p1}. The on-off action of the protection transistor in these circumstances appears as persistent local high frequency oscillation, which of itself has nothing to do with the stability of the amplifiers global feedback loop.

The inclusion of a series base resistor for each protection BJT also ameliorates anomalous oscillation during gross overload, which would otherwise result from the heavy non-linear loading of the protection transistor on its driving circuit as it attempts to exceed the transistor's activation threshold, $(V_{be} \approx 0V6)$. For brevity diodes D_F, D_P, the base-emitter shunt capacitor, and series base resistor are omitted in all subsequent figures.

The resistor values for the arrangement in figure 1 are obtained by drawing the desired protection locus onto a linear scale graph of the output transistor's safe operating area. One of the three resistors, (usually R_3), is assigned an arbitrary value, (typically $100R \leq R_3 \leq 1K$), and the two remaining resistors calculated from simultaneous equations developed from two convenient points on the protection locus.

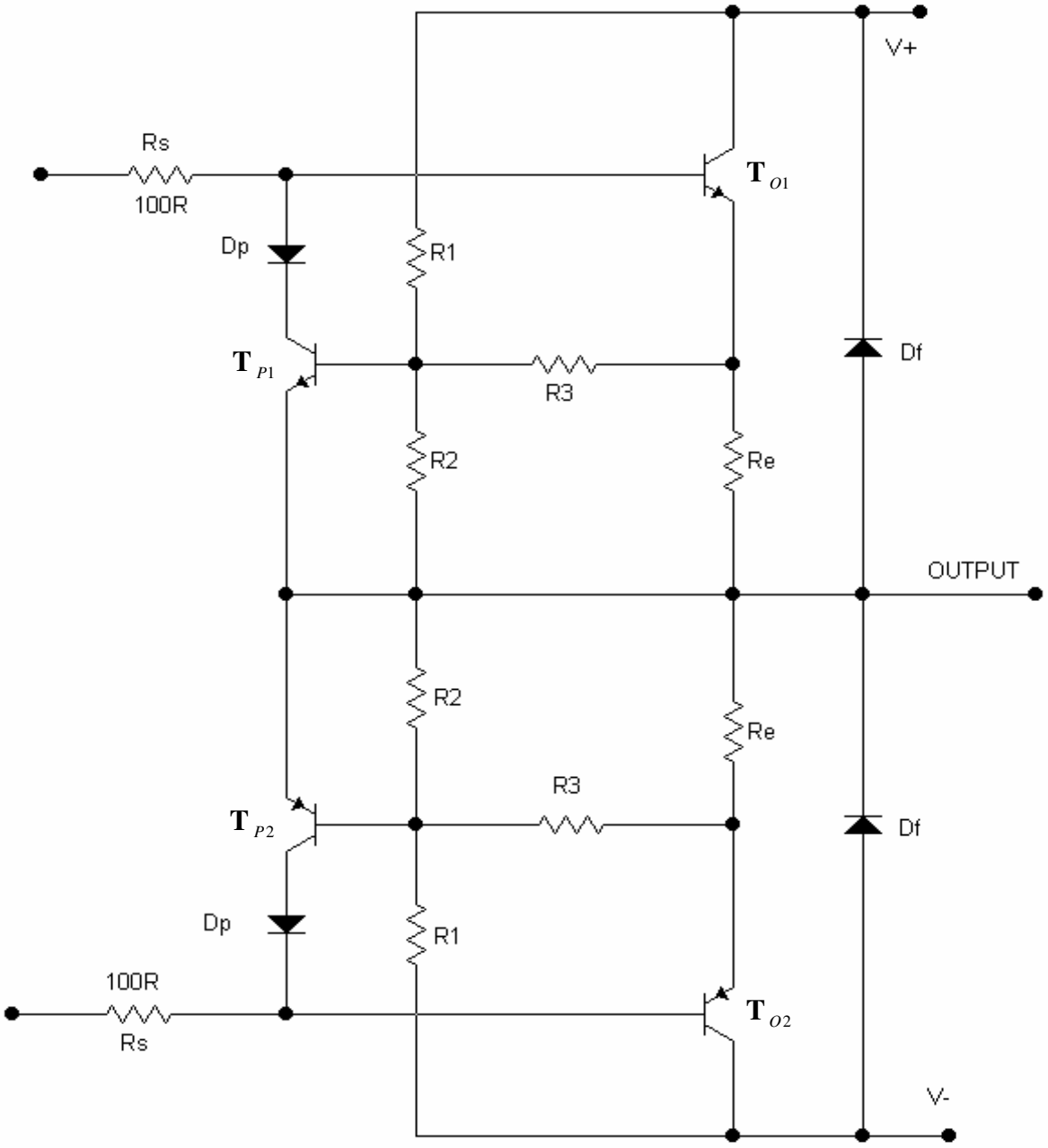

Fig. 1. Single slope, linear foldback protection circuit applied to a complementary emitter follower.

This arrangement requires that the linear protection locus intersect the SOA's Vce axis at a value greater than the sum of the moduli of the amplifiers voltage supplies, otherwise T_{p1} turns on under normal loading when the output swings negative, even with the output open-circuit. Similarly T_{p2} would be activated under normal output loading when the output swings positive. This effectively short-circuits the small signal circuit preceding the output stage directly to the output, causing gross and very audible distortion. Failure to adhere to the above condition appears to have caused some designers to erroneously abandon electronic SOA protection of any form altogether[1,12].

This requirement however, constitutes a significant limitation with regard to efficient utilisation of the comparatively large SOA in the low-Vce region of the graph, especially at high supply-rail voltages where, in the case of bipolar transistors, secondary-breakdown severely curtails flexibility in optimal placement of the protection locus. This is graphically illustrated in figure 2, for an amplifier with ± 40V supply rails, using Motorola's excellent[13] 200W, MJL3281A-MJL1302A complementary power transistors.

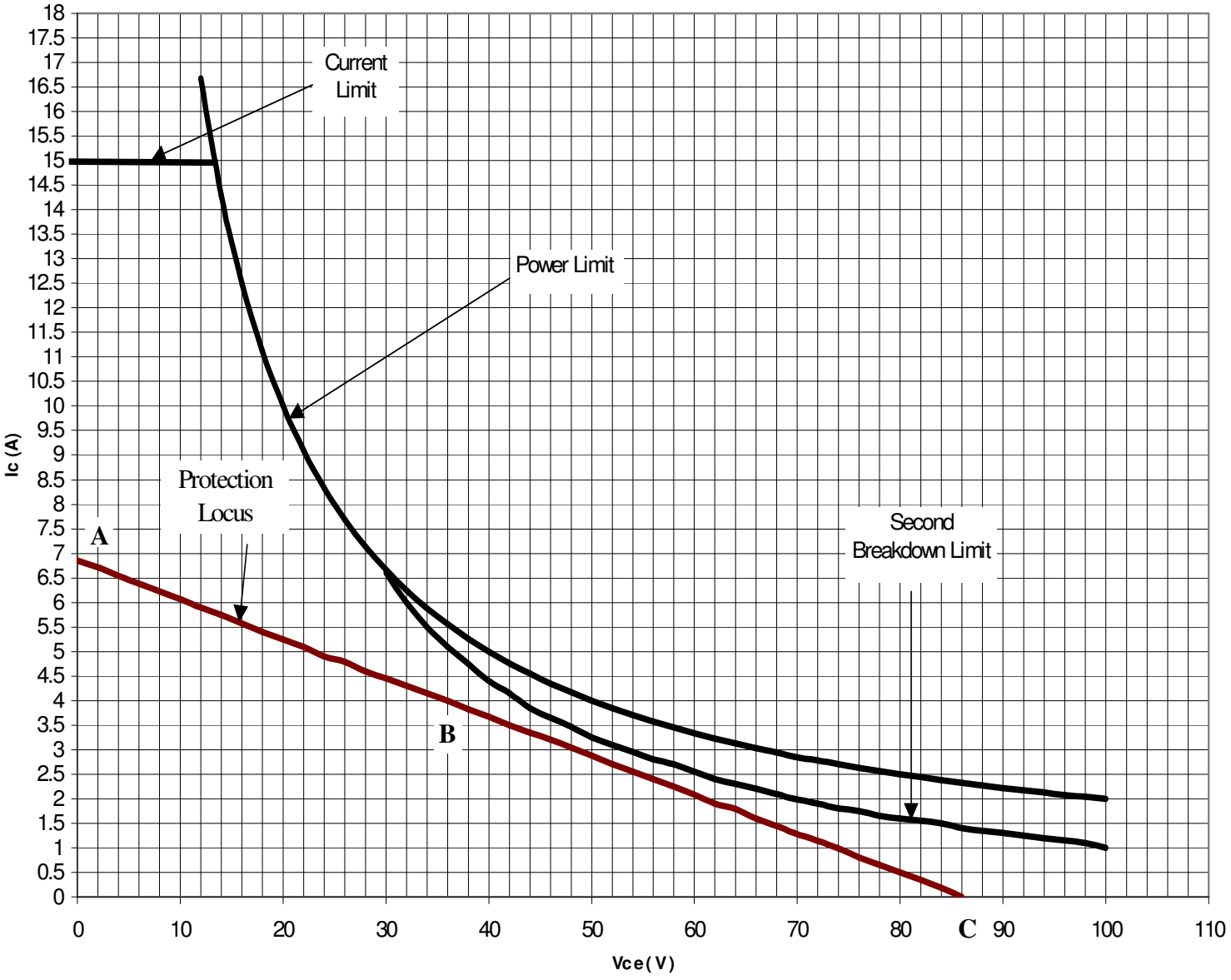

Fig. 2. MJL3281A safe operating area with single slope, linear foldback protection locus drawn to intersect the Vce-axis at a value greater than $2|V_{cc}|$, to prevent premature limiting.

Only the positive half, (fig. 3), of the circuit in figure 1 need be used to calculate the required component values. Ideal devices are assumed, with infinite input impedance, zero saturation voltage, and zero ohmic resistance, -the error thus accrued is negligible in practice, provided high current-gain, $(\beta \geq 100)$, small-signal transistors are used. Let V_{be}=0V6, R_3=220R, and Re=0R22. Taking two arbitrary points A and B on the locus such that, $\{0 \leq V_{ce} < (2|V_{cc}| = 80V)\}$, where for point A, Ic=6.85A; Vce=0V, and for point B, Ic=4A; Vce=36V, it follows from figure 3:

$$0.6 = \frac{1.507R_2}{R_2 + R_1 220/(R_1 + 220)} \tag{1}$$

With reference to figure 4:

$$I_2 = I_1 + I_3 \tag{2}$$

$\Rightarrow$

$$0.6/R_2 = (40 - 3.72)/R_1 + (4 - 3.72)/R_3$$

$\Rightarrow$

$$0.6 = R_2(36.28/R_1 + 0.28/220) \tag{3}$$

Solving (1) and (3) simultaneously gives $R_1 \approx$ 12K4 and $R_2 \approx$ 143R0. To afford an acceptable degree of precision, it is recommended where necessary, that these values be made up from series, or parallel combinations of 1% resistors.

When the output swings to –40V, then 80V appears across R_1 in series with R_2 // R_3, to a good first approximation. Therefore the voltage present at the base of the protection transistor, T_p, is given by:

$$V_{be} \approx \frac{80(R_2 // R_3)}{(R_2 // R_3) + R_1} \approx 0V55$$

It follows therefore that subject to instantaneous collector current, i_c, being less than the maximum permissible collector current, $I_{C(MAX)}$, at $V_{ce} \approx 2|V_{cc}|$, spurious activation of T_p cannot occur. A general expression which allows the rapid verification of the compliance of any amplifier using single slope, linear foldback limiting may be developed:

$$\left|\frac{2V_{cc}(R_2 // R_3)}{\{(R_2 // R_3) + R_1\}}\right| < 0V6$$

$\Rightarrow$

$$\boxed{\left|\frac{2V_{cc}R_2R_3}{(R_2R_3 + R_1R_2 + R_1R_3)}\right| < 0V6} \tag{4}$$

Equation 4 is valid subject to the following condition:

$$i_C < I_{C(MAX)}\Big|_{V_{ce} \approx 2|V_{cc}|} \tag{5}$$

This condition is invariably fulfilled during normal operation, as no practical loudspeaker system would demand that the output transistor sustain $V_{ce} \approx 2|V_{cc}|$, while providing any appreciable current.

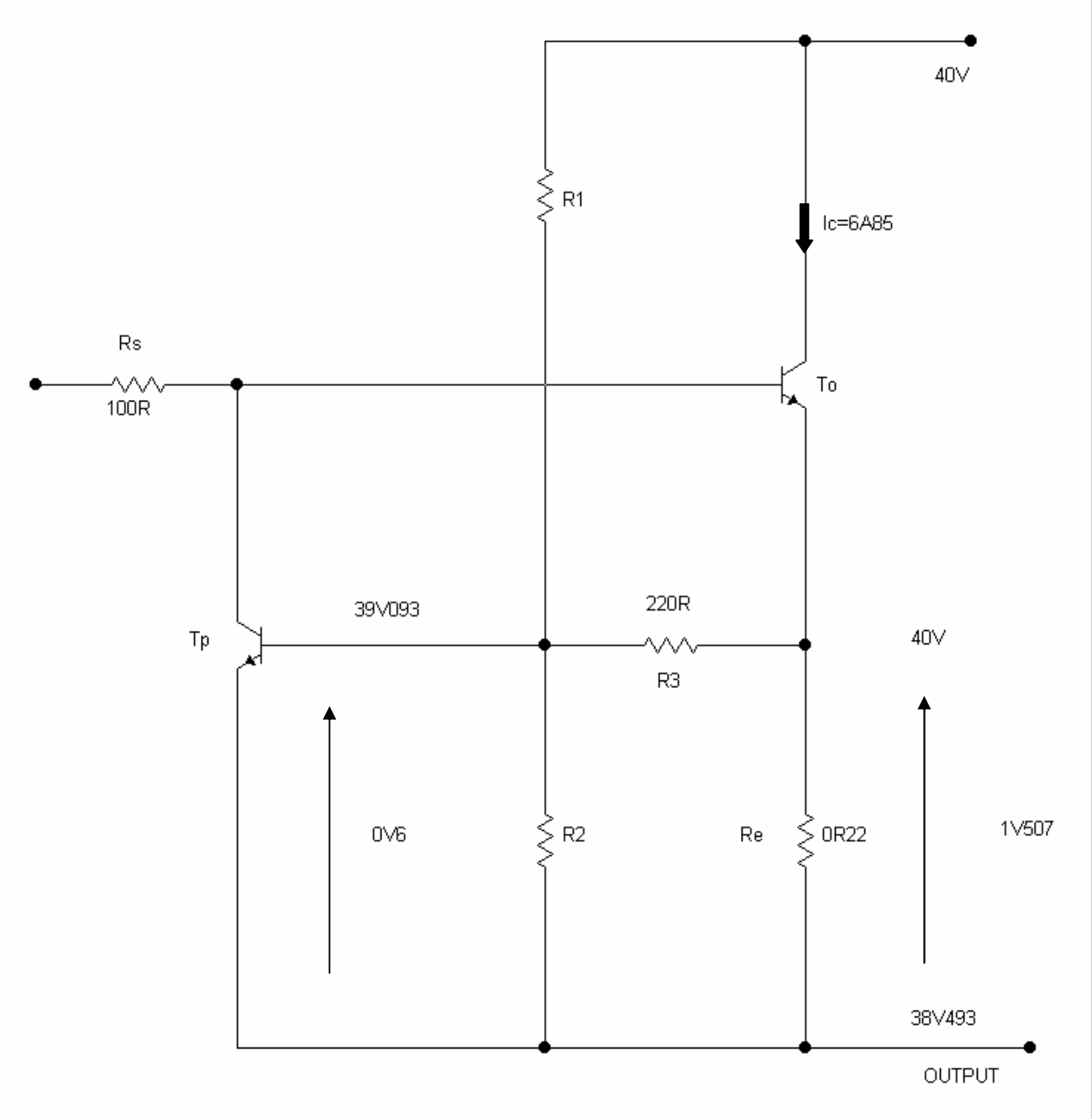

Fig. 3. Output conditions at point A on the protection locus in figure 2.

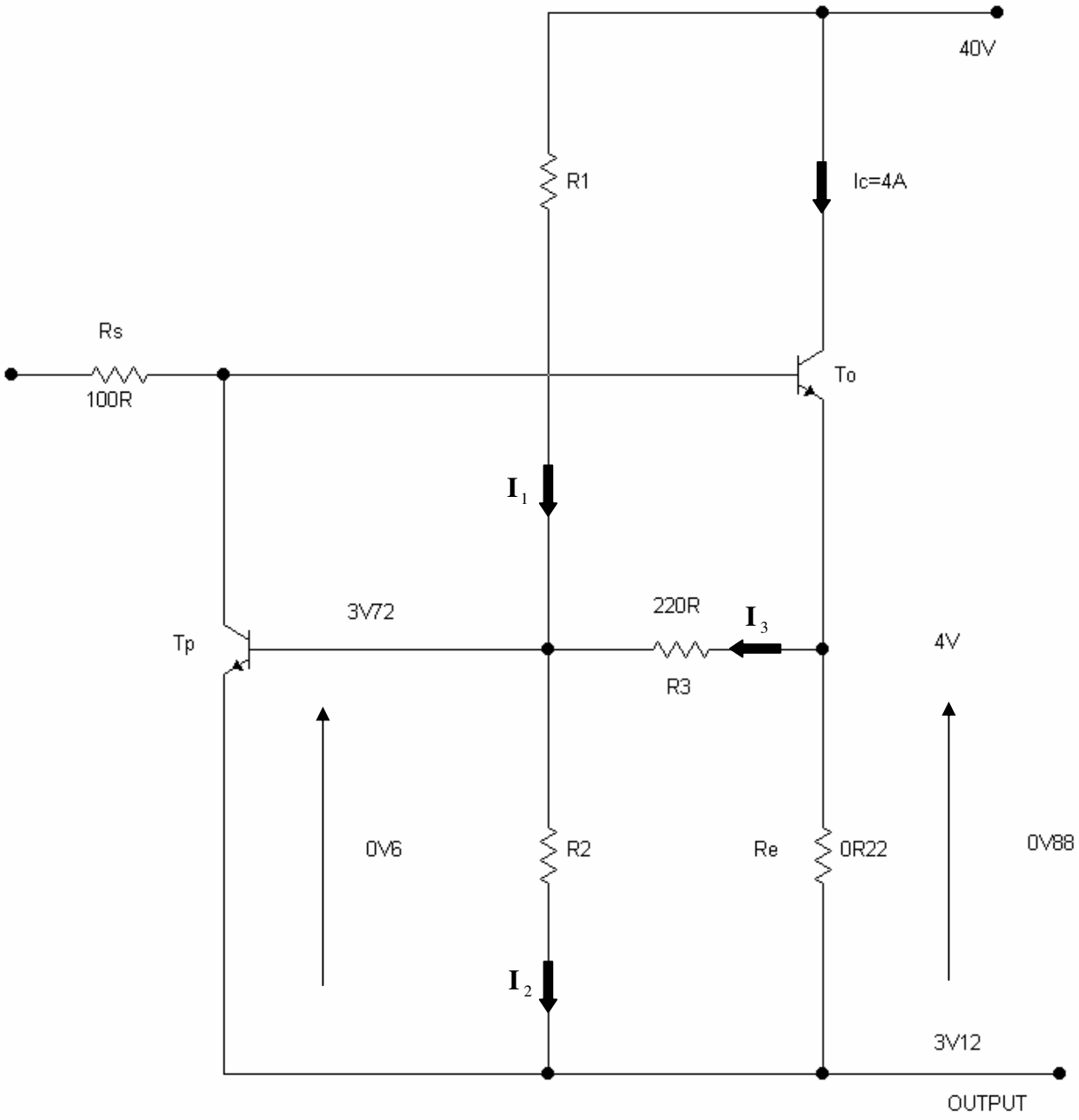

Fig. 4. Output conditions at point B on the protection locus in figure 2.

Figure 5 shows a common variation[10,13,14], on the single slope, linear foldback limiter of figure 1, with resistor R_2 excised, so that from equation 4:

$$\left|\frac{2V_{cc}R_3}{\{R_3+R_1+(R_1R_3/R_2)\}}\right|<0V6$$

Since $R_2 \to \infty$, then:

$$\left|\frac{2V_{cc}R_3}{(R_3+R_1)}\right|<0V6$$

The optimal protection locus for this network, (fig. 6), must be plotted so that calculated resistor values comply with the above condition. This scheme is atrociously inefficient, as for a nominal $V_{ce} \approx 0V$, and $R_e = 0R22$, resistors R_1 and R_3 are in parallel, and collector current I_c, is perforce prematurely limited to $\{I_c|_{V_{ce}\approx 0V} < (V_{be}/R_e \approx 2A7)\}$. A value of $R_e = 0R1$ gives a modest improvement, with $\{I_c|_{V_{ce}\approx 0V} < (V_{be}/R_e \approx 6A0)\}$. Clearly claims[13] of 'load-invariant' drive capability made for power amplifiers using this scheme are rather premature.

The protection locus is realized by deriving output stage conditions, (fig. 7), for a single arbitrary point B on the locus subject to $\{0 < V_{ce} < 2|V_{cc}|\}$. With $V_{cc} = 40V$, $R_e = 0R22$, $R_3 = 220R$, and noting that R_1, R_3 constitute a simple voltage divider:

$$R_1 \approx \frac{(40+39.4)}{(-39.4+39.78)/220R} \approx 46K$$

This unwarranted dependence on the value of R_e is unacceptable, as in some applications such as output stages comprised of paralleled, complementary e-MOSFET pairs, $(0R1 < R_e \le 1R0)$, may be required to ensure equable current sharing.

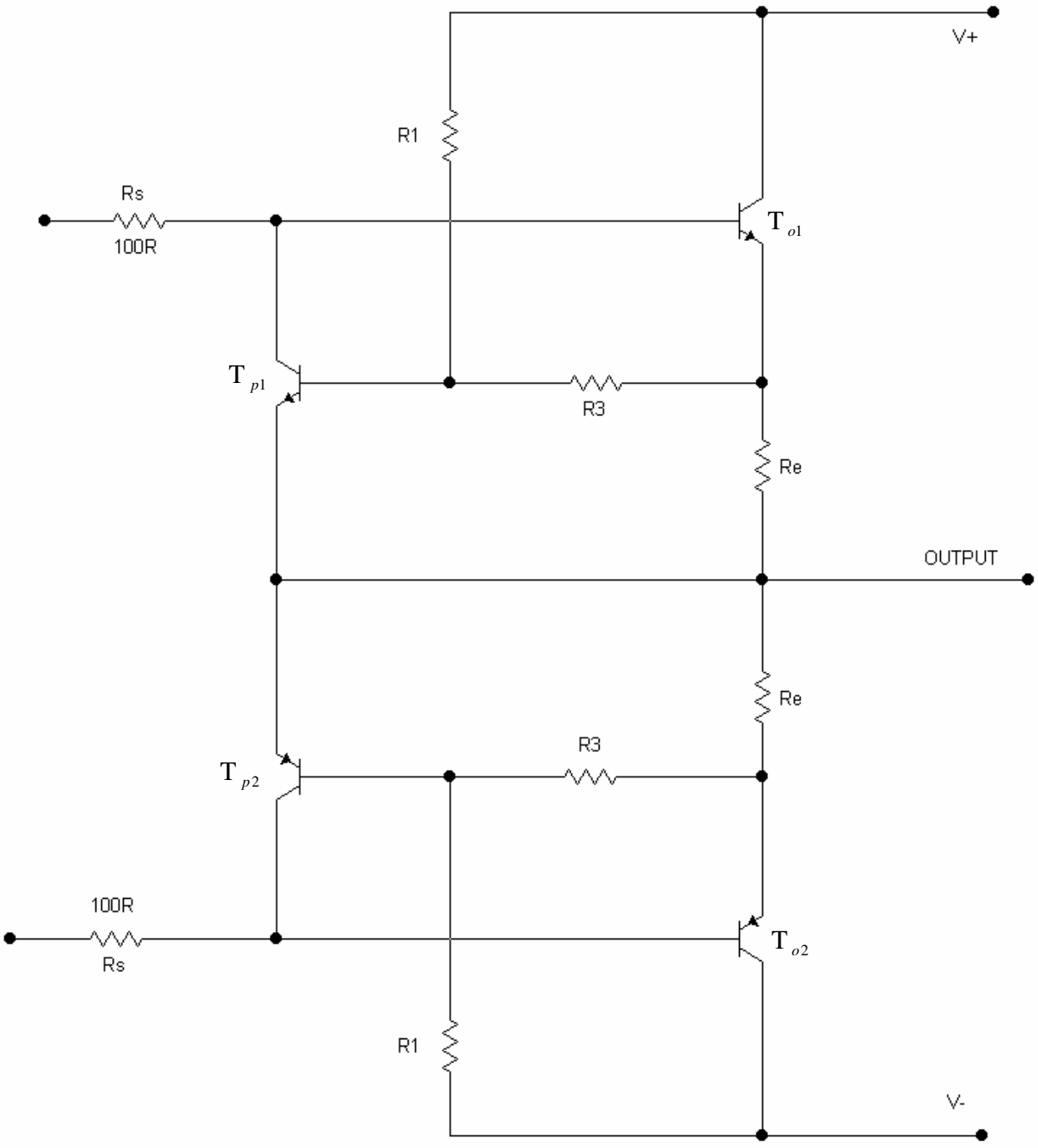

Fig. 5. Compromised single slope, linear foldback scheme resulting in grossly inefficient SOA utilisation.

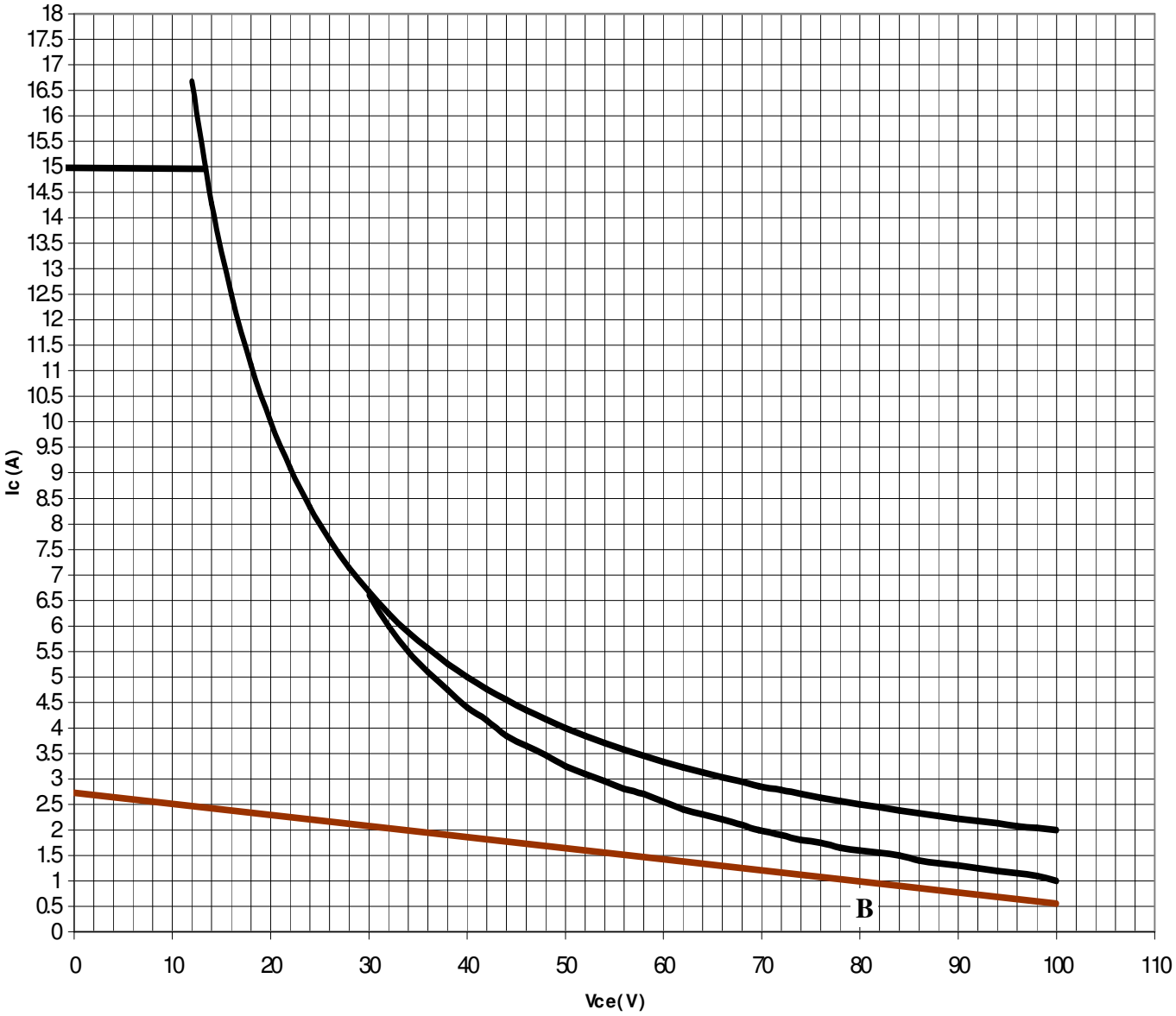

Fig. 6. Linear protection locus clearly shows inflexibility of scheme in figure 5.

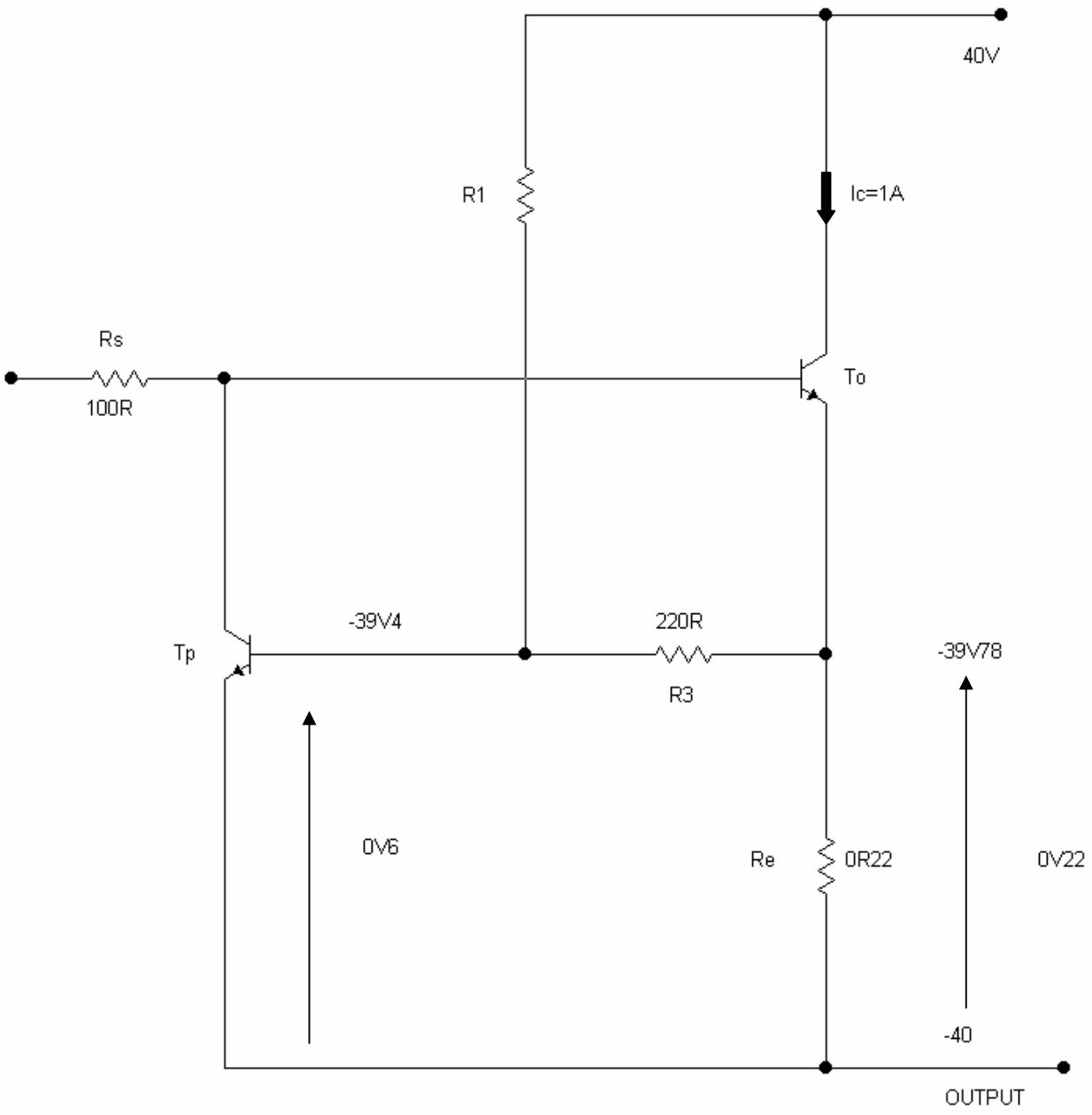

Fig. 7. Output conditions at point B on the protection locus in figure 6.

Driving reactive loads.

A clear appreciation of the nature of the amplifiers load is required to establish the bounds within which the V-I limiter must remain inactive. Figure 8 shows an ideal complementary emitter follower, (in Electronics workbench's excellent Multisim professional simulator[15]), used to drive a standard $(8\Omega\angle 0^0)$ test load to $\pm 40V$ supply rails.

The plots obtained in figure 9 show that the voltage v_{ce}, across T_{o1} is precisely 180^0 out of phase with the current, i_c, its required to source; the voltage across the device is a minimum when its collector current is at a maximum, and vice versa. Instantaneous power dissipation is merely the product of instantaneous device voltage and current. Peak transistor dissipation, $p_{d(\max)} \approx 50W$, occurs twice in T_{o1}'s conducting half-cycle, at half the peak load voltage, $(V_{out}/2 \approx V_{cc}/2)$, and half the peak load current, $i_{c(peak)}/2$.

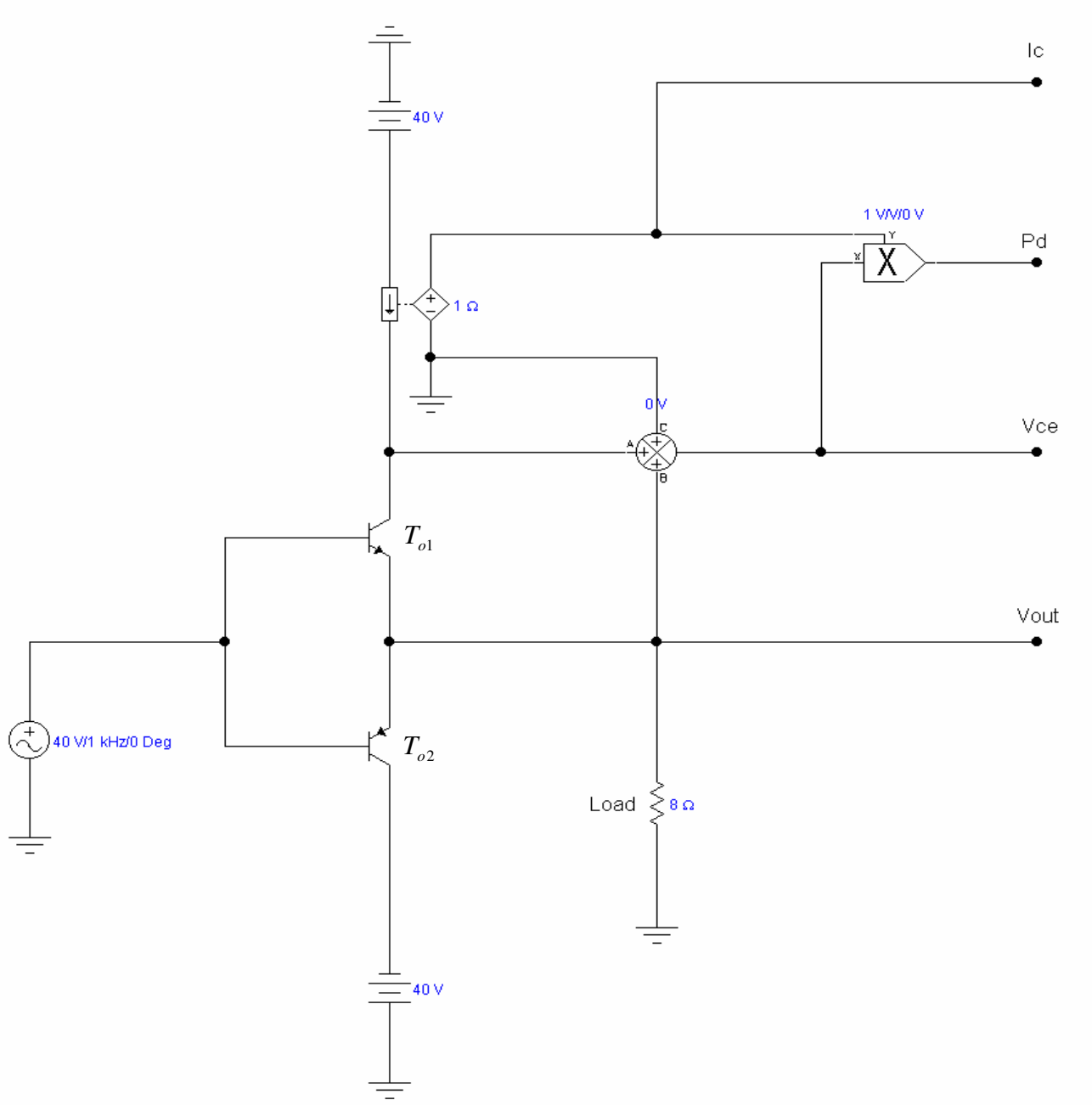

Fig. 8. Ideal emitter follower used to determine instantaneous collector current, Ic, collector-emitter voltage, Vce, and device dissipation, Pd.

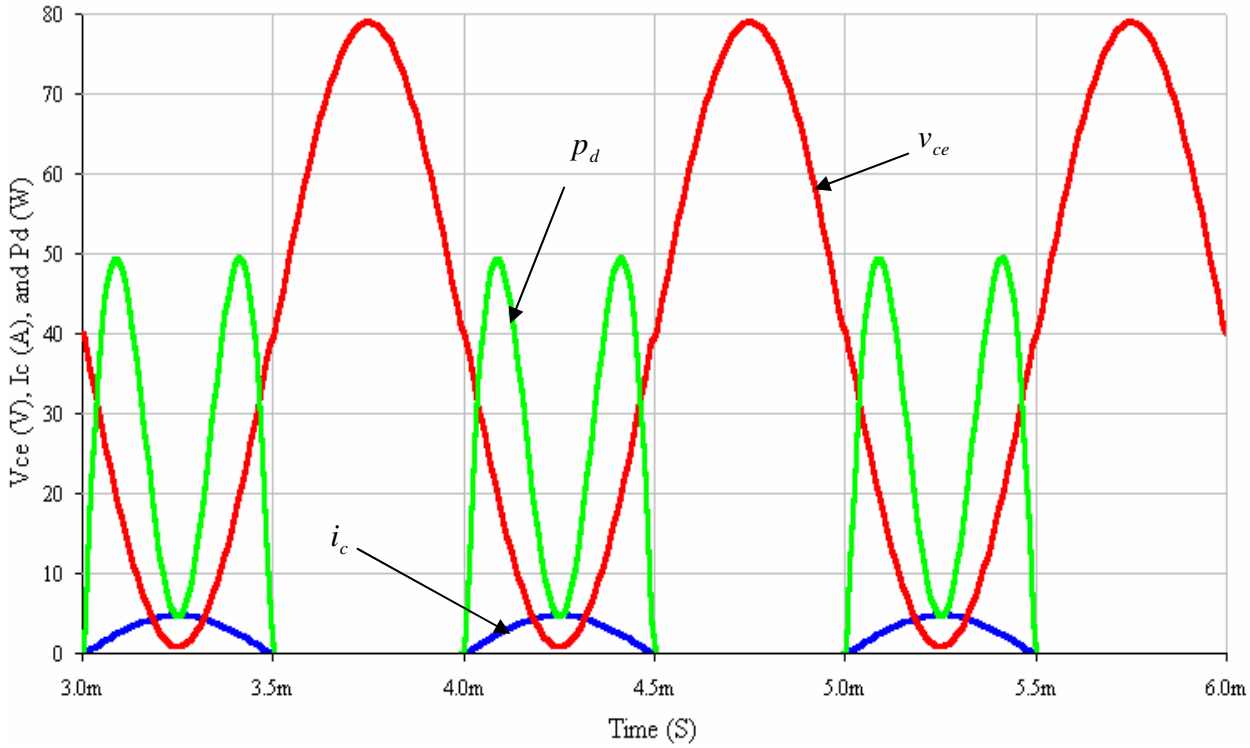

Fig. 9. Instantaneous Vce, Ic, and Pd in sourcing output transistor, driving 100W into $(8\Omega\angle 0^0)$.

As the $(8\Omega\angle 0^0)$ load line lies well below the linear protection locus in figure 10, (reproduced from fig. 2), it is clear that a single pair of MJL3281A-MJL1302A power transistors, operating from ± 40V rails will comfortably drive an 8Ω dummy load to clipping without V-I limiting. This however, will certainly not be the case with loudspeaker loads, which are invariably reactive[16,17]. An amplifier with 'high-fidelity' aspirations, intended to drive full-range, multiple-transducer loudspeaker systems, including electrostatics, should at least be capable of driving a $(4\Omega\angle \pm 60^0)$ impedance without V-I limiting.

A $(4\Omega\angle$-$60^0)$ impedance was devised by driving a 2Ω0 resistor in series with a 45μ9441 capacitor at 1Khz with the ideal complementary emitter follower in figure 8. The traces thus obtained, (fig 11), were used to plot the $(4\Omega\angle\pm 60^0)$ load line in figure 10. Peak transistor dissipation, $p_{d(\max)} \approx 352.93W$, occurs at $v_{ce} \approx 45.97V$, and $i_c \approx 7.68A$.

In other words, (fig. 12), because current leads voltage in a capacitive impedance, the npn transistor, T_{o1} in figure 8, is required to source≈7.68A when the output swings away from the negative supply rail to≈-5.97V. Similarly, the pnp device, T_{o2}, must sink≈7.68A when the output swings to +5.97V from +Vcc. Note that the crossover discontinuity in the output voltage characteristic, (fig. 12), now precedes zero crossing by 60^0, at $|V_{out}| \approx 35V$.

For a $(4\Omega\angle +60^0)$ inductive impedance, in which current lags voltage, the output conditions are reversed, with the load demanding 7.68A from T_{o1} when the output swings from the positive supply to -5.97V. Regardless of the nature of the load however, device voltage, v_{ce}, and load voltage, v_{out}, are always 180^0 out of phase, and being a voltage follower, the input voltage is always in phase with v_{out}.

The linear foldback protection locus of figure 10 only permits 3.1A at Vce=45.97V, therefore a minimum of three, (ideally four), output pairs are required to drive a notional $(4\Omega\angle\pm 60^0)$ loudspeaker system from ± 40V supply rails without intrusive limiter activation. On this basis and using other established techniques[11,18], including D.C. offset, and thermal overload protection, a reliable, low distortion, 100W into $(4\Omega\angle\pm 60^0)$ class-B amplifier may be constructed.

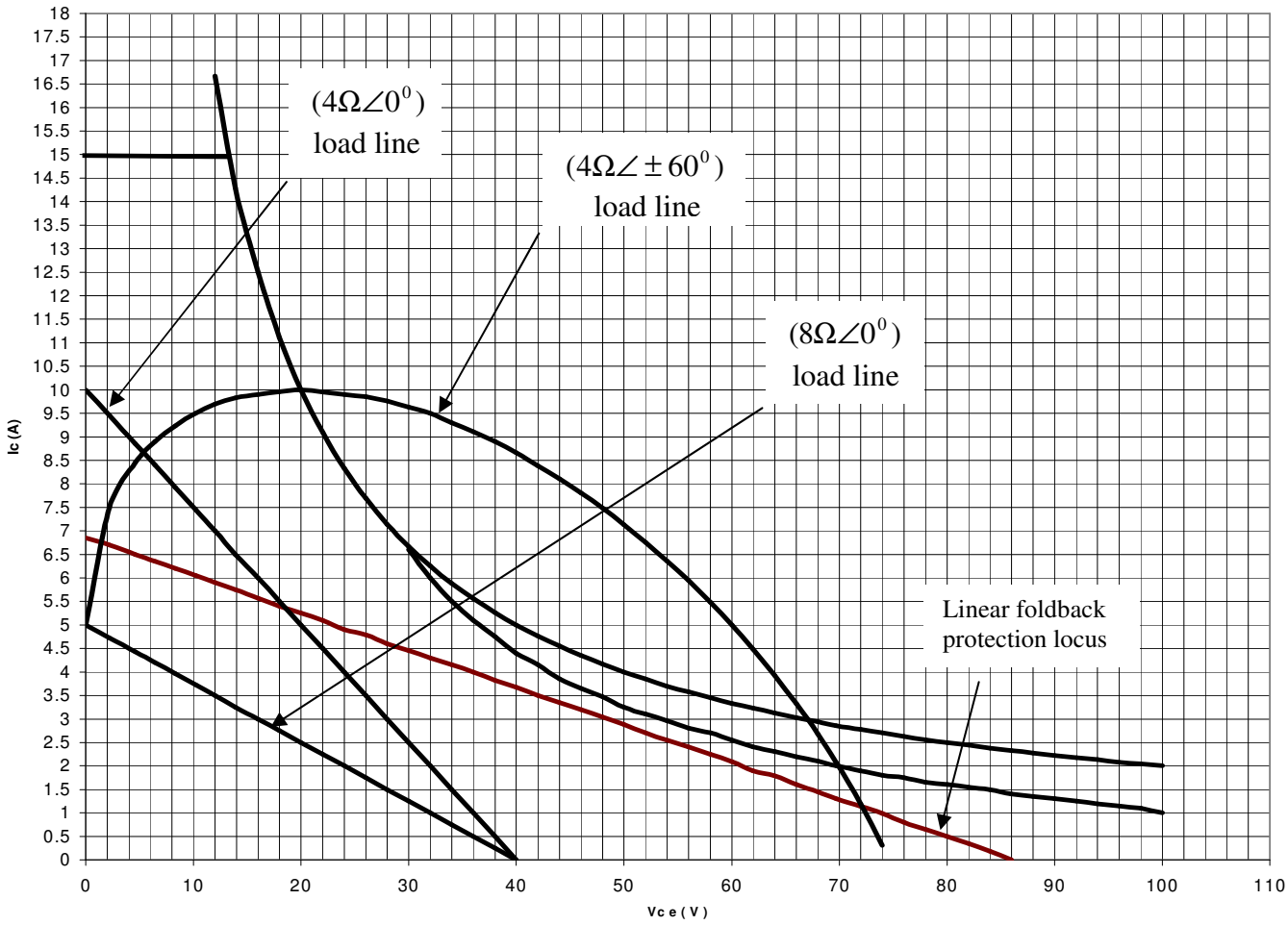

Fig. 10. Reactive load gives rise to an elliptical line, resulting in more than seven times greater peak device dissipation than for the $(8\Omega\angle 0^0)$ case.

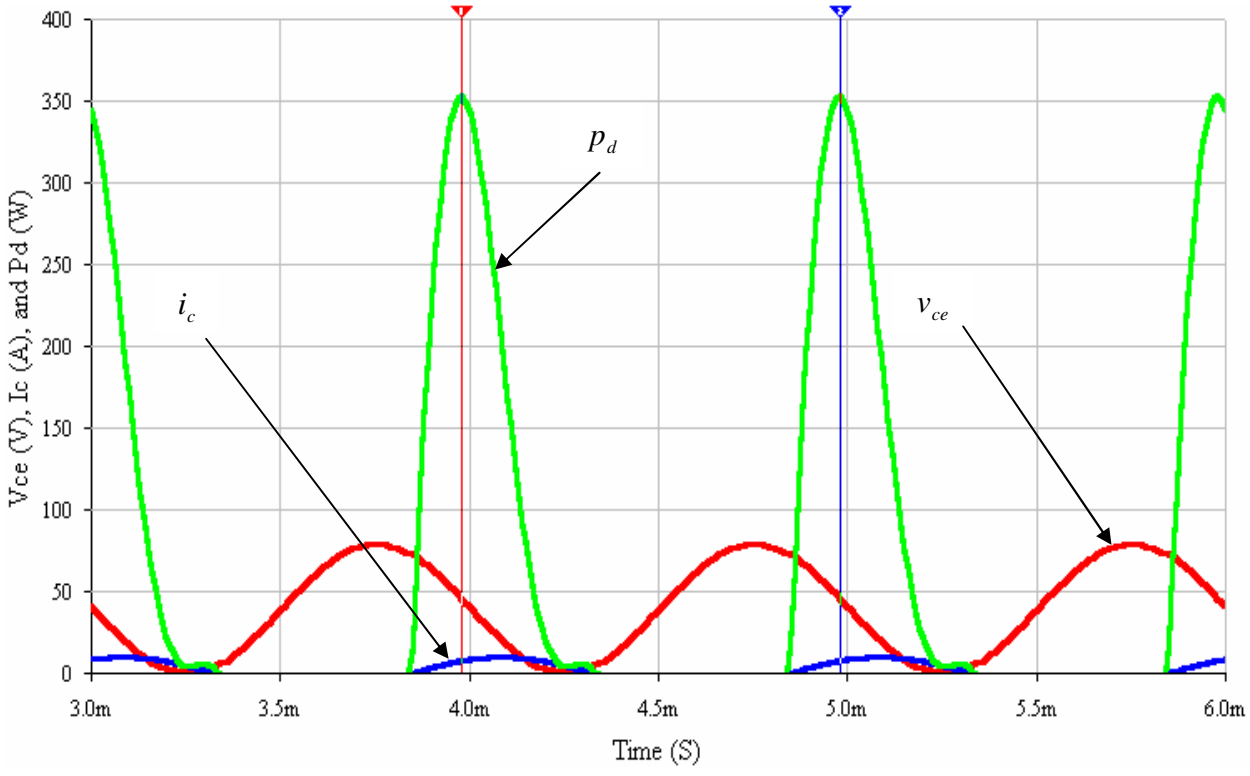

Fig. 11. Instantaneous Vce, Ic, and Pd in sourcing output transistor, driving 150W into $(4\Omega\angle -60^0)$.

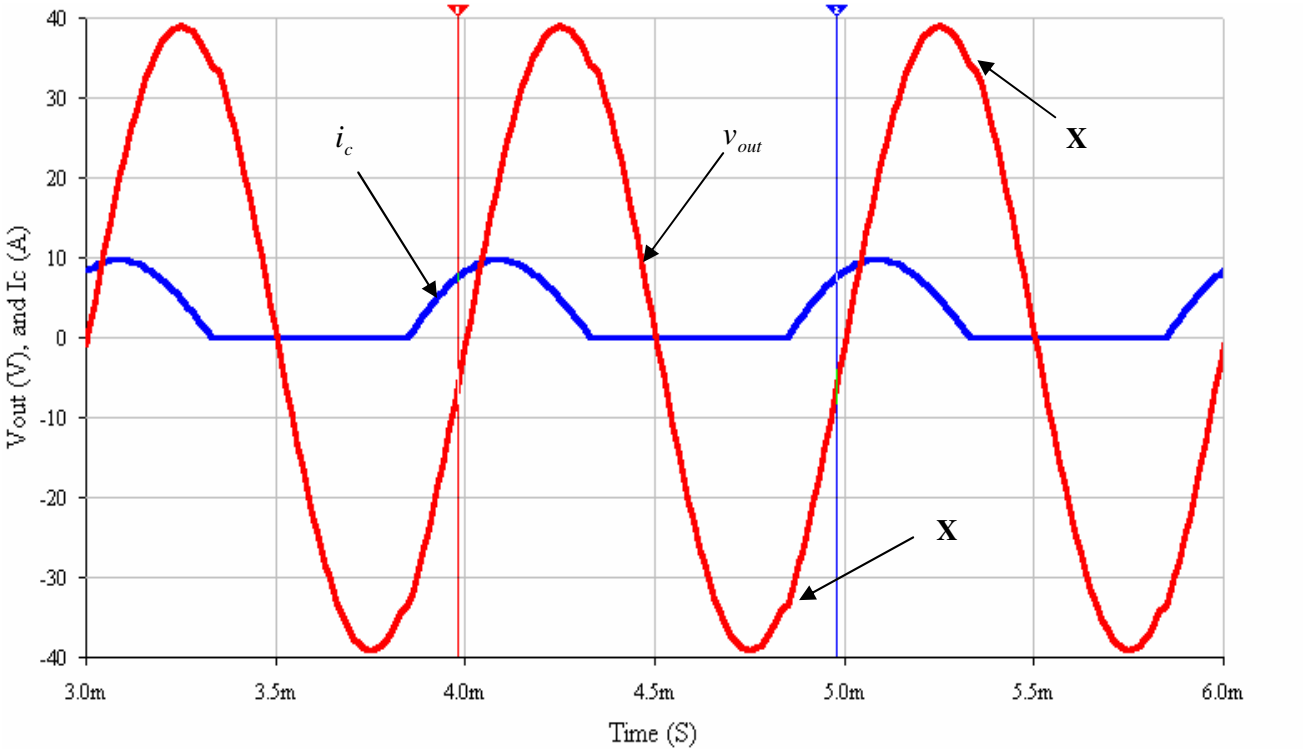

Fig.12. Transistor T_{o1} delivers 7.68A to the $(4\Omega\angle -60^0)$ load when output swings away from -Vcc to -5.97V. Note that the crossover discontinuity marked X precedes zero voltage crossing by 60^0.

As the cost of power transistors is significant, there is a compelling financial incentive to minimise the number of devices used by utilising the SOA as efficiently as possible. To this end it has been suggested[10] that ideally the protection locus should closely match the bounds of the S.O.A. This is unnecessary, as reactive load drive primarily requires that current delivery in the $|V_{cc}| \le V_{ce} < 2|V_{cc}|$ region be maximized without violating D.C safe operating limits. In general an optimally located, non-linear protection locus with no more than one breakpoint should suffice.

Single slope, single breakpoint non-linear foldback limiting.

Introducing a zero-gradient segment, (fig. 13), at some optimal point in the protection locus permits the enhancement of current delivery at the low-Vce end of the SOA, without significantly compromising available current at higher device voltages. The single slope, linear foldback 'protocol', (equation 4), is made redundant, as the protection locus does not cross the Vce-axis at any point. This scheme is briefly mentioned in reference [19], where it is dismissed in favour of the comparatively inferior single slope, linear foldback method.

The zero-slope segment, B-C, is realised by splitting R_2 in figure 1 into voltage divider, R_{2A} and R_{2B}, (fig. 14), and shunting R_3 with a fast recovery diode, D_1. The diode applies a constant voltage, $V_f \approx 0V6$, (to a first-order approximation), across R_3, for $\{64V \le V_{ce} < (2|V_{cc}| = 80V)\}$.

Therefore, for $\{64V \le V_{ce} < (2|V_{cc}| = 80V)\}$, subject to I_c<1A, the diode effectively clamps the voltage across R_{2A}, and R_{2B}, preventing the development of sufficient voltage across R_{2B} to turn on the protection transistor.

However, for $\{64V \le V_{ce} < (2|V_{cc}| = 80V)\}$, and $I_c \ge 1A$, the increased potential drop across Re with I_c results in a net increase in voltage across R_{2A}, and R_{2B}, inducing a large enough voltage drop across R_{2B} to trigger the protection transistor.

For $(0V \le V_{ce} < 64V)$, the diode is off, (open-circuit to a first-order approximation), and the circuit reverts to a linear foldback, single slope regime.

Resistor values are calculated by developing simultaneous equations for segments B-C, and A-B, at points B and A respectively, (figs. 15, and 16). Resistor, R_1 is selected with a view to minimising diode power dissipation when R_1 and the diode are exposed to the magnitude sum of the supply rails. With reference to figure 15, let R_1=8K2, and I_d=1mA. Assuming $V_{be} = V_f \approx 0V6$, then:

$$I_1 = I_d + I_2 + I_3 \tag{6}$$

And,

$$R_{2B} = \left(\frac{0.6}{0.33}\right) R_{2A} \tag{7}$$

From equation 6:

$$\frac{(40 + 23.4)}{8K2} = 1mA + \frac{0.33}{R_{2A}} + \frac{0.6}{R_3} \tag{8}$$

With reference to figure 16, and invoking equation 7:

$$0.6 = \frac{1.65R_{2A}(0.6/0.33)}{R_{2A}(0.6/0.33) + R_{2A} + 8K2R_3/(8K2 + R_3)} \tag{9}$$

Solving equations 8, and 9 simultaneously:

$$R_3 \approx 198R7$$

$$R_{2A} \approx 88R9$$

And,

$$R_{2B} = R_{2A}(0.6/0.22) \approx 161R6$$

As was the case with the linear foldback locus of figure 2, a minimum of three output pairs is required to drive a $(4\Omega \angle \pm 60^0)$ load, since available current at Vce≈45V97 remains unchanged at Ic≈3A1. However with the protection locus in figure 13, available current per output pair at Vce≈4V is increased from 6A4 to 7A1, and the current at $V_{ce} \approx 2|V_{cc}|$, increases from 0A5 to just under 1A5 per output pair.

Since the locus is non-linear, caution must be exercised to ensure that, while pursuing the secondary objective of enhancing current delivery in the low-Vce region of the SOA, available current in the critical higher device voltage region, (i.e., $|V_{cc}| \le V_{ce} < 2|V_{cc}|$), is not simultaneously compromised by the location of the breakpoint.

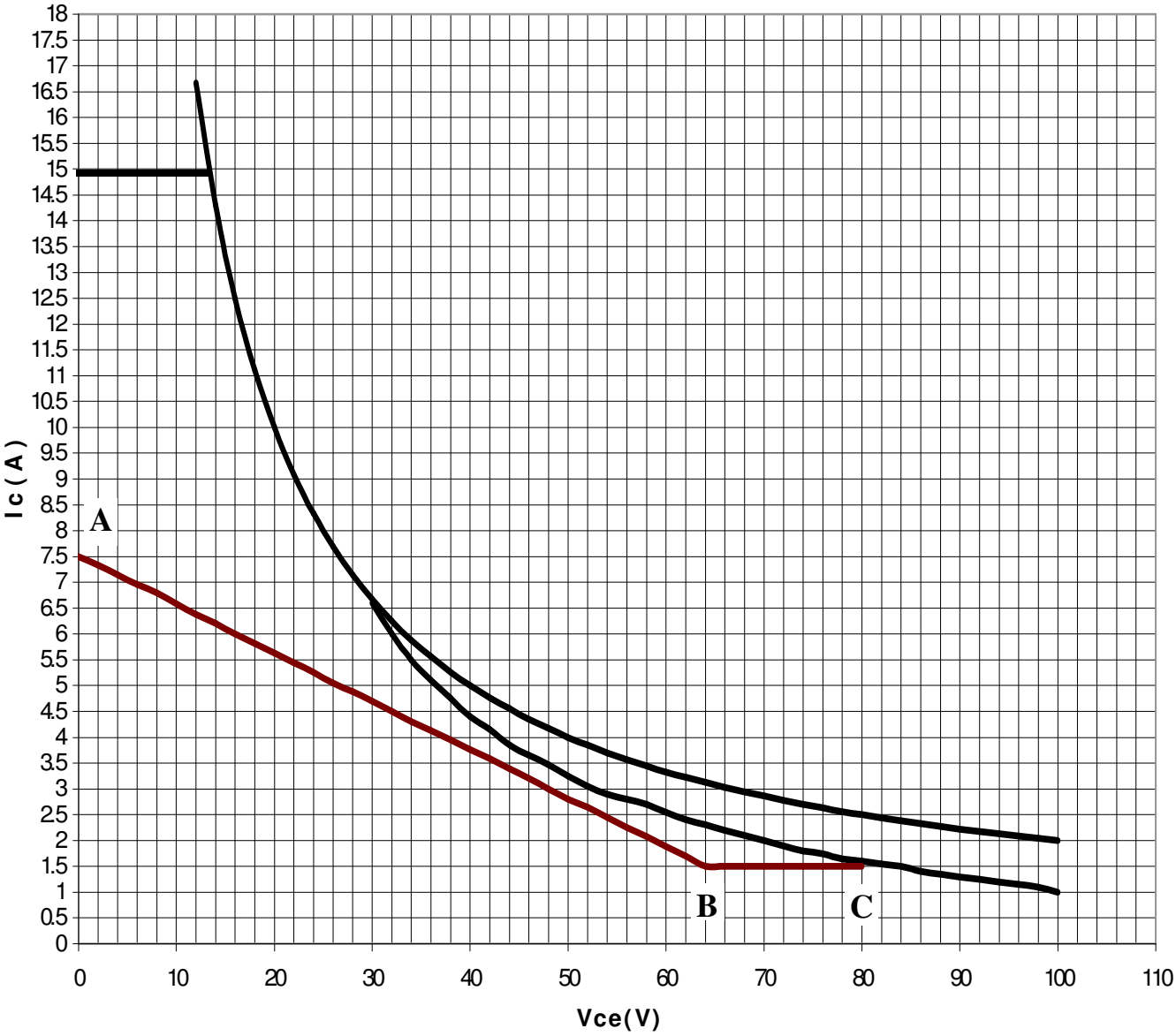

Fig.13. Single slope, single breakpoint non-linear foldback protection locus.

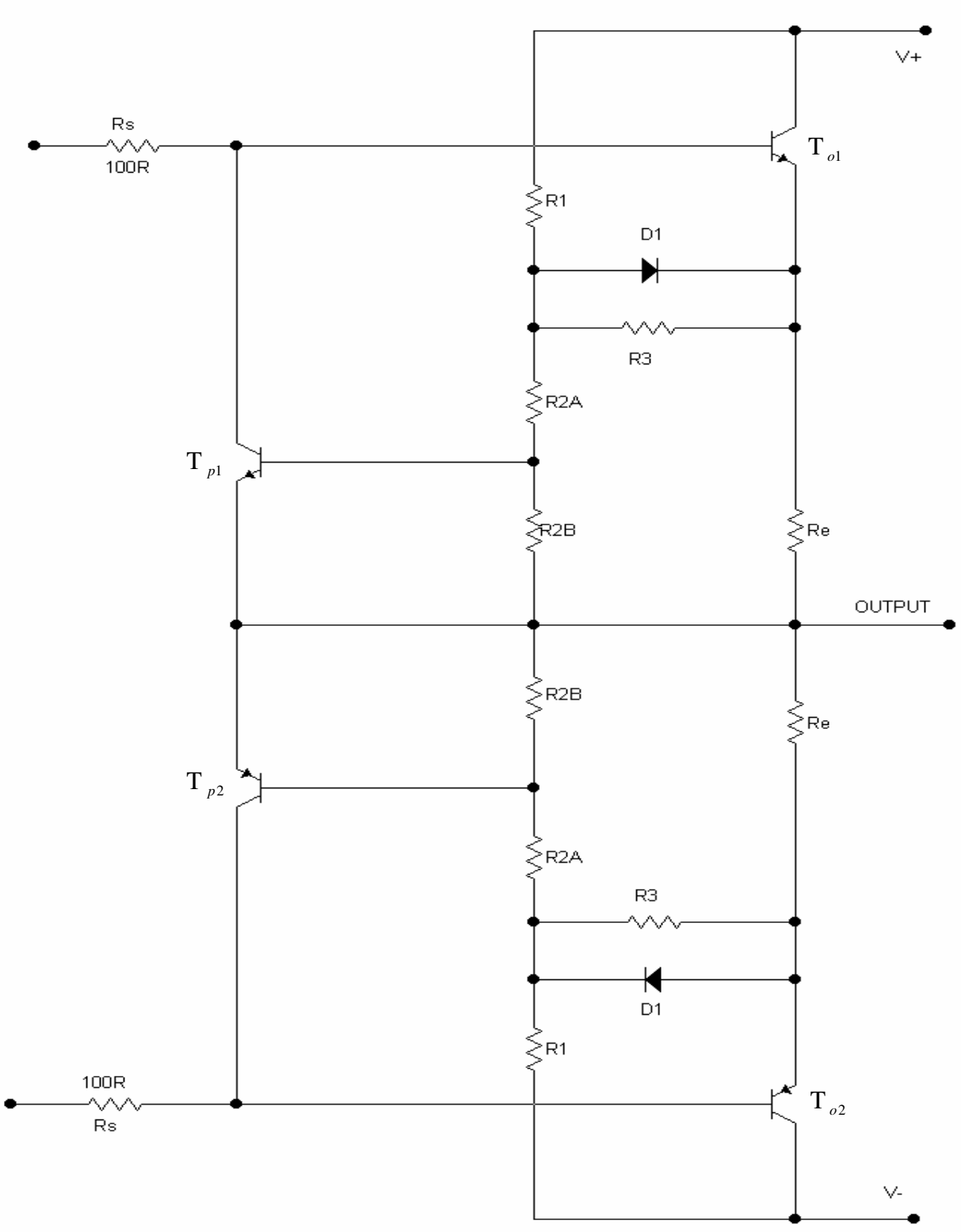

Fig.14. Single slope, single breakpoint non-linear foldback protection circuit as applied to a complementary emitter follower.

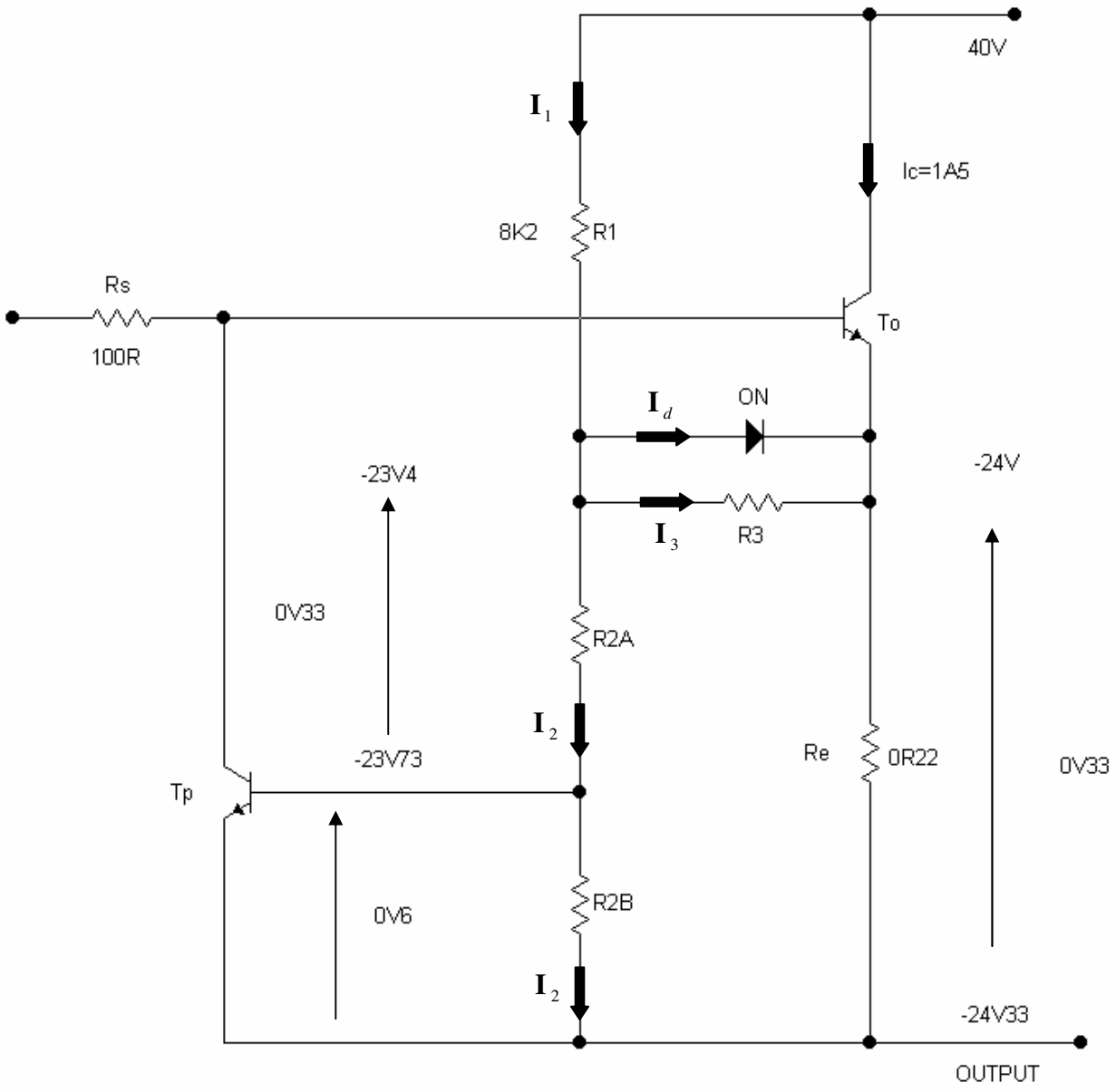

Fig.15. Output conditions at point B on the protection locus in figure 13.

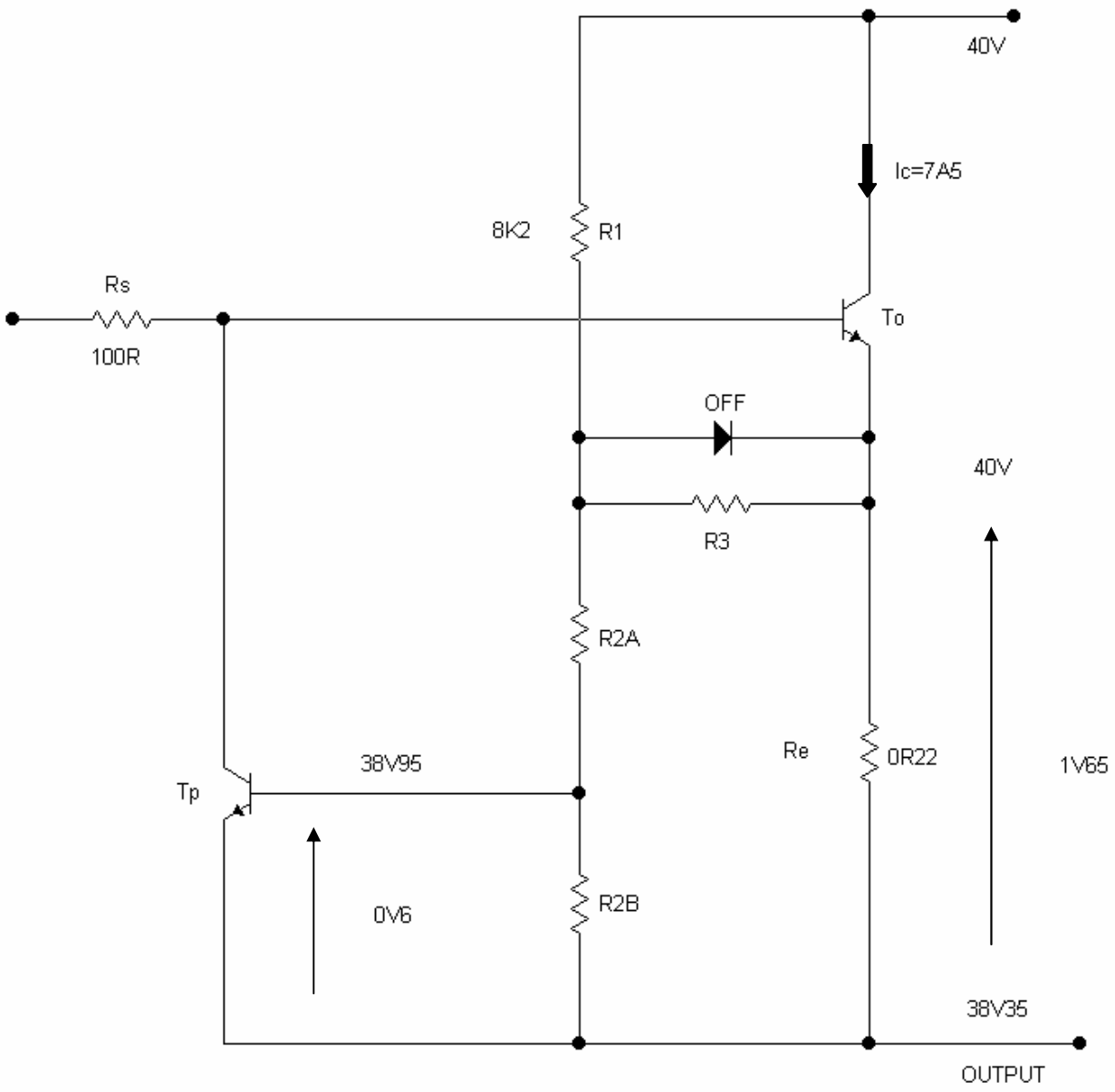

Fig. 16. Output conditions at point A on the protection locus in figure 13.

The circuits in figures 17, and 18 are frequently used[5,20,21], to realize single slope, single breakpoint non-linear foldback protection. The zener diode in figure 17 is used to establish the flat portion of the locus. This is a rather unsatisfactory solution as in practice, the zener breakdown voltage[22] can vary about its nominal value with current by as much as 25%, as the diode is driven in and out of breakdown, as is the case here. The breakpoint in the protection locus would therefore be ill defined in practice, significantly enhancing the potential for SOA violation.

The more dependable p-n diode is used, (fig. 18), to effect a single slope, single breakpoint regime by means of a simple, voltage polarity-dependent divider[23]. However this scheme, (beloved of American manufacturers), is sub-optimal with respect to flexibility in breakpoint placement, as diode commutation can only occur at $V_{out} \approx 0V$, (i.e. $V_{ce} \approx V_{cc}$), so that the nominally zero-slope portion of the locus is solely defined by the voltage drop across R_e being equal to the protection transistors base-emitter voltage, Vbe.

The locus in figure 20, requires a nominal $R_e = 0R47$, more than doubling gain-step distortion[11, pg.256.] generated by a class-AB amplifier, relative to the circuit in figure 14 for which $R_e = 0R22$. A smaller value for R_e cannot be employed as this would result in a commensurate and necessarily unsafe vertical displacement of segment B-C. Thus segment B-C is fixed for $|V_{cc}| = 40V$, and results in even more inefficient SOA usage in the crucial $|V_{cc}| \le V_{ce} < 2|V_{cc}|$ region than the compromised single slope, linear foldback arrangement in figure 5.

Further, using a fixed reference voltage, (zero volts in this case), independent of the floating collector-emitter voltage, V_{ce}, as the basis for VI protection is rather optimistic, as it presumes equally invariant supply rails that do not sag under load. A nominal 40V supply rail which sags by 5V under load would effect a 5V horizontal displacement, (fig. 20), of segment A-B to D-E. Conversely, a primary supply surge could cause a potentially disastrous horizontal translocation along B-C of segment A-B, into and perhaps well beyond the transistor's SOA limits

Since the diodes in figure 18 are in theory never forward biased simultaneously, the modification in figure 19 is often adopted[18], in what may at first appear to be an elegant simplification. The excision of one of the resistors in this fashion is alas a false economy at best, as the performance of the circuit is now significantly compromised by the finite reverse recovery time of the diodes, with minority carrier storage causing the diodes to conduct briefly when reverse biased. This often results in minute, intermittent zero-crossing oscillation at the output, particularly with a reactive load, which may easily be misdiagnosed as crossover distortion.

Since segment B-C is established by merely selecting $R_e = 0R47$, only point A on locus A-B-C, (fig. 20), is required to obtain a solution.

With reference to figure 21, and letting $R_1 = 220R$, and $V_{cc} = 40V$:

$$I_2 \approx I_1$$

Where,

$$I_1 = (40 - 34.02)/220R \approx 27.18mA$$

With $V_f \approx 0V7$ at 27mA,

$$R_2 = V_{R2}/I_2 \approx (34.02 - 0.7)/27.18mA \approx 1K2$$

The circuit in figure 18 is capable of modest improvement however, and therefore merits closer scrutiny.

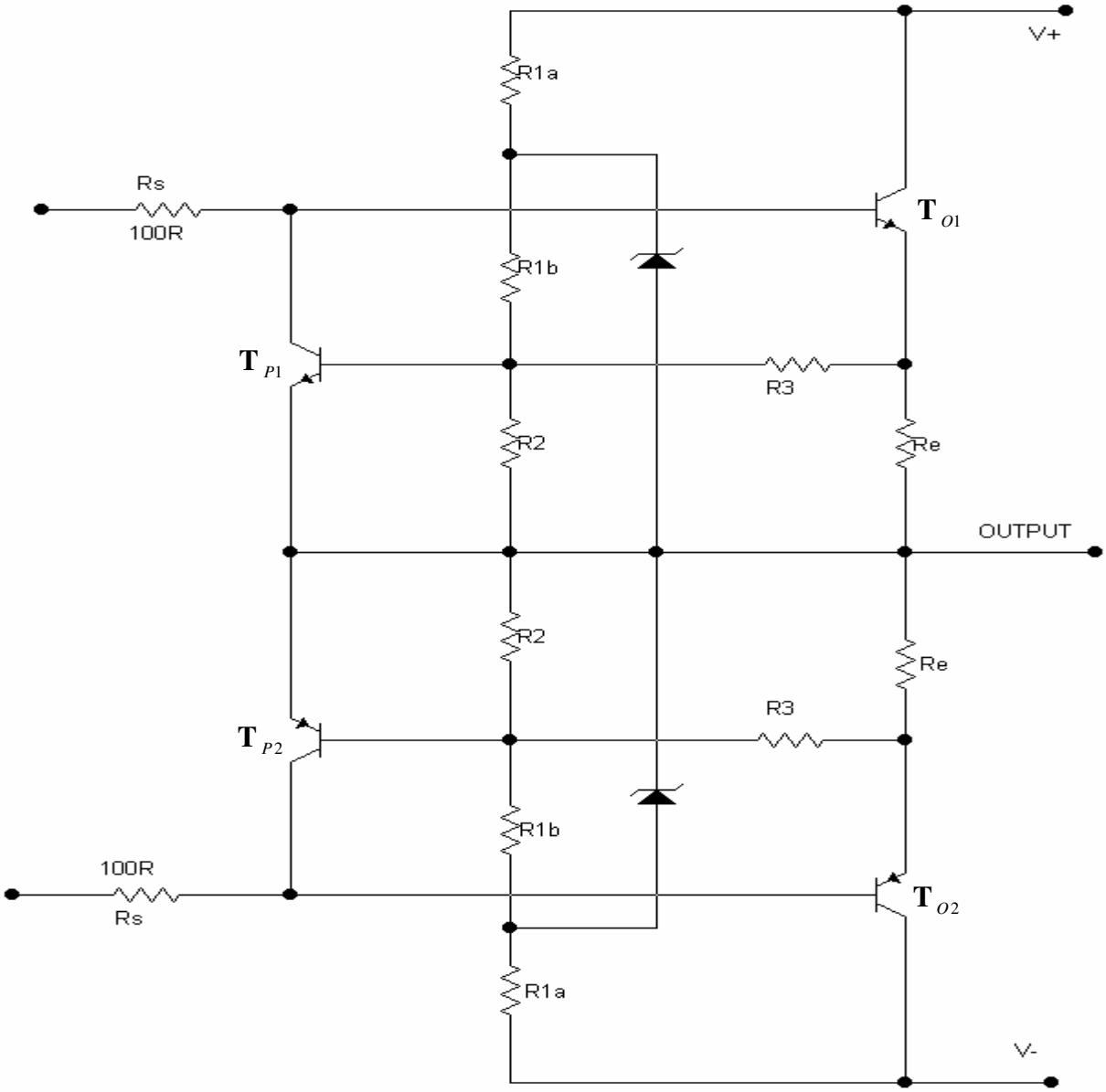

Fig. 17. Zener diode-based single slope, single breakpoint non-linear foldback limiter.

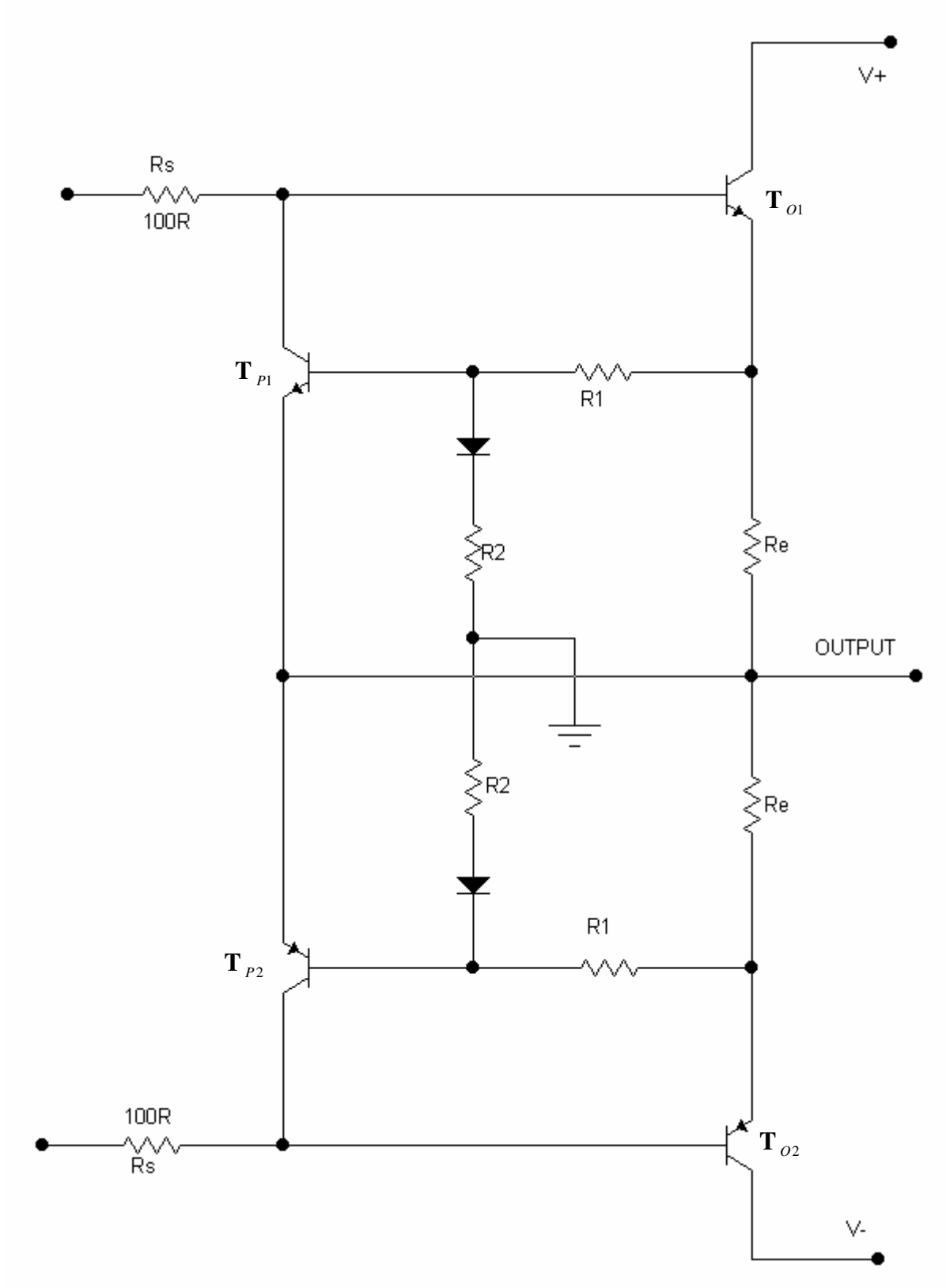

Fig. 18. Polarity-dependent voltage divider used to introduce single breakpoint in otherwise linear-slope locus.

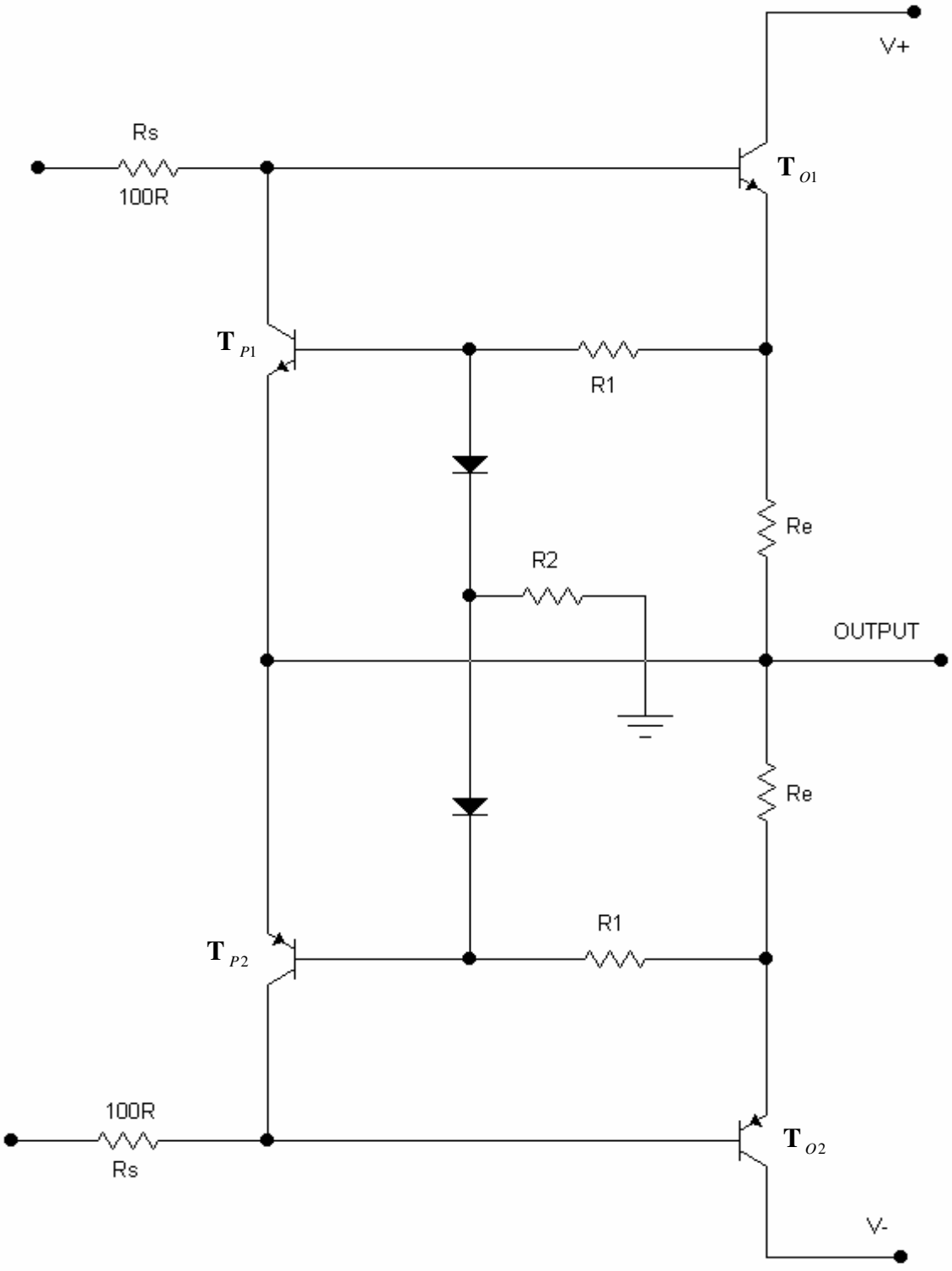

Fig. 19. A common variation in figure 18, which results in inferior performance due to the finite reverse recovery time of the diodes.

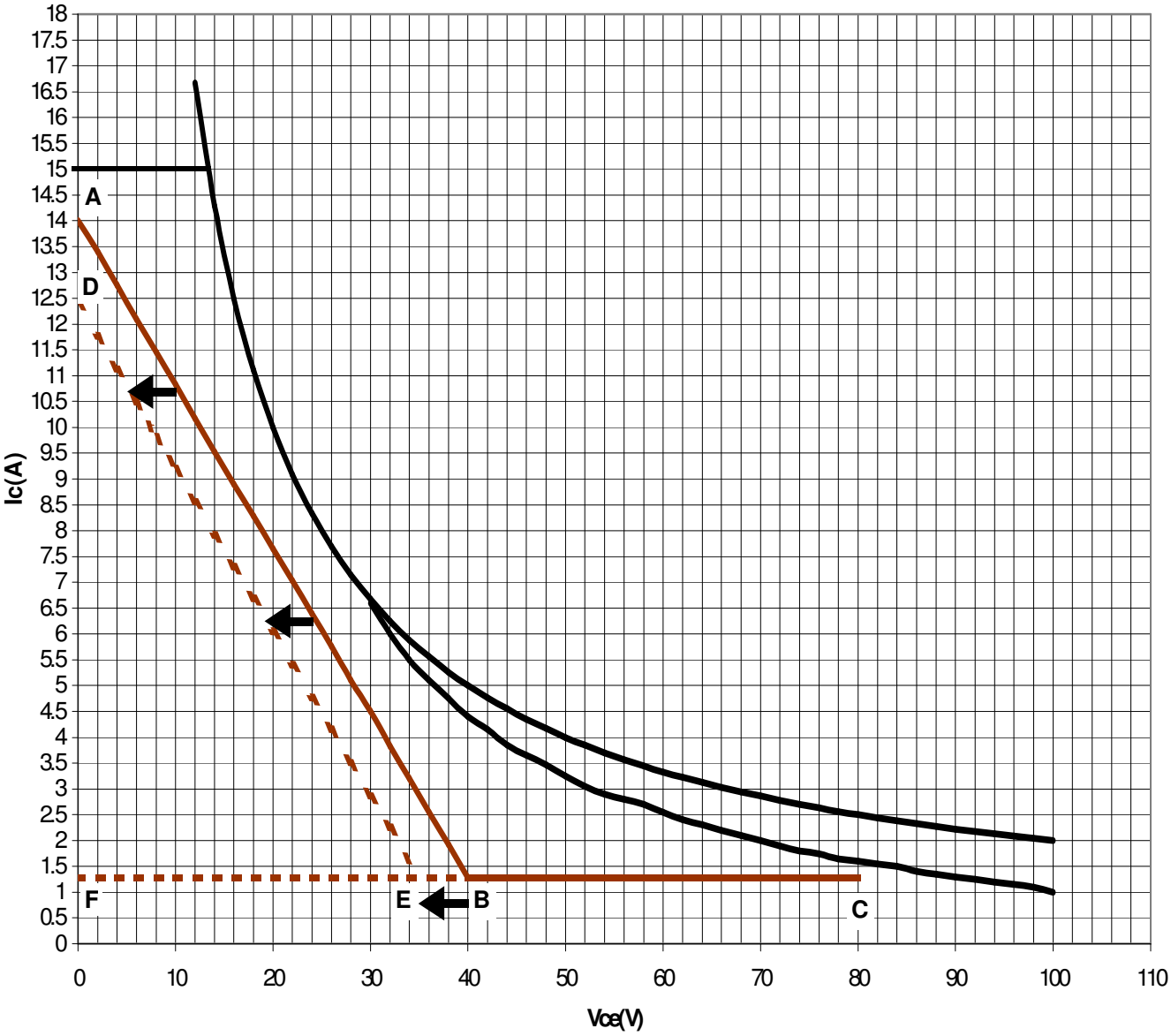

Fig. 20. Single slope, single breakpoint, non-linear protection locus described by network in figure 18. A notional 5V drop in the supply rail causes an equivalent horizontal translation of segment A-B to D-E.

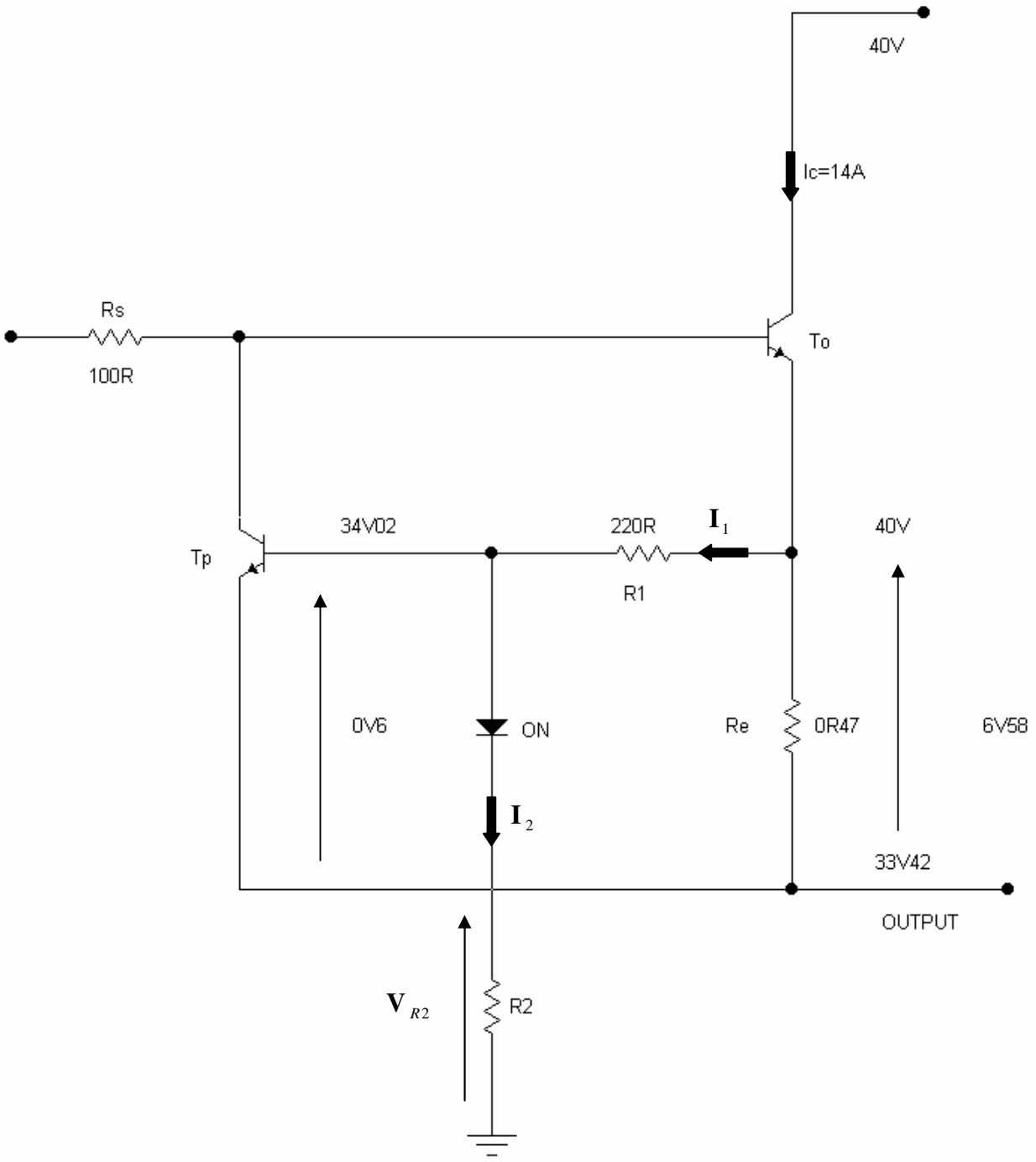

Fig. 21. Output conditions at point A on the protection locus in figure 20.

This scheme can be made more efficient, (fig. 22), by changing the voltage dividers fixed reference voltage from zero to two arbitrary voltages, $V_{\mathrm{Re}f1}$, and $V_{\mathrm{Re}f2}$, of equal magnitude but opposite polarity, such that $\left\{0V < \left(\left|V_{\mathrm{Re}f1}\right| = \left|V_{\mathrm{Re}f2}\right|\right) < \left|V_{cc}\right|\right\}$; nominal 40V rails are assumed. This enhances the flexibility of the circuit, as the breakpoint can now be freely located along C-F, (fig. 23), giving rise to a more efficient locus, B-E-F.

The reference voltage is generated by a zener diode, which in contrast with figure 17, is acceptable, as the current established by the diode's current limiting resistor, R_z, is reasonably constant, which makes for a substantially invariant voltage drop across the diode. A depletion mode MOSFET configured as a current regulator could be used instead of R_z to firmly establish quiescent conditions. This is expensive, and therefore probably unjustifiable in a commercial unit.

The reference voltage, is equal in magnitude to the output voltage, V_{out}, at the breakpoint in locus B-E-F, (fig. 24), i.e: $\left|V_{\mathrm{Re}f1}\right| = \left|V_{\mathrm{Re}f2}\right| = \left|V_{out}\right|_{V_{ce}=60V} = 20V6$, with $V_{\mathrm{Re}f1} = -20V6$, and $V_{\mathrm{Re}f2} = +20V6$. This calls for a nominal 60V6 zener diode. It is recommended however, that the required voltage drop be realized with multiple low-voltage devices, $(6V \le V_Z \le 12V)$, as these posses a significantly lower series impedance [22]. Therefore Z_1 and Z_2 may in fact consist of six Motorola 1N5240B 10V zeners, in series with a forward biased 1N4148 diode, the whole quiescing at a nominal 10mA established by R_z.

Crucially in figure 22, the cathode of diode Z_1 is connected directly to $+V_{cc}$, effectively bootstraping $V_{\mathrm{Re}f1}$ to the supply rail, so that any anomalies on the supply are directly impressed on the reference voltage. This substantially eliminates the potentially fatal tendency of segment B-E to migrate back and forth along C-F with non-ideal supply rail variation. Similarly $V_{\mathrm{Re}f2}$ is bootstrapped to the supply rail by connecting the anode of Z_2 to $-V_{cc}$.

With reference to figure 25, and taking $R_1 = 220R$, and $V_{cc} = 40V$:

$$I_2 \approx I_1$$

Where,

$$I_1 = (40 - 35.9)/220R \approx 18.64mA$$

With $V_f \approx 0V7$ at 20mA,

$$R_2 = V_{R2}/I_2 \approx (35.9 - 0.7 + 20.6)/18.64mA \approx 3K0$$

The dependence of segment E-F on the value of R_e for the circuit in figure 22 remains its achilles heel. The singular advantage of the network in figure 14 therefore, is that it permits the arbitrary location of a breakpoint in the protection locus without undue reference to the value of R_e.

Moreover, because the entire network of figure 14 floats between the supply and output rails, the position of the locus in the SOA remains resolutely invariant in the face of deviant power supply behaviour, without recourse to a bootstrapped voltage reference. The accuracy of such a reference is necessarily compromised by its dependance on zener diodes, which are only available in discreet, preferred values.

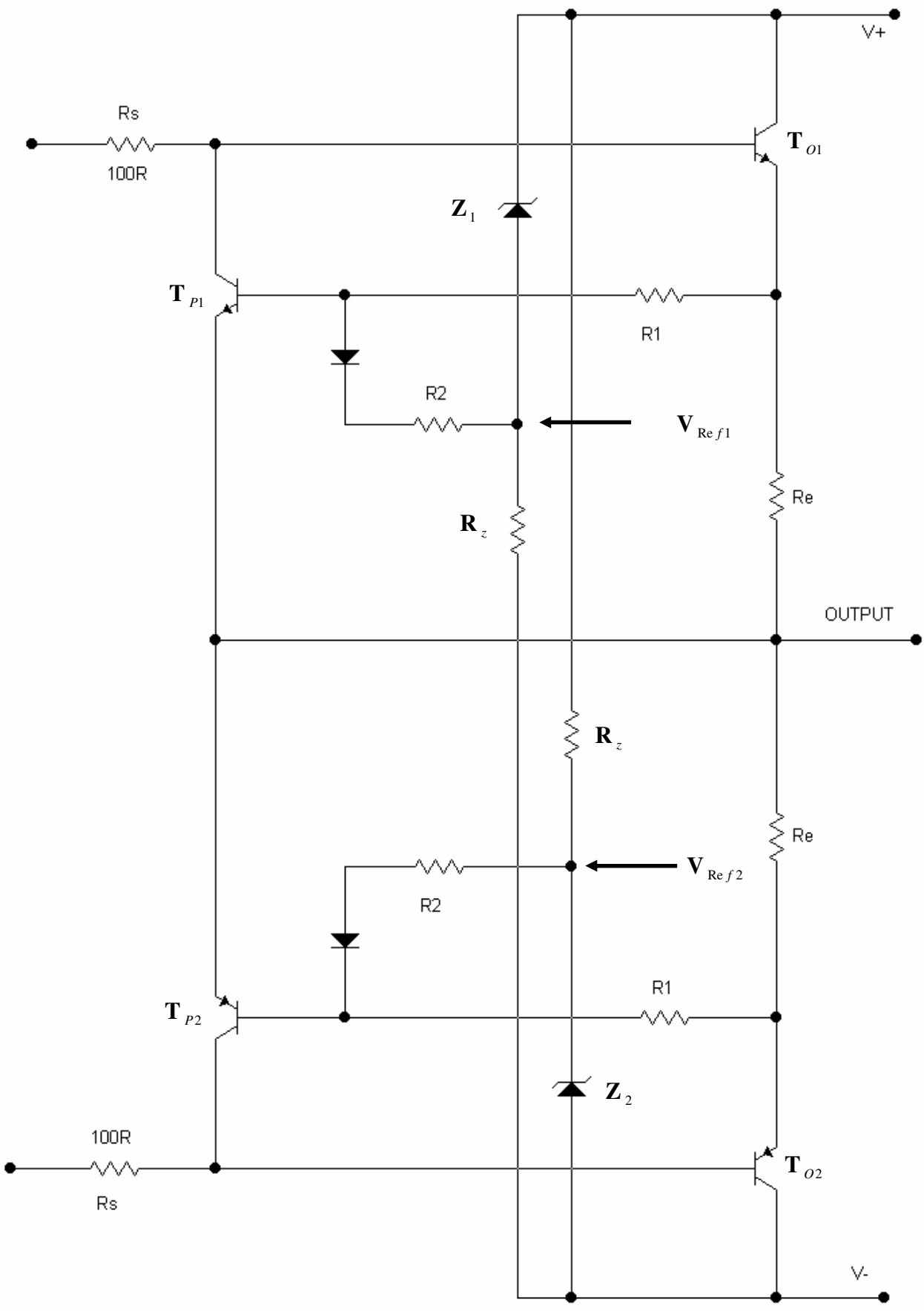

Fig. 22. The use of arbitrary voltage references of equal magnitude makes for a worthwhile improvement in efficiency.

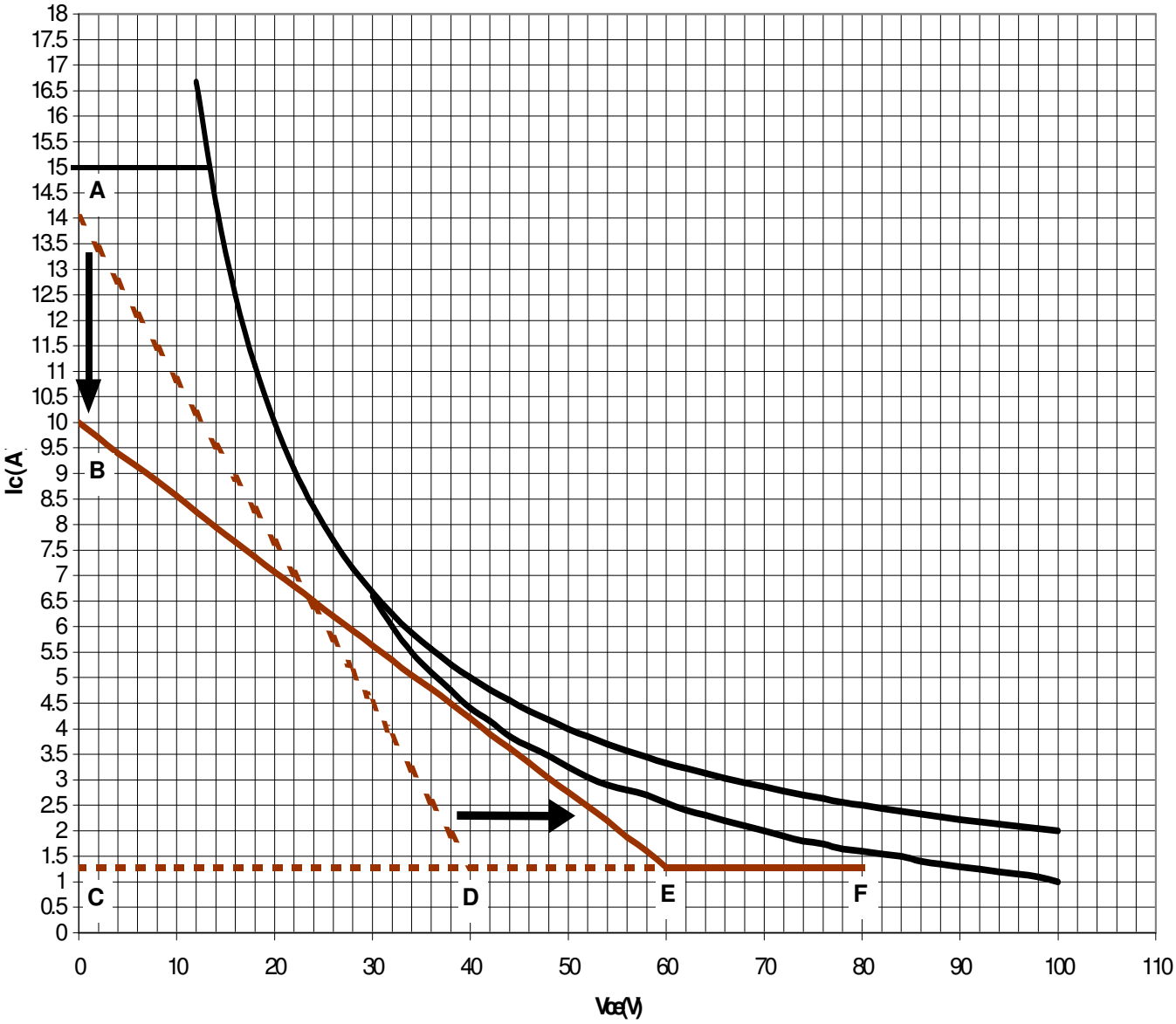

Fig. 23. Improved single slope, single breakpoint locus, B-E-F, realised by using an arbitrary voltage reference.

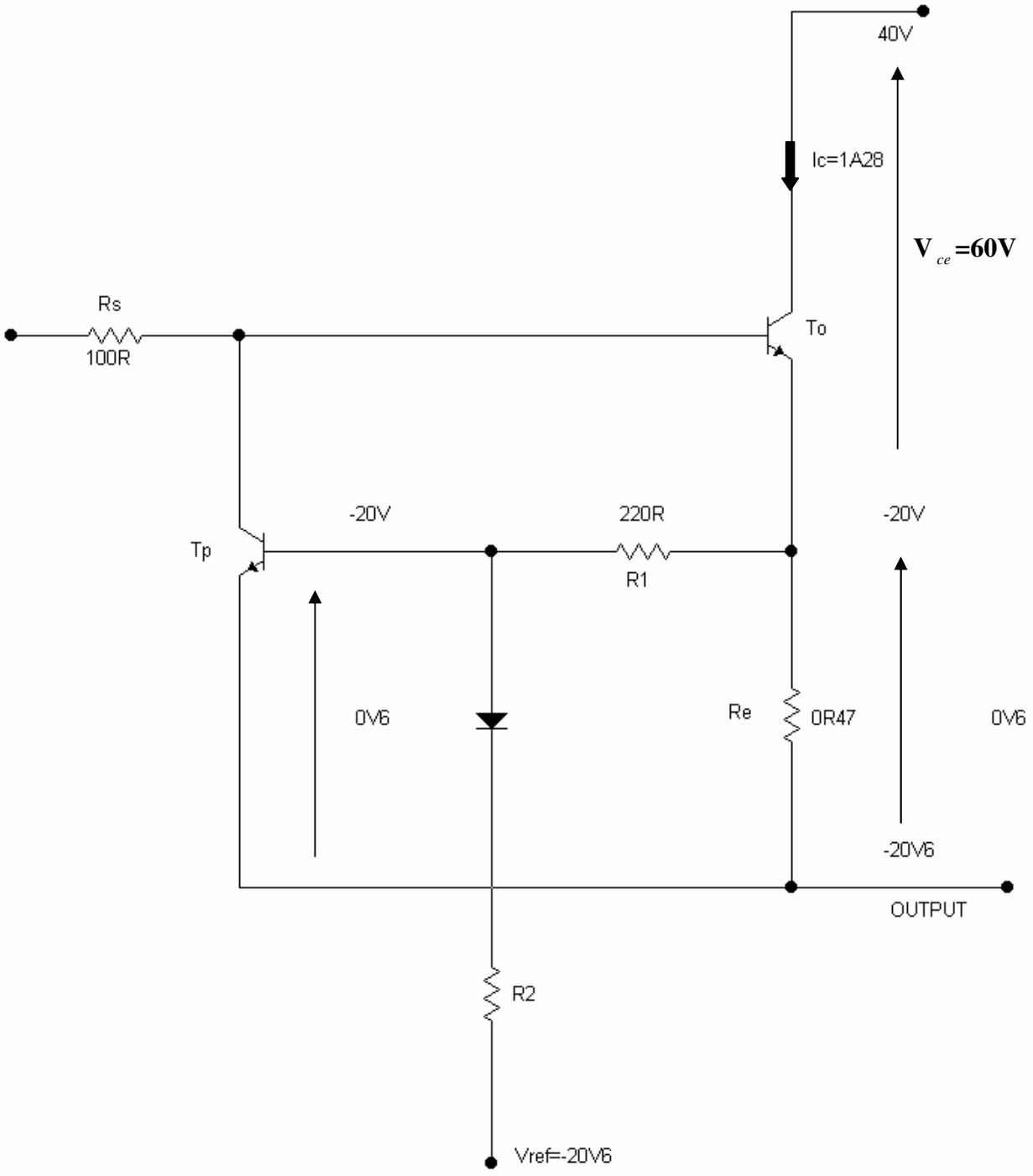

Fig. 24. The reference voltage is made equal in magnitude to the output voltage at the breakpoint, (i.e., when Vce=60V); the diode is then at the threshold of conduction.

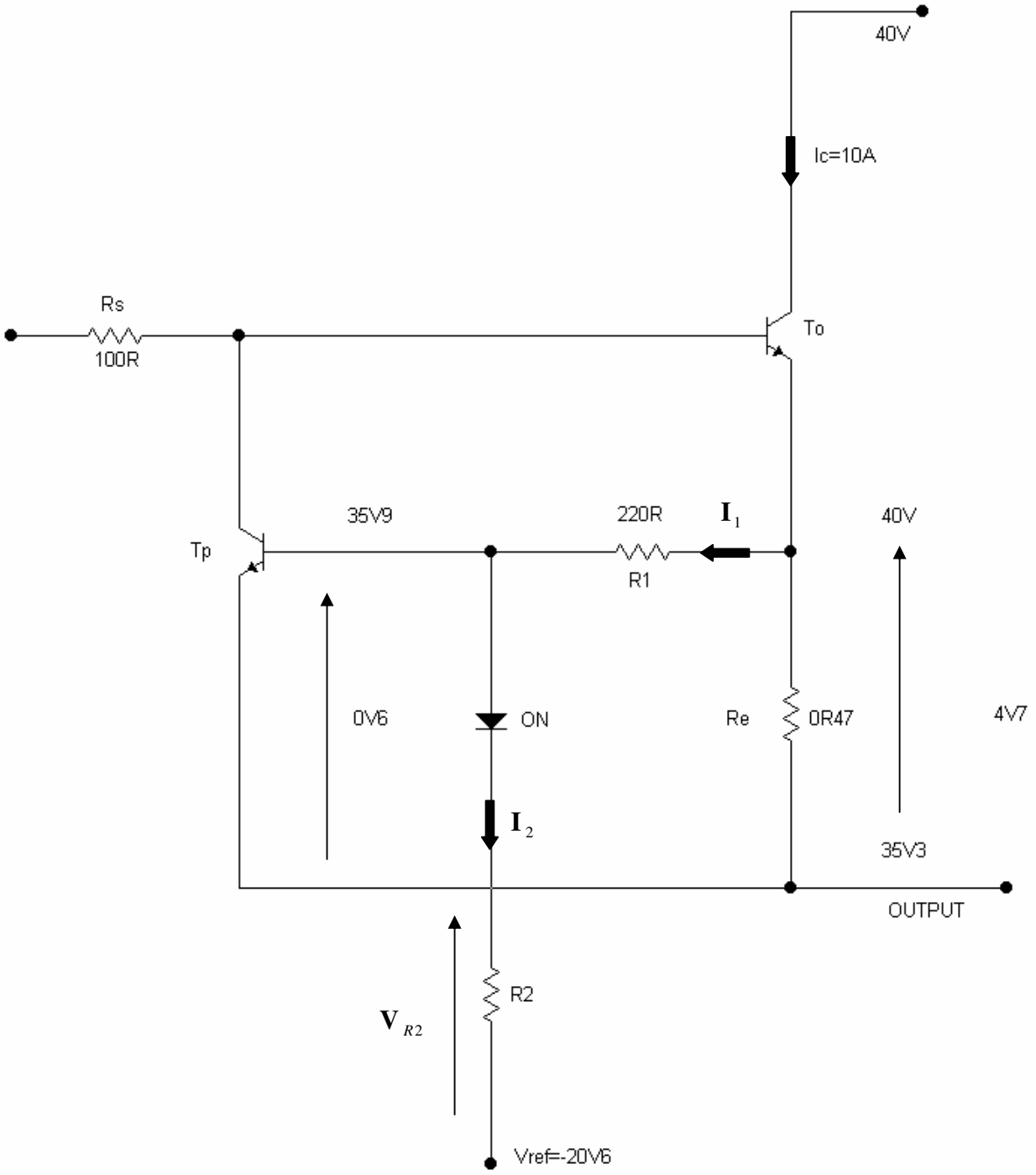

Fig. 25. Output conditions at point B on the protection locus in figure 23.

Dual slope, single breakpoint, non-linear foldback limiting.

Introducing a resistor, R_d, in series with the diode in figure 27, causes the voltage drop across the series combination to increase linearly above the diodes conduction threshold, which in turn induces a net linear increase in potential across the voltage divider R_{2A}, and R_{2B}. This gives rise to segment B-D in the protection locus, (fig. 26), whose gradient can be varied linearly with R_d about point B, thus permitting greater flexibility with regard to optimal placement of the breakpoint.

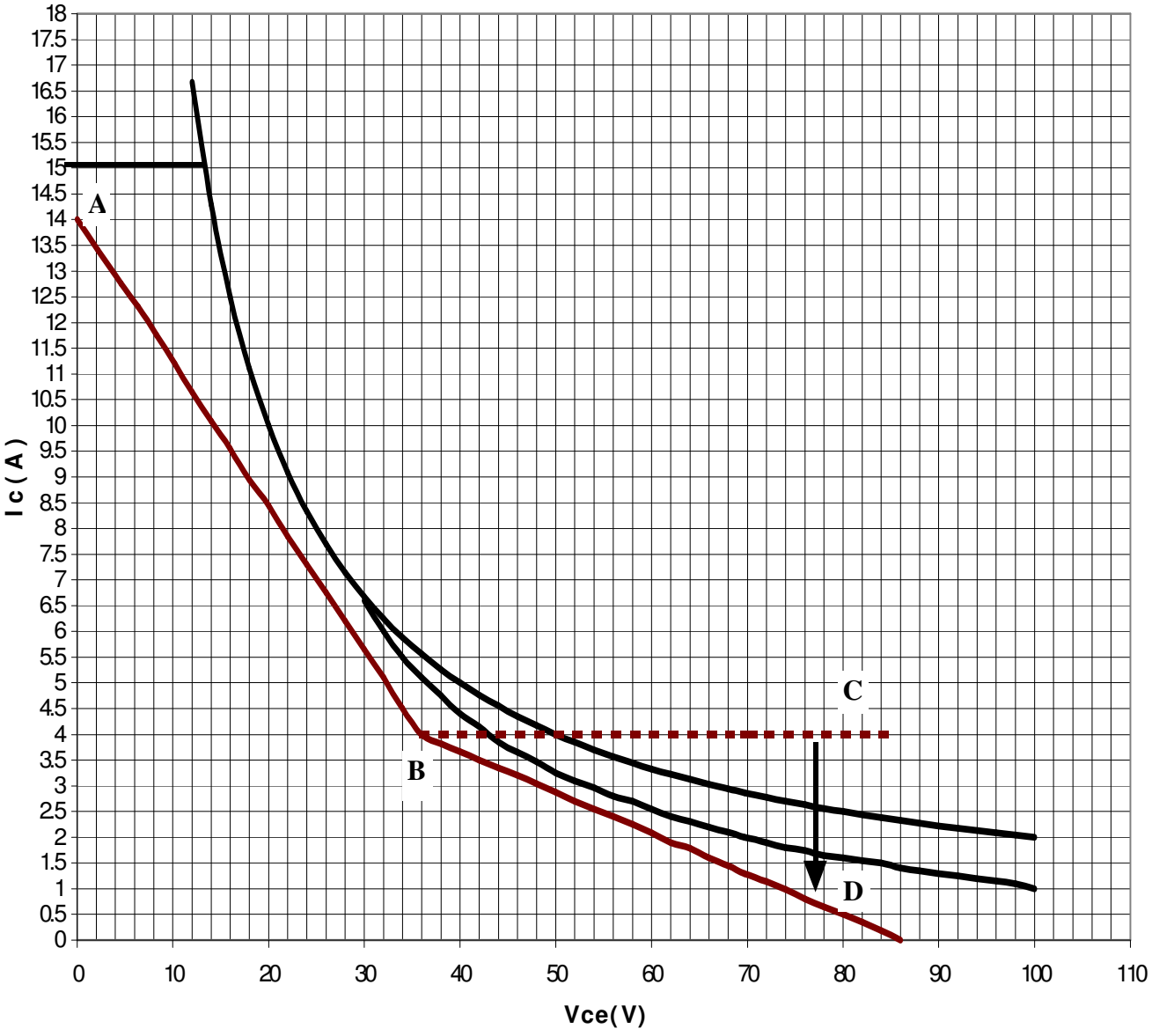

Fig.26. Dual slope, single breakpoint, non-linear foldback protection locus.

As is the case with single slope, linear foldback limiting, segment B-D must intersect the SOA's Vce axis at a value greater than the sum of the moduli of the supply rails, if spurious limiter activation is to be prevented. Available current per output pair at Vce≈4V, is further increased to 12A8 compared to 7A1 for the locus in figure 13.

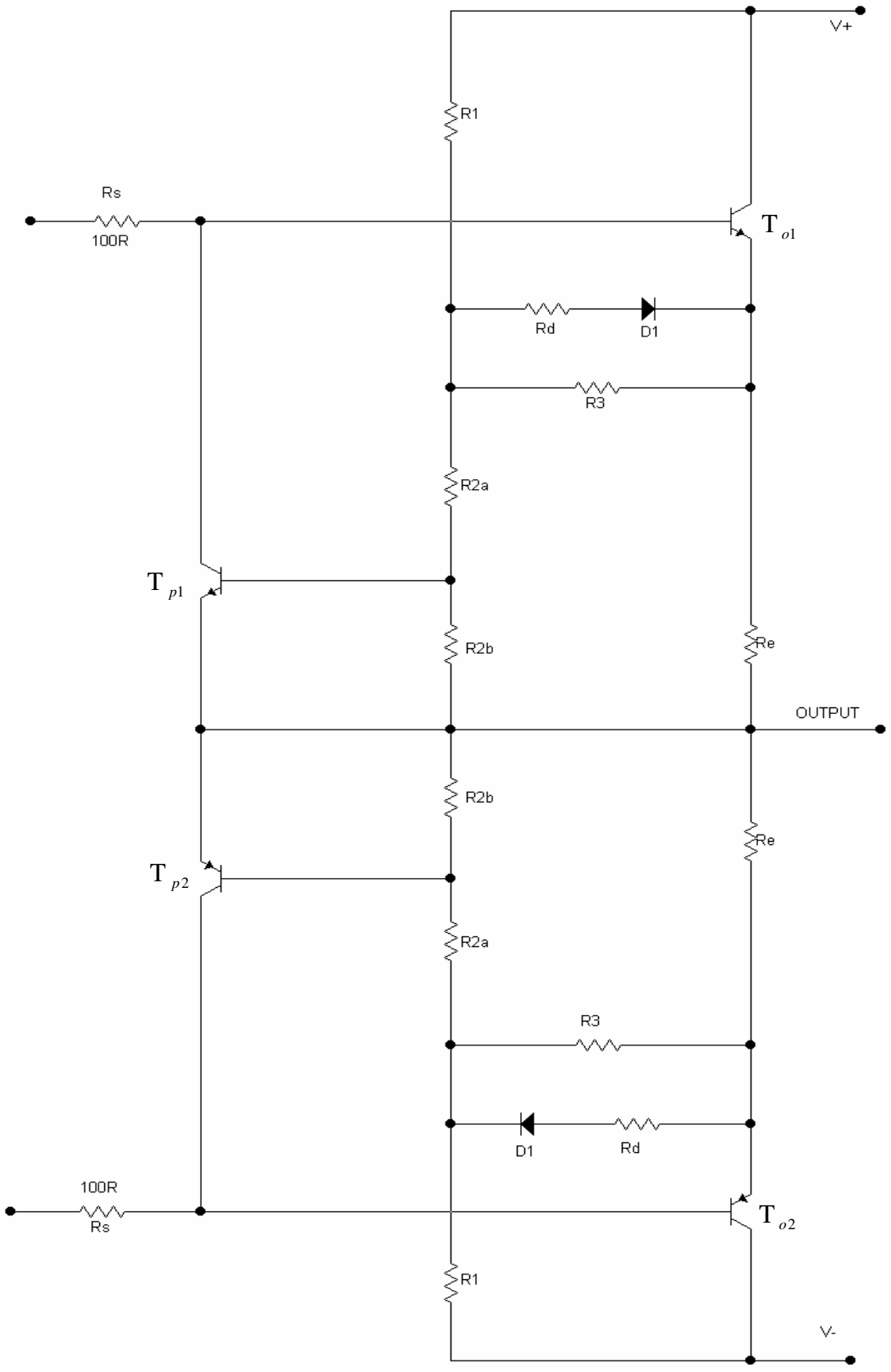

Fig.27. Dual slope, single breakpoint, non-linear foldback limiter.

Initially, resistor values without R_d are calculated for segment A-B-C, (fig. 28, and 29), and the value of R_d established *in situ*, (fig. 30), using any convenient set of points along B-D.

With reference to figure 28, and selecting R_1=8K2; I_d=1mA:

$$I_1 = I_d + I_2 + I_3 \tag{10}$$

And,

$$R_{2B} = \left(\frac{0.6}{0.88}\right) R_{2A} \tag{11}$$

From equation 10:

$$\frac{(40 - 4.6)}{8K2} = 1mA + \frac{0.88}{R_{2A}} + \frac{0.6}{R_3} \tag{12}$$

From figure 29, and invoking equation 11:

$$0.6 = \frac{3.08R_{2A}(0.6/0.88)}{R_{2A}(0.6/0.88) + R_{2A} + 8K2R_3/(8K2 + R_3)} \tag{13}$$

Solving (12), and (13), simultaneously:

$$R_3 \approx 704R7,$$

$$R_{2A} \approx 356R9,$$

And,

$$R_{2B} = (0.6/0.88)R_{2A} \approx 243R3.$$

With reference to figure 30:

$$I_2 = (0.6/R_{2B}) = (0.6/243R3) \approx 2.47mA$$

$\Rightarrow$

$$V_X = (I_2 R_{2A} - 39V4) \approx -38V52$$

$\Rightarrow$

$$V_{R3} = (V_X + 39V89) \approx 1V37$$

$\Rightarrow$

$$I_3 = (V_{R3}/R3) \approx 1.94mA$$

But,

$$I_d = I_1 - (I_2 + I_3) \tag{14}$$

Where,

$$I_1 = (40 - V_X)/8K2 \approx 9.58mA.$$

$\Rightarrow$

$$I_d = 9.58mA - (2.47mA + 1.94mA) \approx 5.17mA$$

$\Rightarrow$

$$R_d = (V_{Rd}/I_d) = (V_{R3} - 0.6)/I_d \approx 149R1$$

It may well be worthwhile at this point to consider that, while the forward voltage drop, $V_f \approx 0.6V$ at $I_d \approx 1mA$ for most small signal diodes at $27^0 C$, for a suitable device, such as the 1N4148, $V_f \approx 0V65$ at $I_d \approx 5mA$, requiring that R_d calculated above be revised downwards for enhanced precision. Thus,

$$R_d = (V_{Rd}/I_d) = (V_{R3} - 0.65)/I_d \approx 139R3$$

As previously recommended, the calculated resistor values should be made up from series, and/or parallel combinations of 1% components where necessary.

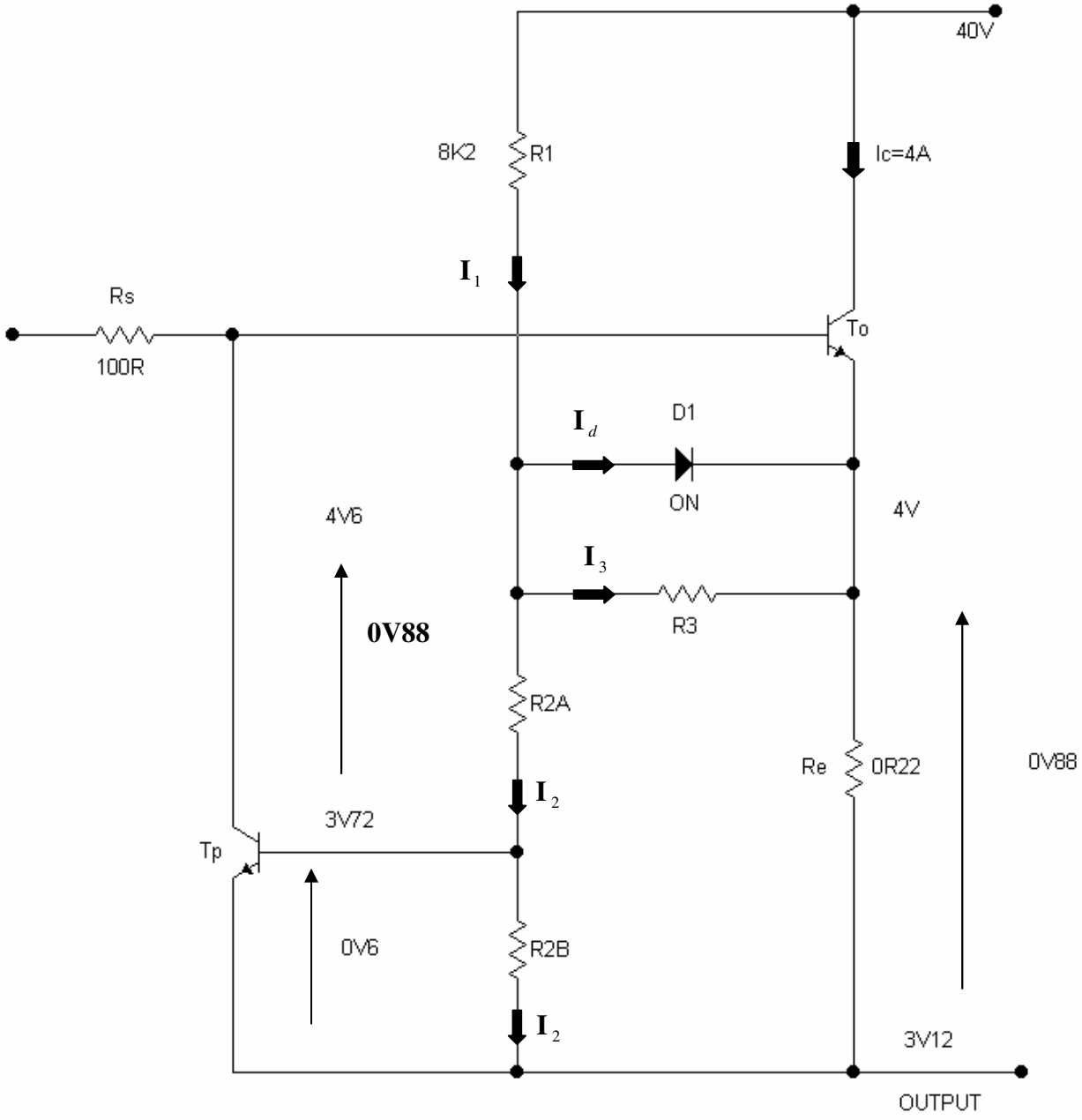

Fig. 28. Output conditions at point B on the protection locus in figure 26.

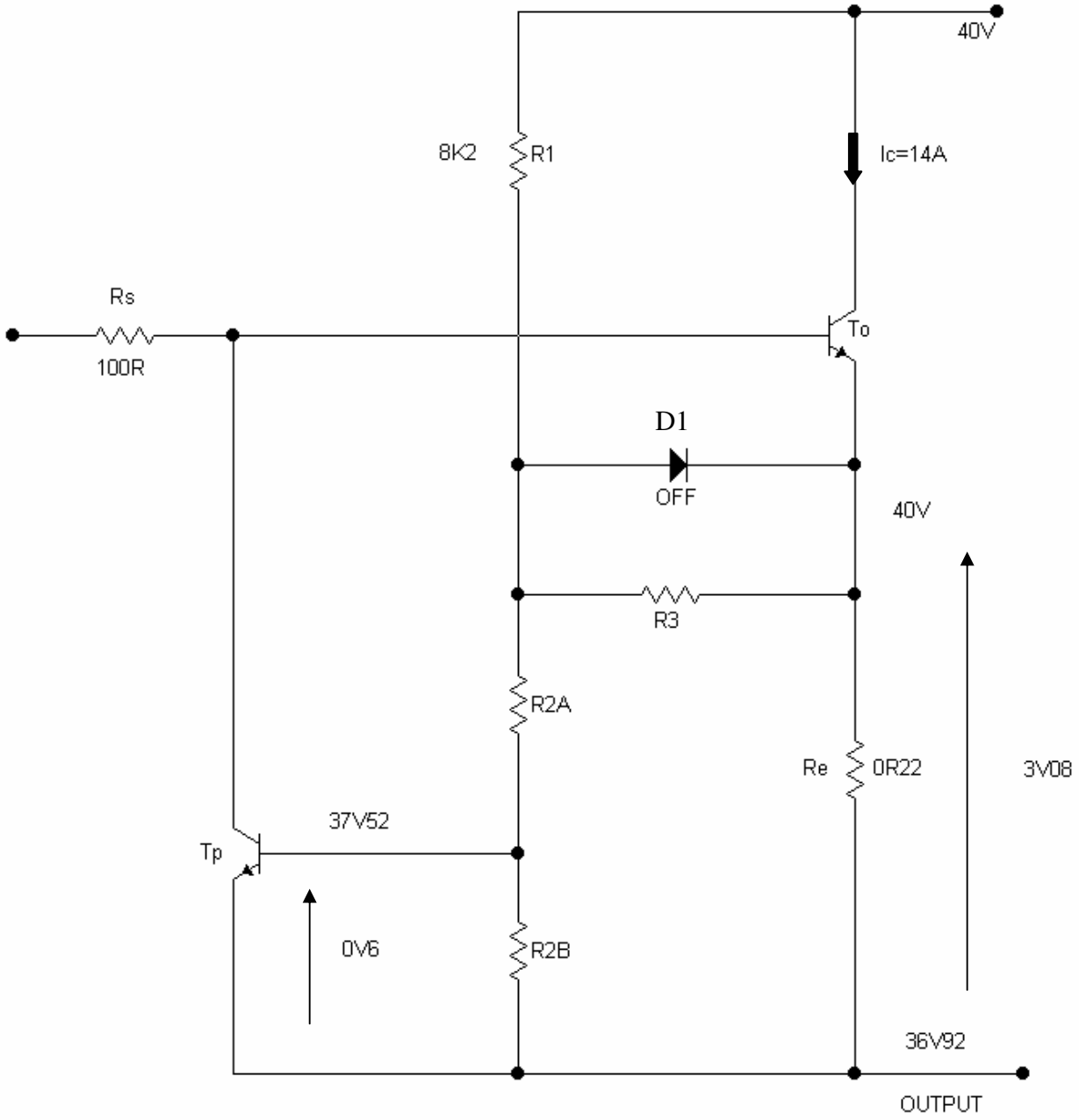

Fig. 29. Output conditions at point A on the locus in figure 26.

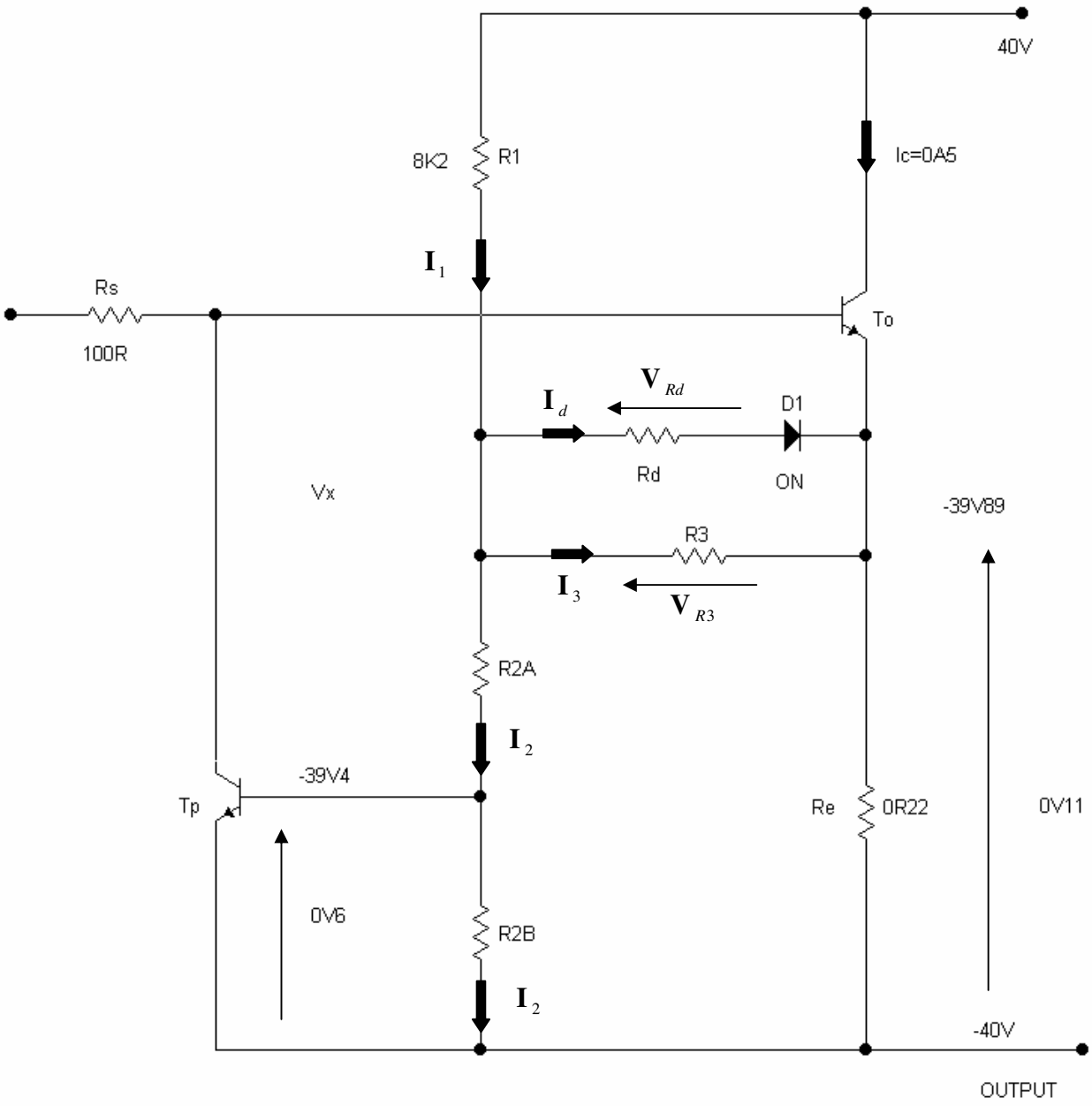

Fig. 30. Output conditions at point D on the locus in figure 26.

The dual slope, single breakpoint scheme in figure 31, sometimes erroneously[10] described as 'treble slope', (*sic*), is an amalgam of the circuits in figures 5, and 18. As in figure 18, the breakpoint occurs at $V_{out} \approx 0V$, (i.e. $V_{ce} \approx V_{cc}$), giving locus A-D-E-F, (fig. 32). However, segment D-E-F, being part of C-D-E-F, is established by R_1, and R_3, and its efficacy is therefore as dependent on the value of R_e as the network in figure 5. Resistor R_2 merely pulls the base of the protection transistor low as required for $\{0V \le V_{ce} < 40V\}$, giving segment A-D, whose position in the SOA is ill-defined for non-ideal supply rails, due to the use of an invariant voltage reference.

Since the breakpoint for this arrangement is fixed at $V_{ce} \approx V_{cc}$, only points A and F on locus A-D-E-F are required to obtain a solution.

With reference to figure 33, let $R_3 = 220R$, and $V_{cc} = 40V$:

$$I_1 \approx I_3$$

Where,

$$I_3 = (-39.4 + 39.78)/220R \approx 1.73mA$$

$\Rightarrow$

$$R_1 = (40 + 39.4)/1.73mA \approx 46K$$

With reference to figure 34:

$$I_2 \approx (40 - 37.52)/(R_1 \,//\, R_3) = 2.48/219R \approx 11.33mA$$

With $V_f \approx 0V7$ at $11mA$,

$$R_2 = V_{R2}/I_2 = (37.52 - 0.7)/11.33mA \approx 3K3$$

This scheme is clearly inferior to the standard linear foldback arrangement of figure 1, as it permits the delivery of only 1A5 at Vce≈45V97, requiring a minimum of six output pairs for $(4\Omega \angle \pm 60^0)$ load drive from $\pm 40V$ supply rails.

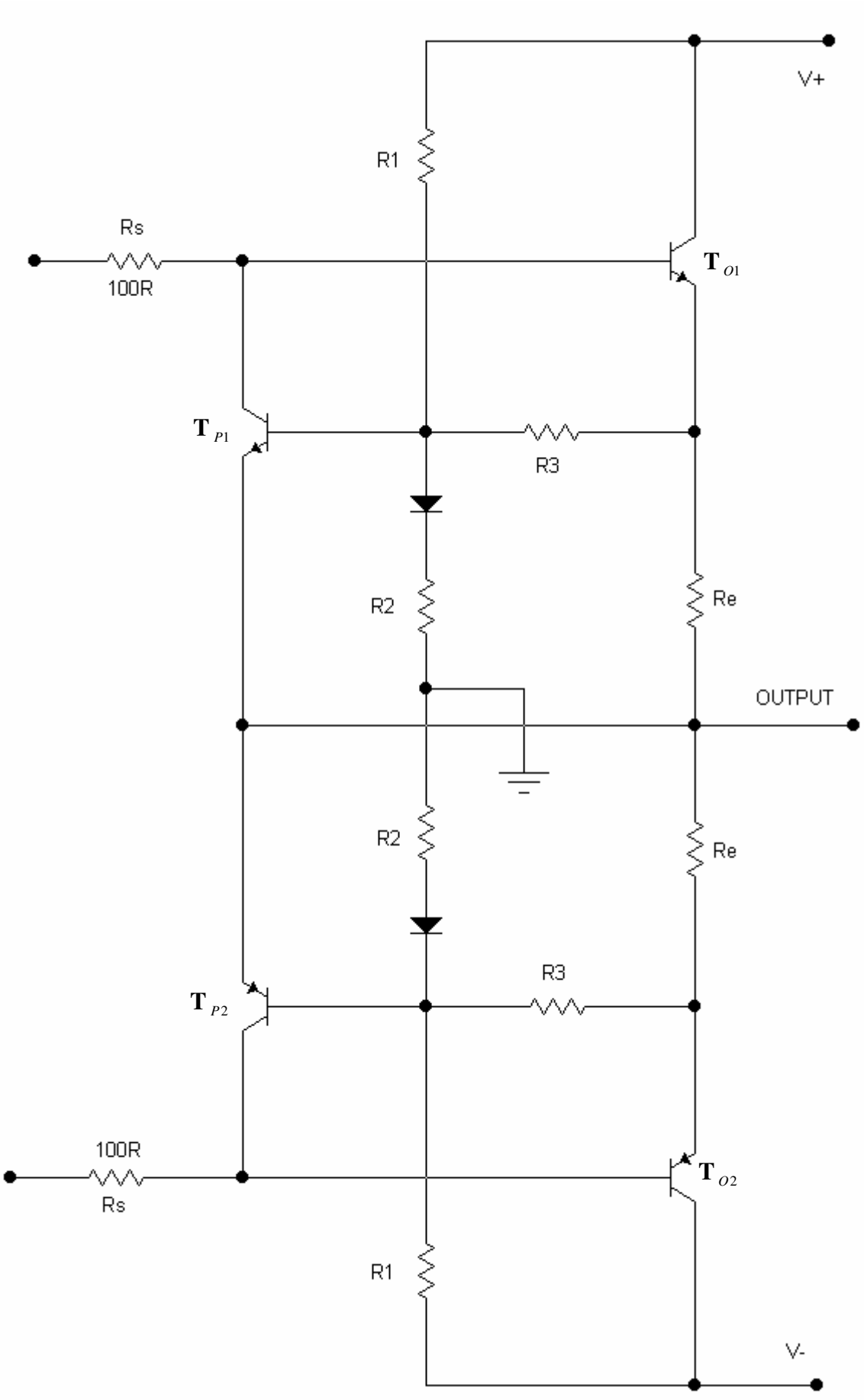

Fig. 31. This dual slope single breakpoint scheme is a logical development of the circuits in figures 5, and 18.

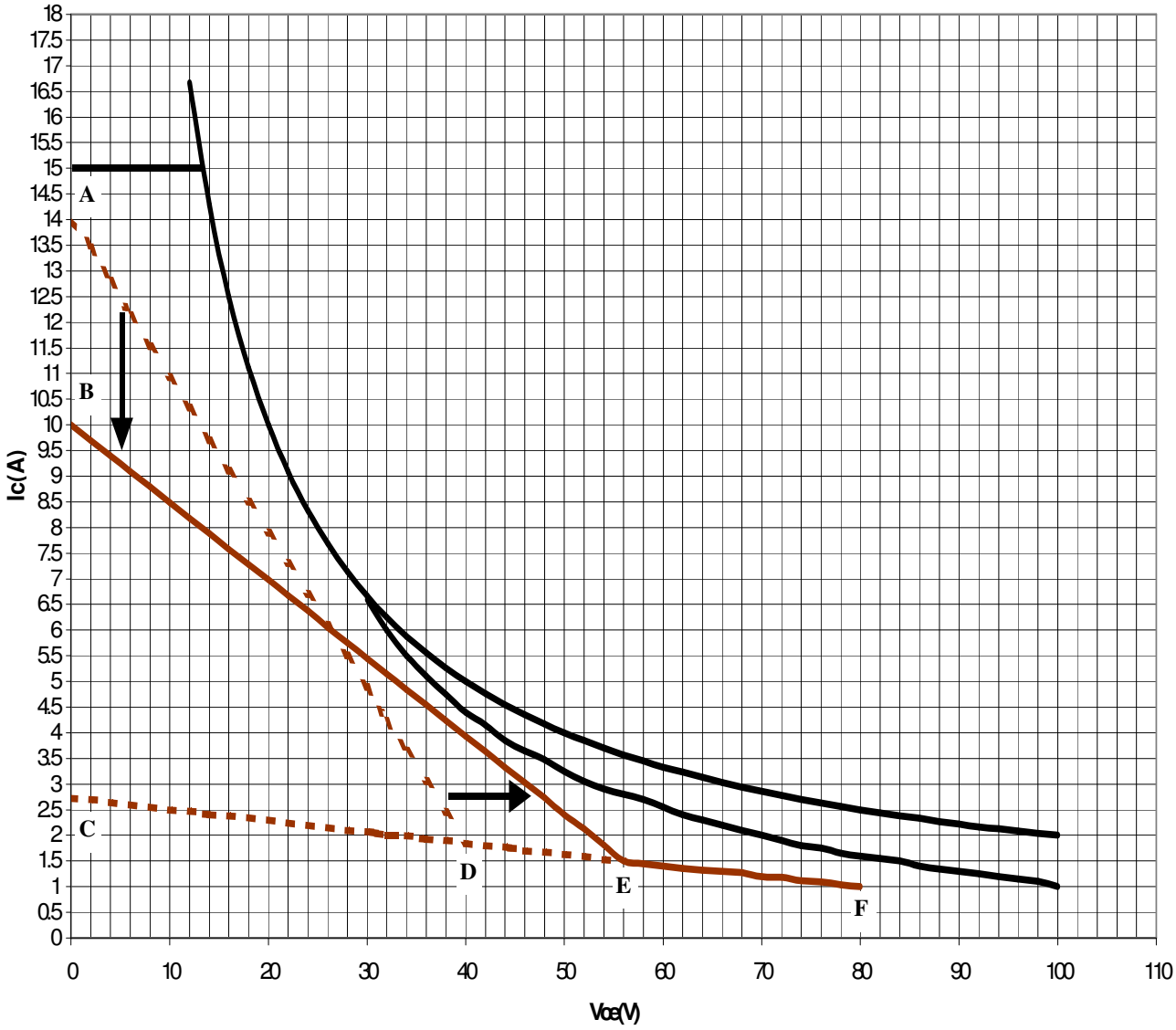

Fig. 32. Dual slope single breakpoint loci described by the circuits in figure 31 and 35.

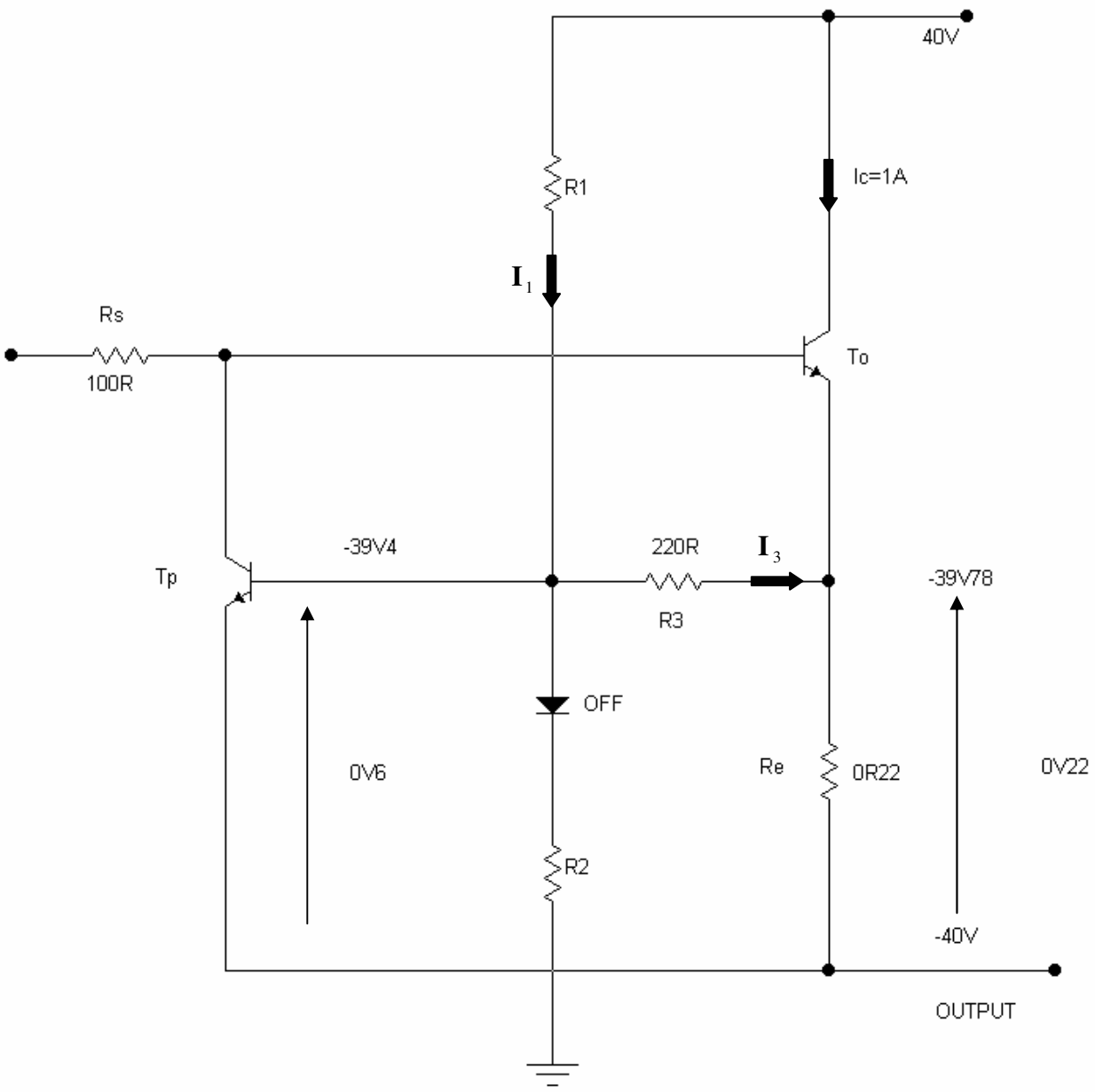

Fig. 33. Output conditions at point F on locus A-D-E-F of figure 32.

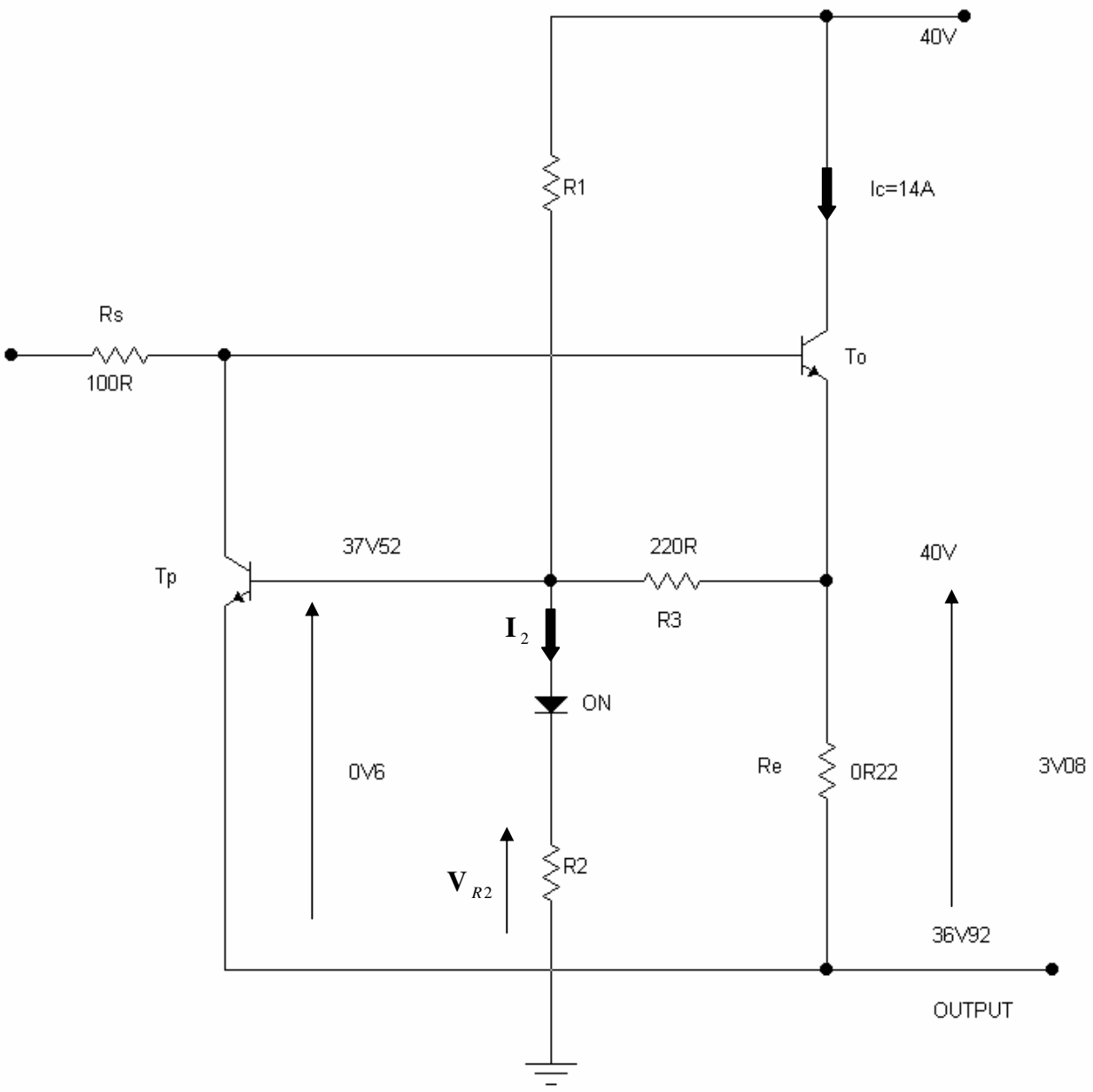

Fig. 34. Output conditions at point A on locus A-D-E-F of figure 32.

As in figure 22, the network in figure 31 can be usefully improved, (fig. 35), by changing the diode reference from zero to an arbitrary voltage, $V_{\mathrm{Re}f.}$, such that, $(0V < \left|V_{\mathrm{Re}f.}\right| < \left|V_{cc}\right|)$. This enhances the flexibility of the circuit, as the breakpoint can now be moved freely along segment C-F, giving rise to a more efficient locus, B-E-F, (fig. 32), whose position in the SOA is unaffected by supply rail variation.

The reference voltage is established by determining the output conditions at the breakpoint, (fig. 36). Therefore for locus B-E-F in figure 32, $V_{\mathrm{Re}f1} = -16V33$, and $V_{\mathrm{Re}f2} = +16V33$, which calls for a nominal 56V33 zener diode. As previously recommended, multiple low-voltage devices should be used to minimize series impedance.

With reference to figure 37:

$$I_1 \approx I_3$$

Where,

$$I_3 = (-39.4 + 39.78)/220R \approx 1.73mA$$

$\Rightarrow$

$$R_1 = (40 + 39.4)/1.73mA \approx 46K$$

With reference to figure 38:

$$I_2 = (40 - 38.4)/(R_1 \,//\, R_3) = 1.6/219R0 \approx 7.3mA$$

With $V_f \approx 0V65$ at 7mA,

$$R_2 = V_{R2}/I_2 = (38.4 - 0.65 + 16.33)/7.3mA \approx 7K4$$

Note that there is no change in the value of R_1 and R_3 in the circuits of figure 5, 31, and 35, with different values of R_2 required to merely pull the base of the protection transistor low as appropriate when the series diode is forward biased.

Although the efficacy of the protection locus is in part ameliorated by the means described above, the gradient of segment E-F, being part of C-D-E-F, is determined by resistors R_1, R_3, and limited by practical values of R_e - an affliction absent in the circuit of figure 27.

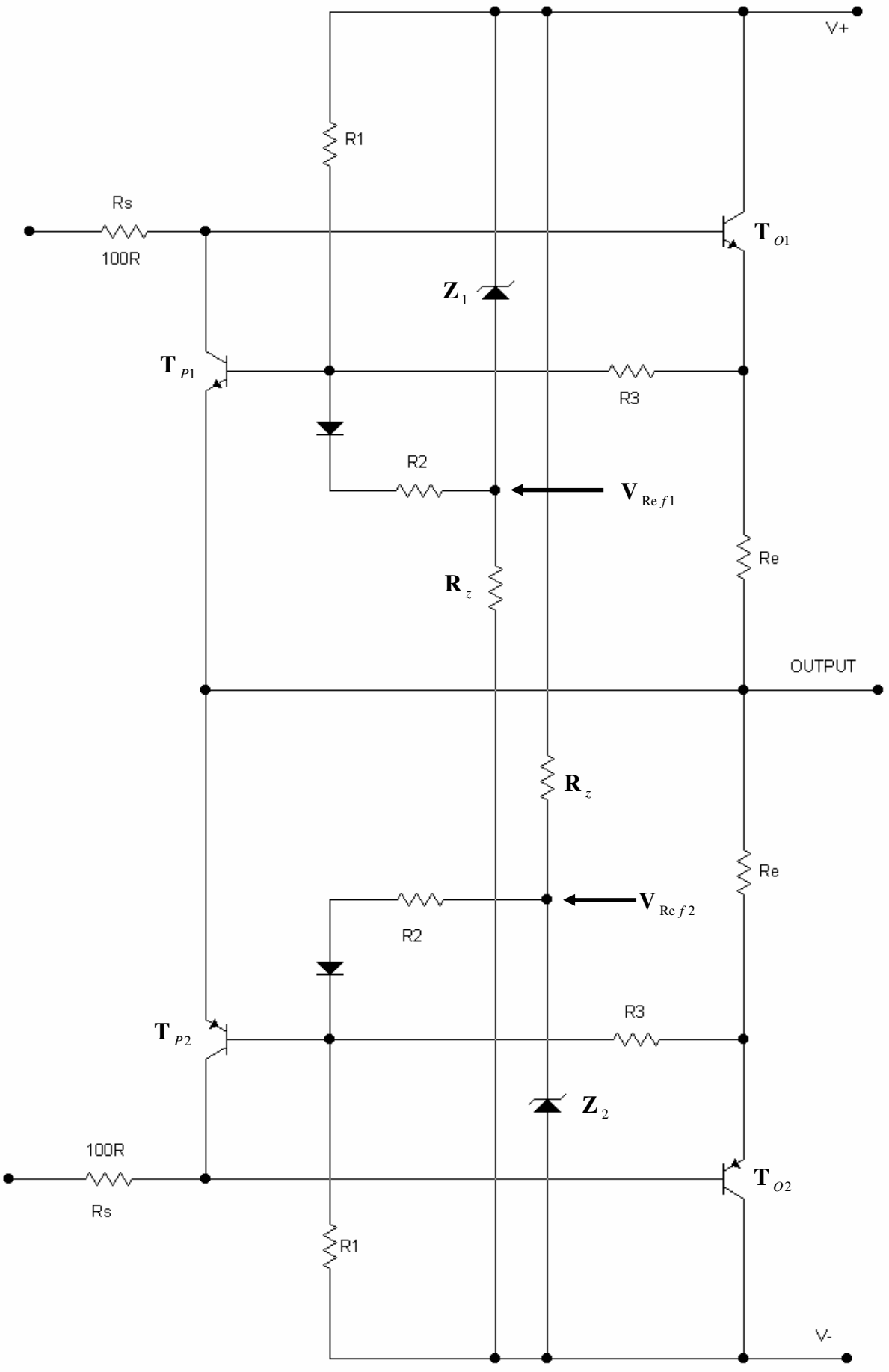

Fig. 35. Efficacy of the compromised dual slope scheme of figure 31 is improved by using arbitrary, bootstrapped voltage references of equal magnitude.

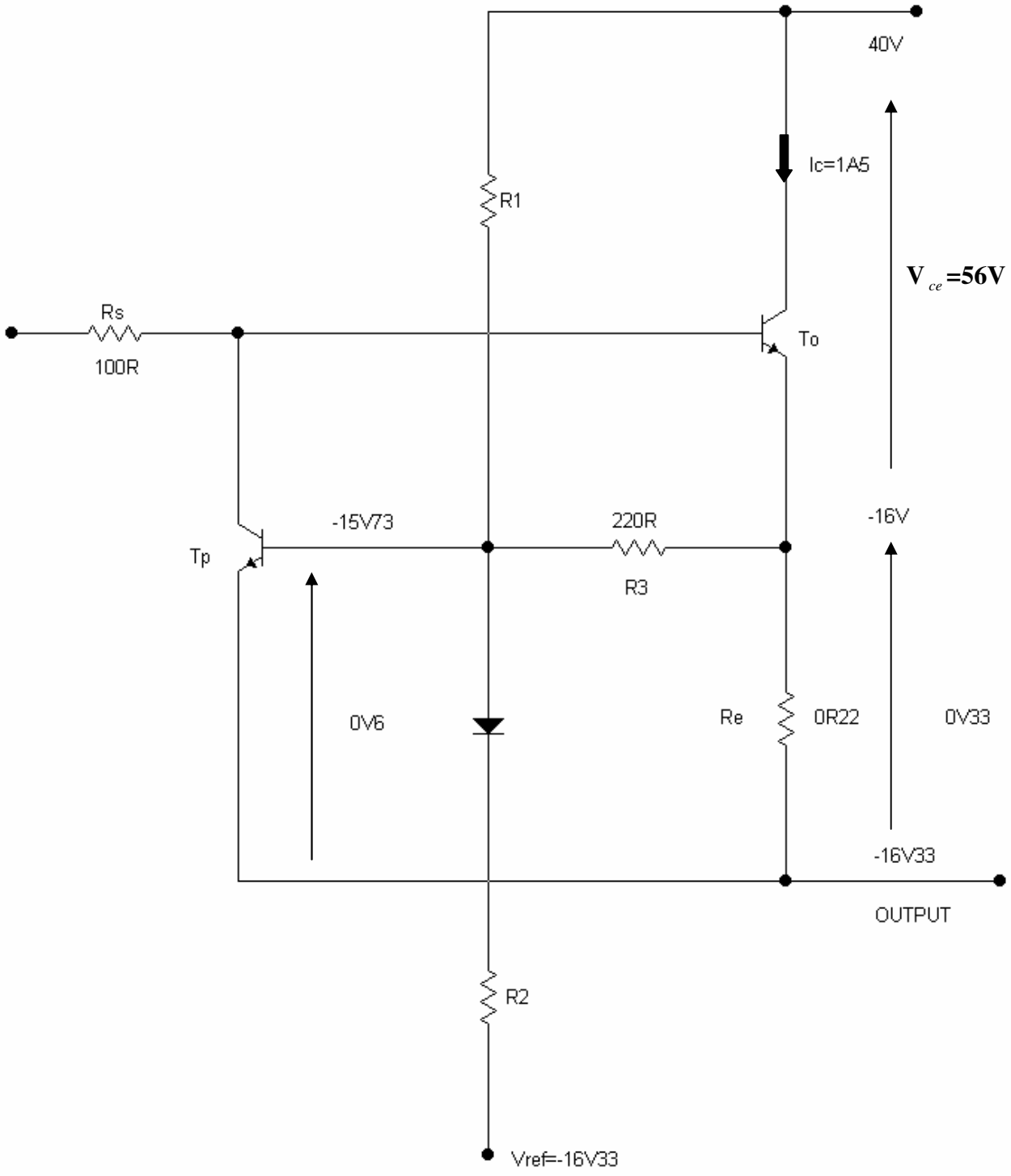

Fig. 36. The reference voltage is made equal in magnitude to the output voltage at the breakpoint, (i.e., when Vce=56V); the diode is then at the threshold of conduction.

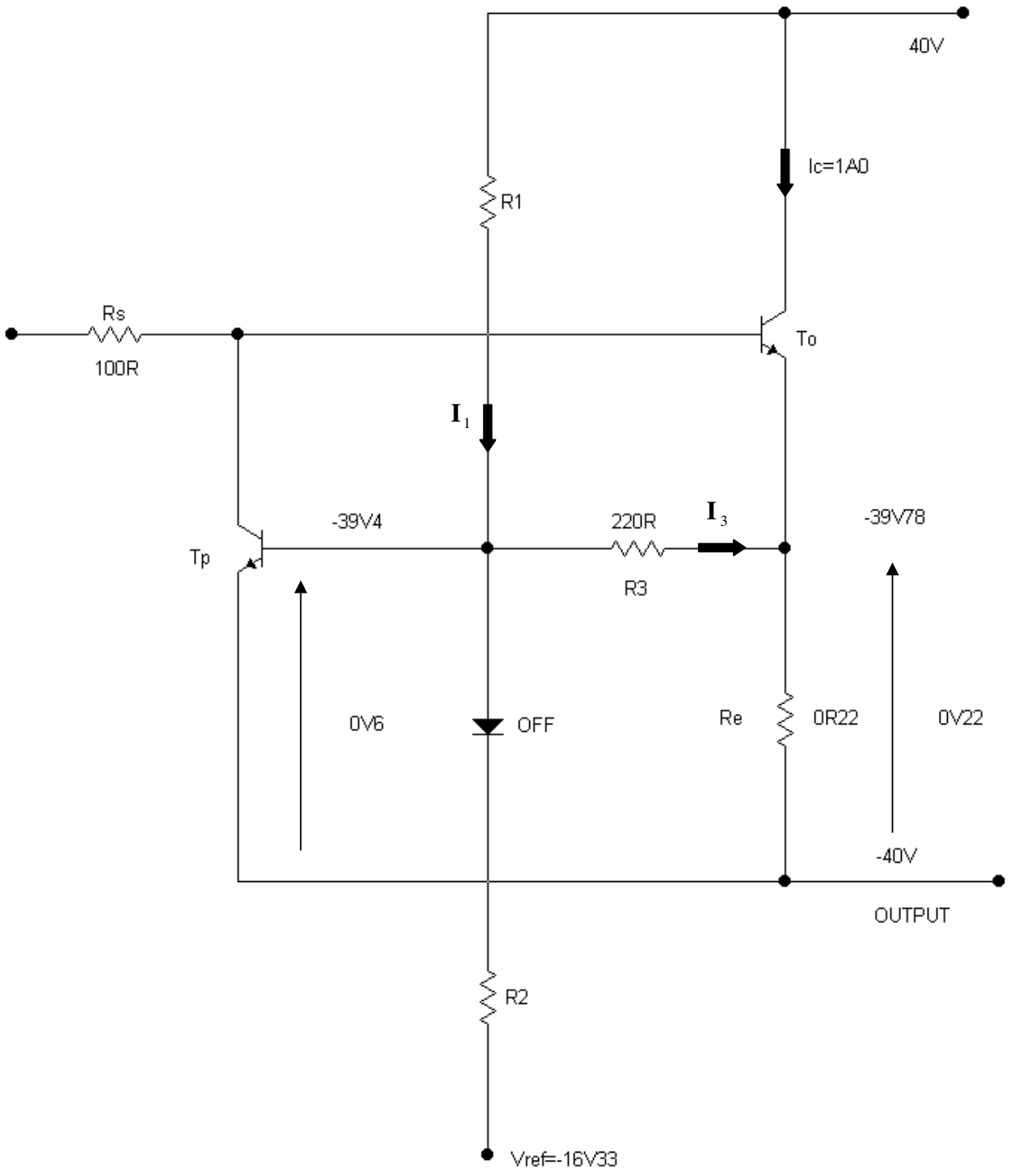

Fig. 37. Output conditions at point F on the protection locus in figure 32.

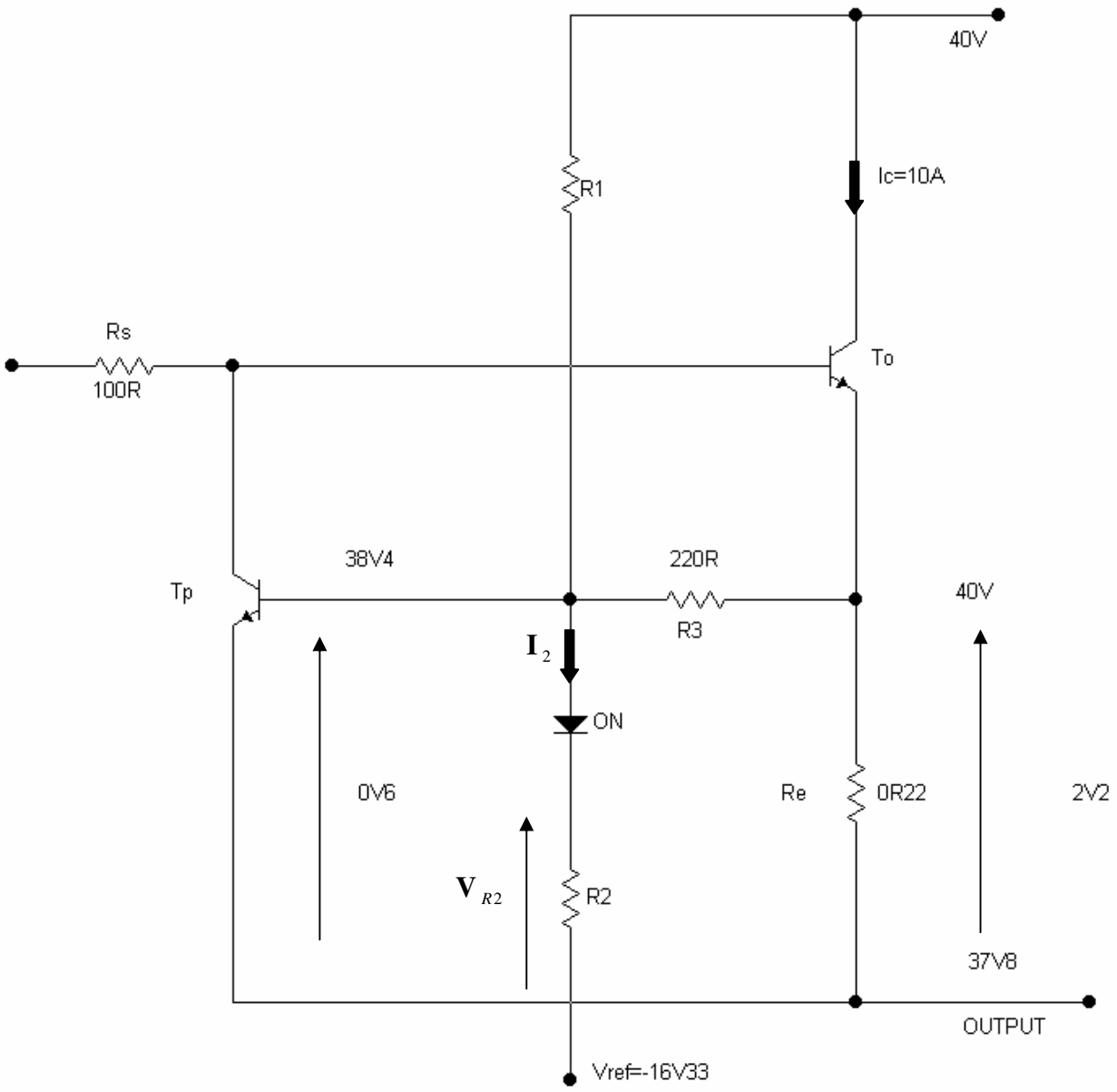

Fig. 38. Output conditions at point B on the protection locus in figure 32.

Complete independence from R_e of both segments of the dual slope protection locus described by the circuit in figure 35 can be accomplished by the introduction of a base-emitter resistor, R_2, (fig. 39), for each protection transistor. The result is in fact merely a union of the linear single slope scheme of figure 1, and the non-linear single slope circuit of figure 22.

The linear, single slope locus in figure 2 is reproduced in figure 40 as segment B-C-D, for which equations (1) and (3) are valid. Therefore, (fig. 41), with $R_3 = 220R$, then $R_1 = 12K4$, and $R_2 = 143R$. Resistor R_4 pulls the base of the protection transistor low as required for $\{0V \le V_{ce} \le 42V\}$, giving segment A-C.

The reference voltage is equal to the output voltage when $V_{ce} = 42V$, thus, $V_{\mathrm{Re}f1} = 40V - \{42V + (3A5 * 0R22)\} = -2V77$, and $V_{\mathrm{Re}f2} = +2V77$.

With reference to figure 41:

$$(I_2 + I_4) \approx (I_1 + I_3)$$

$\Rightarrow$

$$I_4 \approx (I_1 + I_3 - I_2)$$

$\Rightarrow$

$$I_4 = (40 - 37.96)/12K4 + (40 - 37.96)/220R - 0.6/143R$$

$\Rightarrow$

$$I_4 \approx 5.24mA$$

With $V_f \approx 0V6$,

$$R_4 = V_{R4}/I_4 = (37.96 - 0.6 + 2.77)/5.24mA$$

$\Rightarrow$

$$R_4 \approx 7K7$$

The flexibility of the scheme in figure 39 is significantly improved relative to figure 35. However such flexibility is easily surpassed by the network in figure 27, whose accuracy is not compromised by dependence on discreet value zener references.

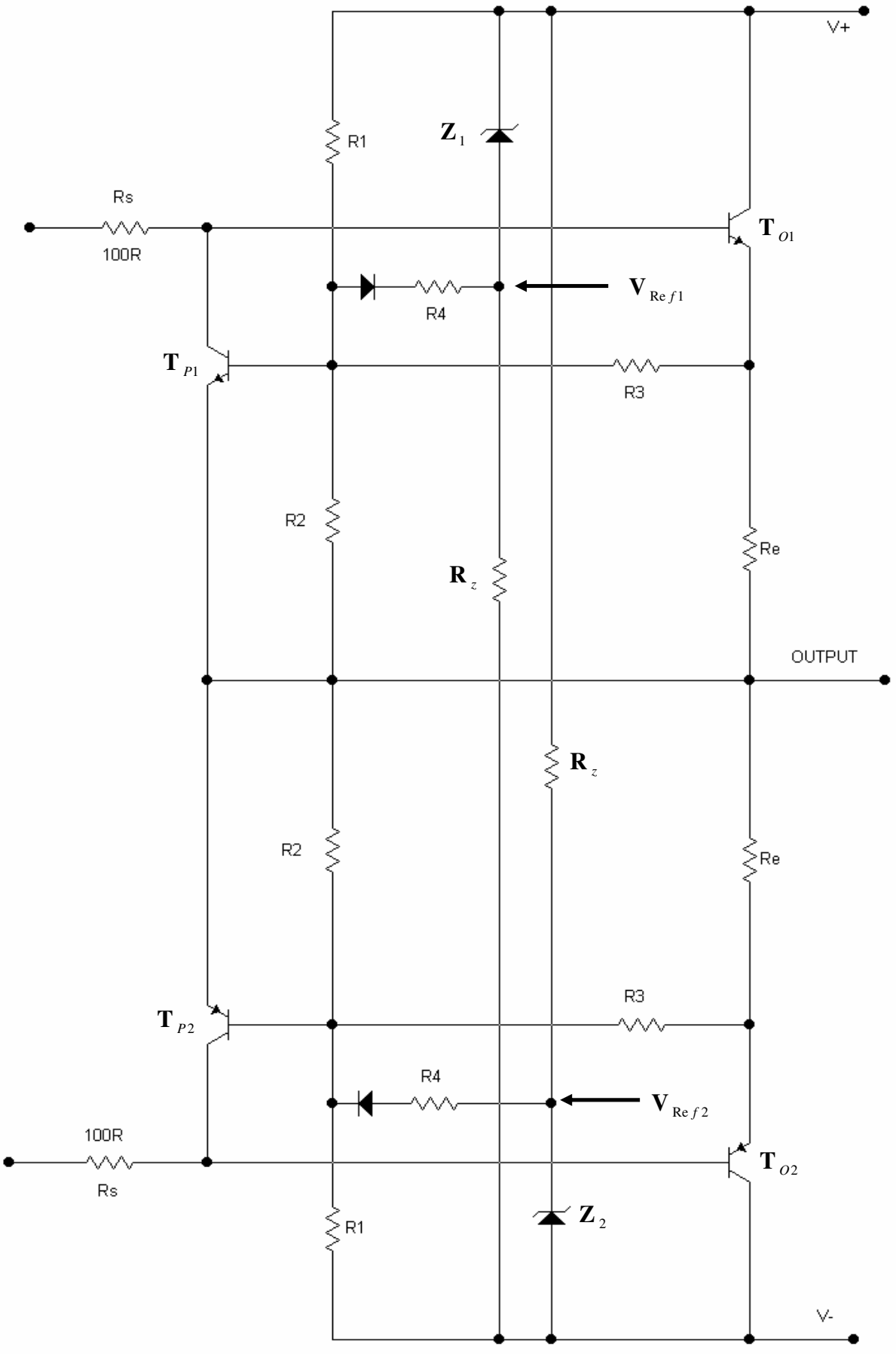

Fig. 39. Introducing resistor R_2 into the circuit of figure 35 permits placement of an arbitrary locus in the SOA, without undue dependence on the value of R_e.

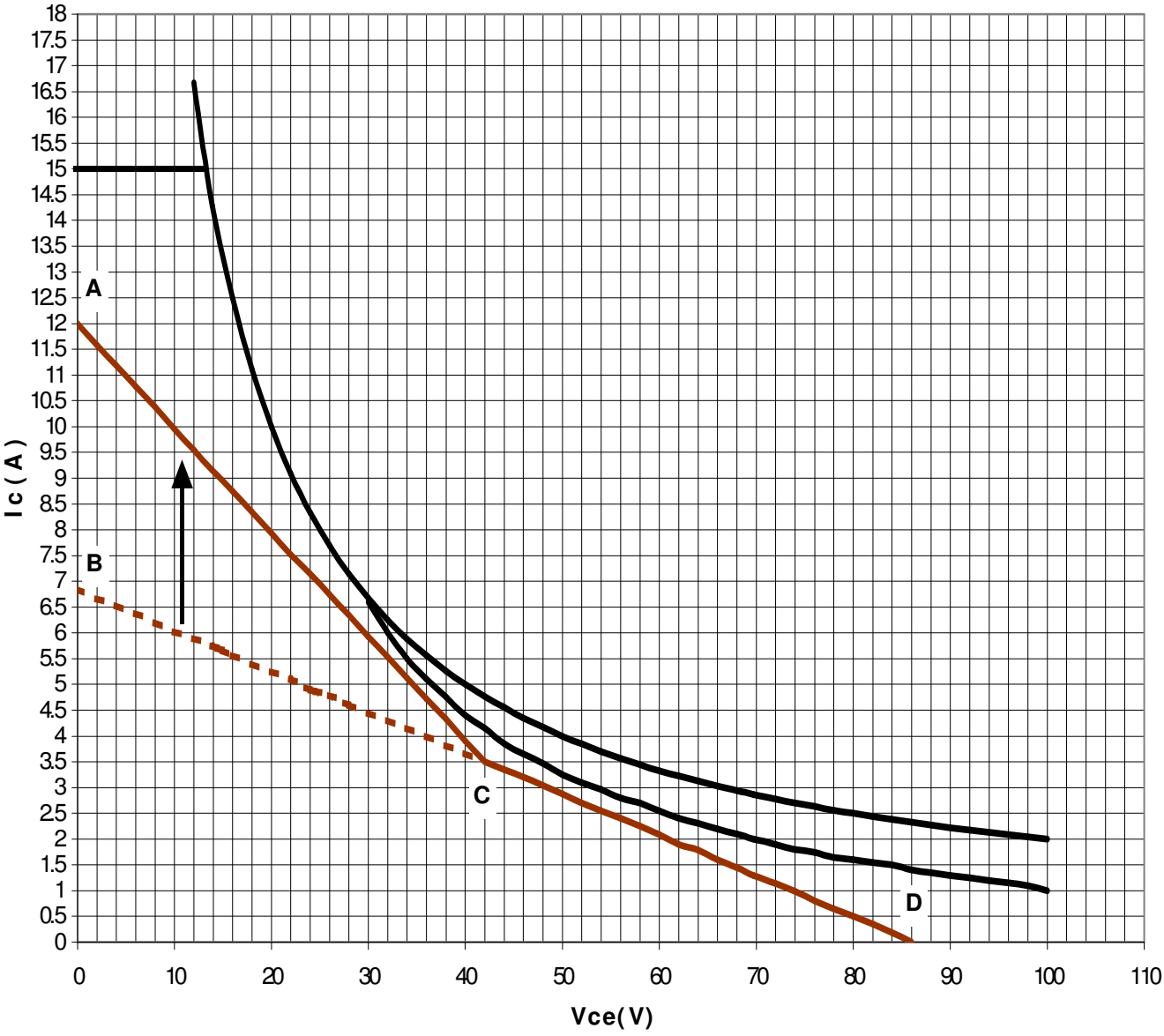

Fig. 40. Dual slope, single breakpoint protection locus described by the circuit of figure 39. Resistor R_4 modifies the linear single slope segment B-C-D, of figure 2 by effecting a vertical translation of segment B-C about point C.

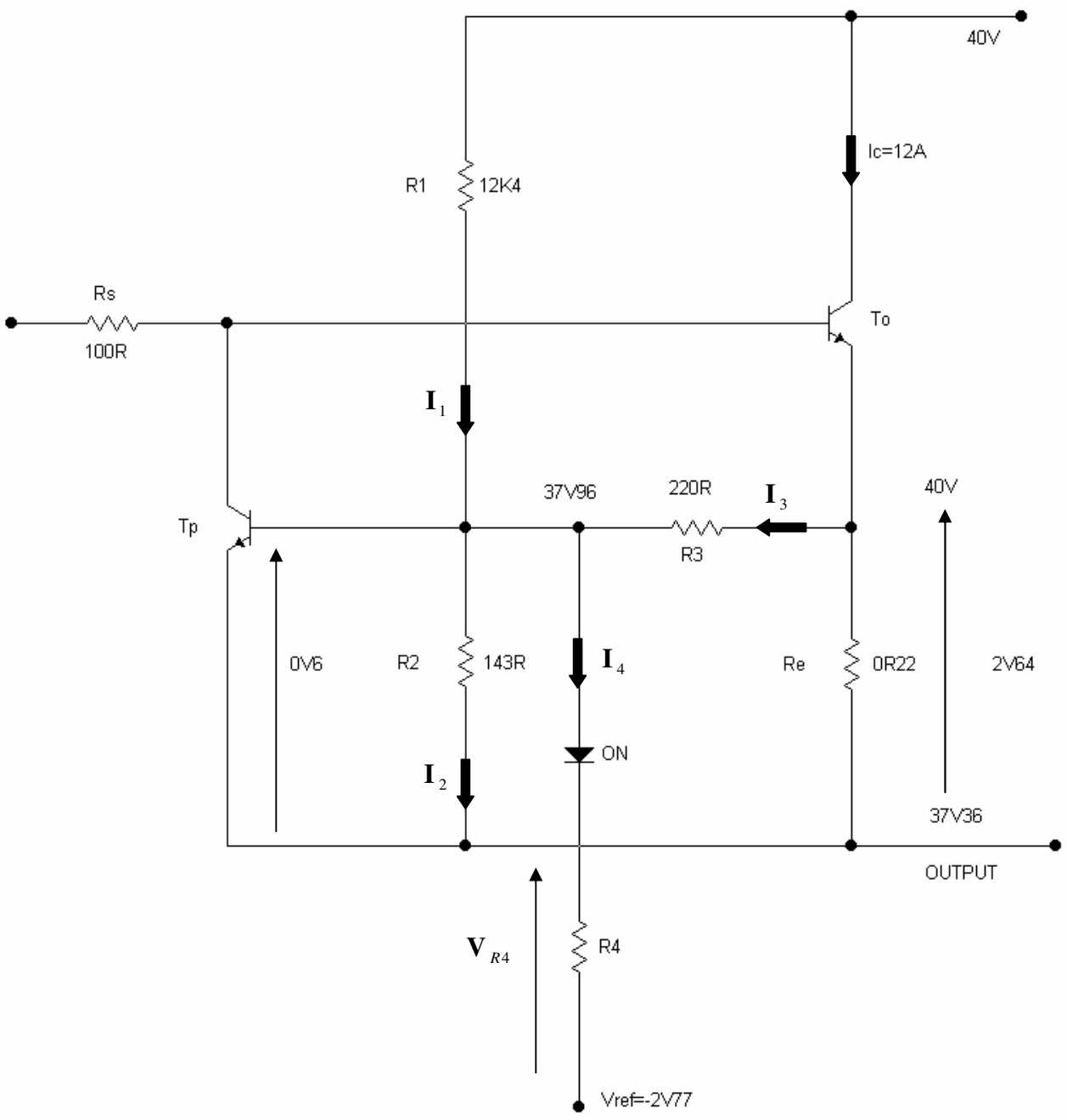

Fig. 41. Output conditions at point A on protection locus A-C-D in figure 40.

Treble slope, dual breakpoint, non-linear foldback limiting.

With modern power transistors and practical loudspeaker systems, an optimally located dual slope protection locus realized by the limiter in figure 27 can hardly be improved upon with respect to efficiency in the critical $\{|V_{cc}| \le V_{ce} < 2|V_{cc}|\}$ region.

However, for purely resistive laboratory loads with which a power amplifier's published specifications are obtained, the $\{0V \le V_{ce} \le |V_{cc}|\}$ region of the SOA is of primary interest, (fig. 10). In a competitive market place therefore, even when the truth of the matter is known, an amplifier designed to maintain its rated voltage swing across resistive loads of decreasing magnitude, (down to 1 ohm), without limiter intrusion, may be commercially rewarding. A suitably robust power supply and conservative thermal management are assumed.

To this end the treble slope design in figure 42 is presented. The circuit is a straightforward amalgam of the dual slope scheme of figure 27, and the single slope, single breakpoint network of figure 22. The circuit in figure 27 produces the dual slope characteristic B-D-F, (fig. 43), while resistor R_4 pulls the base of the protection transistor low as appropriate for $\{0V \le V_{ce} \le 42V\}$, giving segment A-C. Fifty-volt supply rails are assumed; a treble slope locus with $\pm 40V$ rails is vastly unnecessary.

The reference voltage is equal in magnitude to the output voltage, V_{out}, at breakpoint C, (fig. 43), i.e: $|V_{\mathrm{Re}f1}| = |V_{\mathrm{Re}f2}| = |V_{out}|_{V_{ce}=42V} = 7V23$, with $V_{\mathrm{Re}f1} = 7V23$, and $V_{\mathrm{Re}f2} = -7V23$. As previously established for figure 27, component values without R_d are calculated for segment B-D-E, (fig. 44, and 45), and the value of R_d established *in situ*, (fig. 46), using any convenient set of points along D-F. Resistor R_4 is then calculated for a nominal $V_{ce} = 0V$, at point A, (fig.47).

With reference to figure 44, let R_1=8K2, and $V_f \approx 0V6$ when I_d=1mA.

$\Rightarrow$

$$I_1 = I_d + I_2 + I_3 \tag{15}$$

And,

$$R_{2B} = \left(\frac{0.6}{0.44}\right) R_{2A} \tag{16}$$

From equation 15:

$$\frac{(50+11.4)}{8K2} = 1mA + \frac{0.44}{R_{2A}} + \frac{0.6}{R_3} \tag{17}$$

From figure 45, and invoking equation 16:

$$0.6 = \frac{1.474R_{2A}(0.6/0.44)}{R_{2A}(0.6/0.44) + R_{2A} + 8K2R_3/(8K2 + R_3)} \tag{18}$$

Solving (17) and (18) simultaneously:

$$R_3 \approx 160R7$$

$$R_{2A} \approx 159R8$$

$$R_{2B} = (0.6/0.44)R_{2A} \approx 217R9$$

With reference to figure 46:

$$I_2 = (0.6/R_{2B}) = (0.6/217R9) \approx 2.75mA$$

$\Rightarrow$

$$V_X = (I_2 R_{2A} - 49V4) \approx -48V96$$

$\Rightarrow$

$$V_{R3} = (V_X + 49V89) \approx 0V93$$

$\Rightarrow$

$$I_3 = (V_{R3}/R3) \approx 5.79mA$$

But,

$$I_d = I_1 - (I_2 + I_3) \tag{19}$$

Where,

$$I_1 = (40 - V_X)/8K2 \approx 10.85mA.$$

$\Rightarrow$

$$I_d = 10.85mA - (2.75mA + 5.79mA) \approx 2.31mA$$

$\Rightarrow$

$$R_d = (V_{Rd}/I_d) = (V_{R3} - 0.6)/I_d \approx 143R0$$

From figure 47:

$$R_4 = (V_{R4}/I_4) \tag{20}$$

Where:

$$I_4 = I_{2A} - I_{2B} \tag{21}$$

$\Rightarrow$

$$I_4 = \frac{(50 - 47.96)}{\{(R_1 // R_3) + R_{2A}\}} - \frac{0.6}{R_{2B}} \approx 3.67mA$$

$\Rightarrow$

$$R_4 = (47.96 - 7.23 - 0.6)/3.67mA \approx 10K9$$

A $(4\Omega \angle \pm 60^0)$ load driven to $\pm 50V$ rails requires $i_c \approx 9A5$ when $v_{ce} \approx 59V$, resulting in peak transistor dissipation, $p_{d(\max)} \approx 561W$. The treble slope protection locus of figure 43 allows 2A at $v_{ce} \approx 59V$ for a single complementary transistor pair. Therefore, five complementary pairs are required to drive a notional $(4\Omega \angle \pm 60^0)$ loudspeaker system from $\pm 50V$ supply rails without intrusive limiter activation.

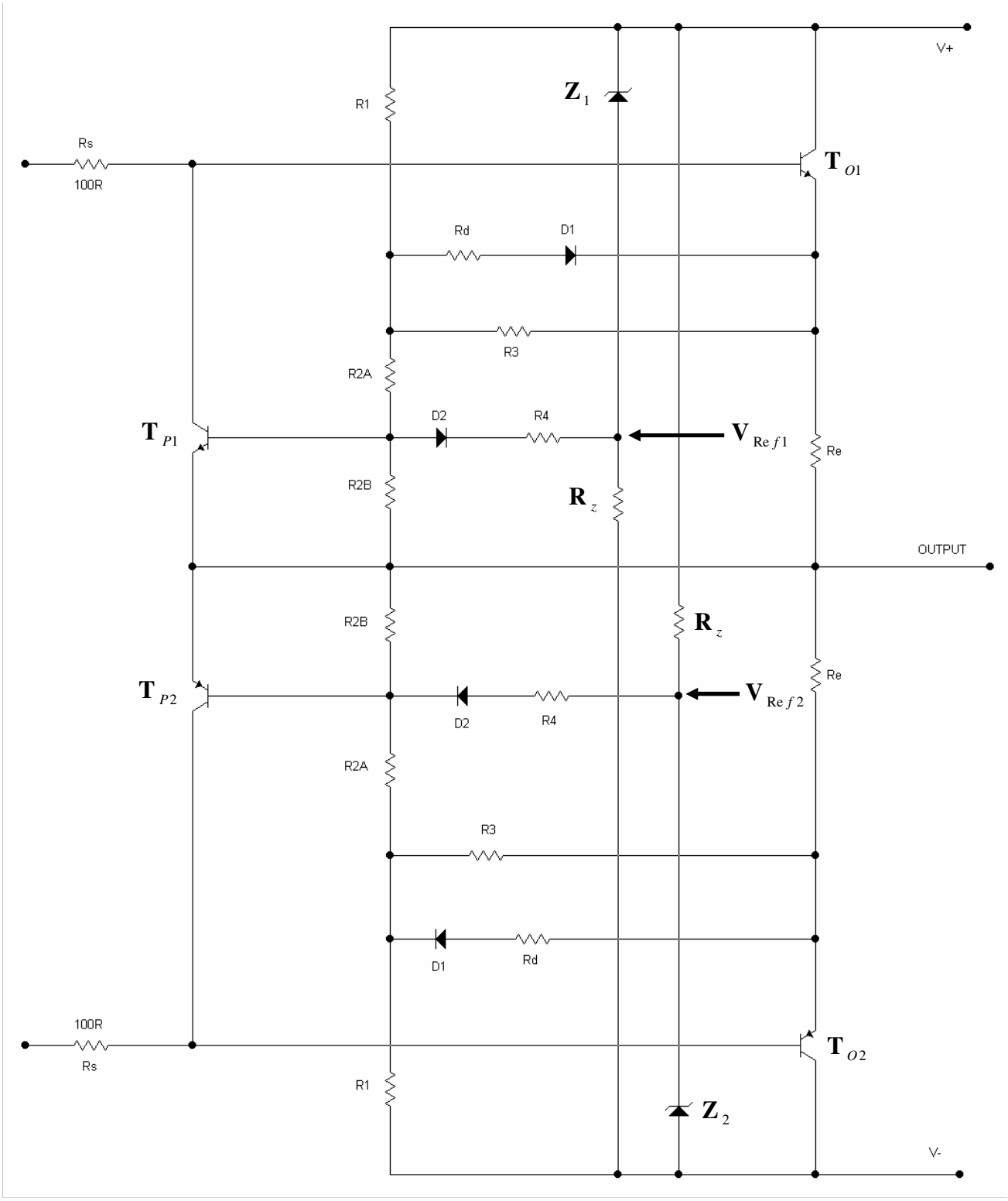

Fig. 42. Treble slope, dual breakpoint, non-linear foldback limiter.

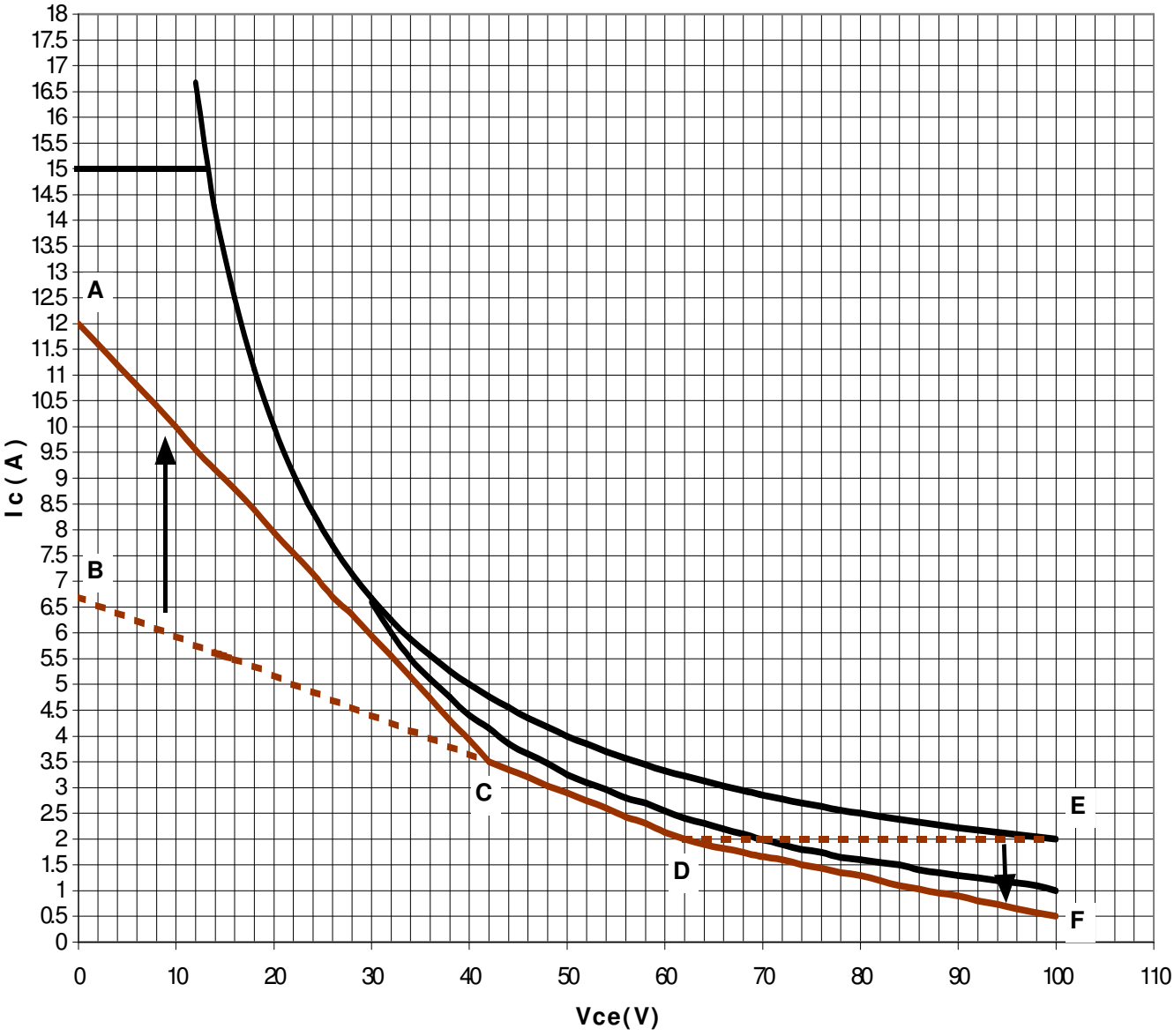

Fig. 43. Treble slope, dual breakpoint protection locus described by the circuit of figure 42. Resistor R_4 modifies the dual slope characteristic B-D-F by effecting a vertical translation of segment B-C about point C.

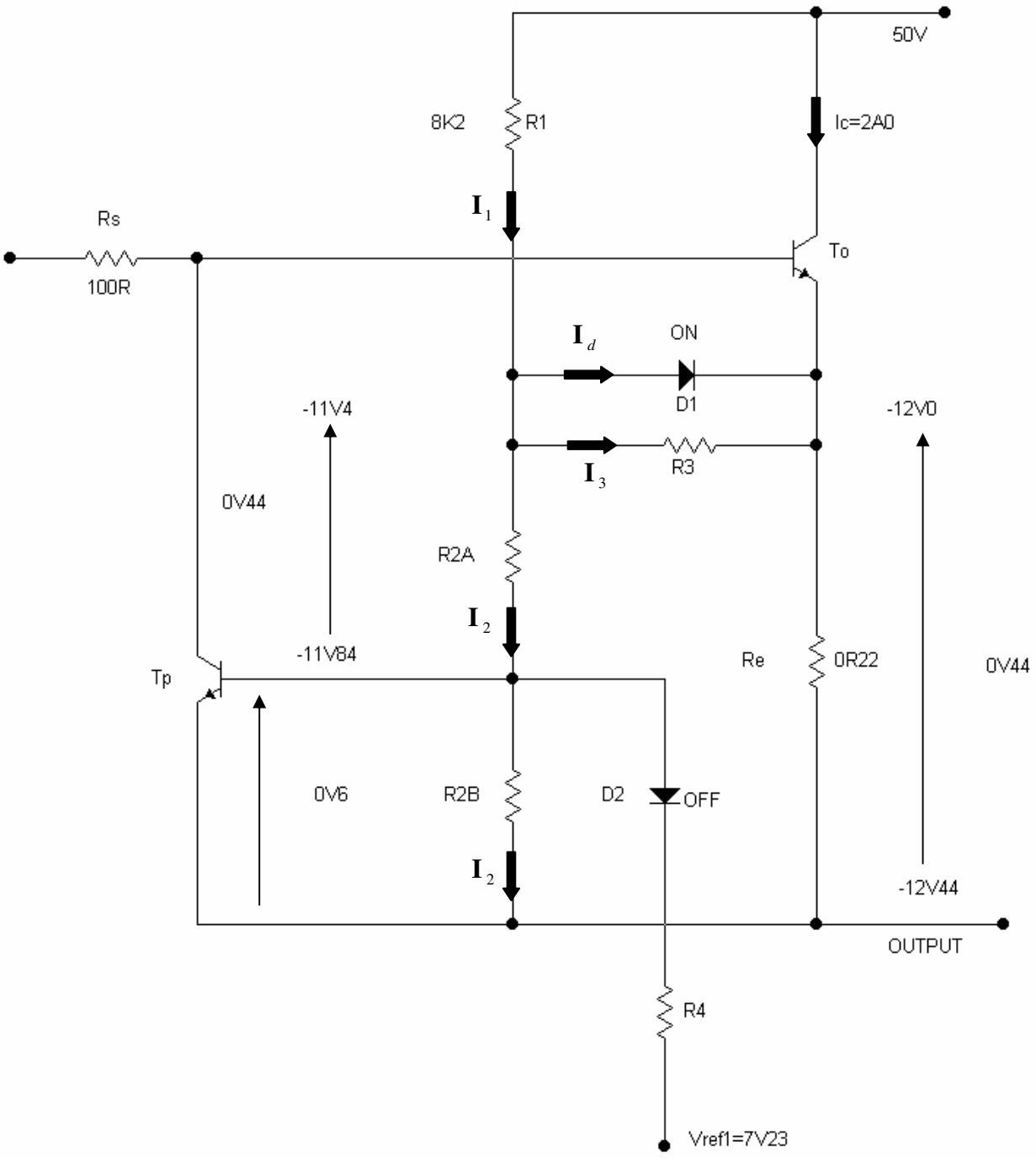

Fig. 44. Output conditions at point D on characteristic B-D-E in figure 43.

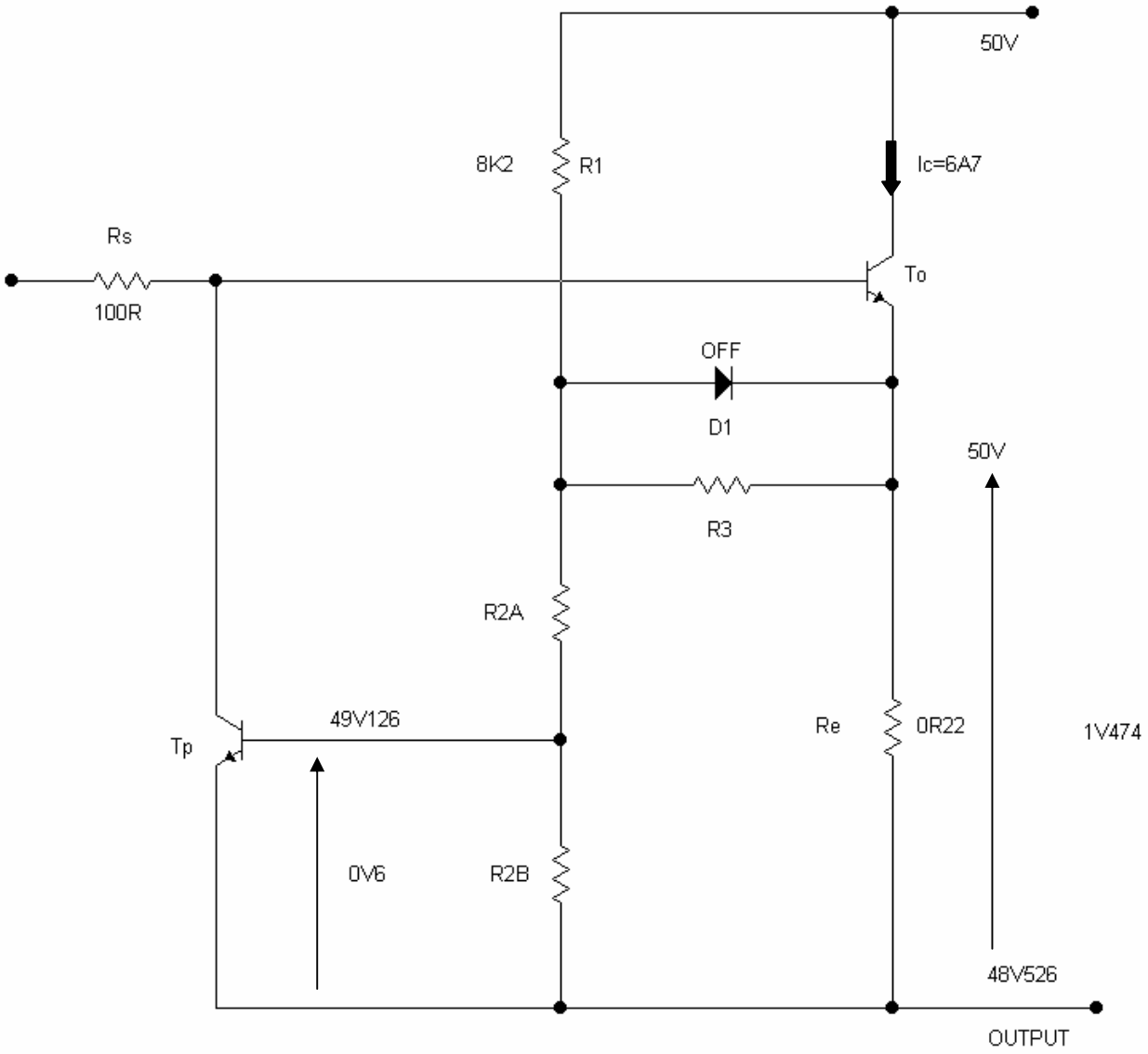

Fig. 45. Output conditions at point B on characteristic B-D-E in figure 43.

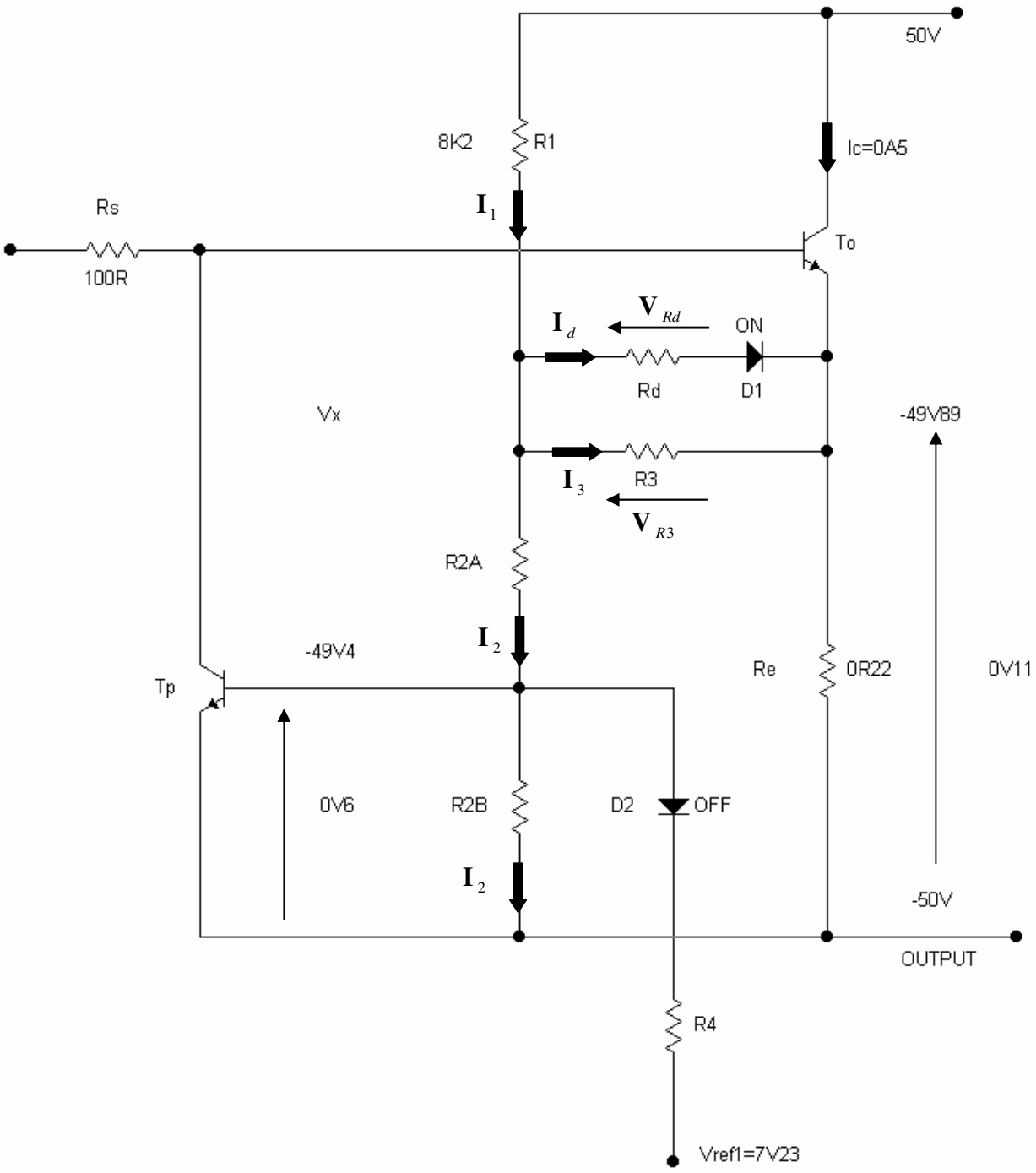

Fig. 46. Output conditions at point F on dual-slope characteristic B-D-F of figure 43.

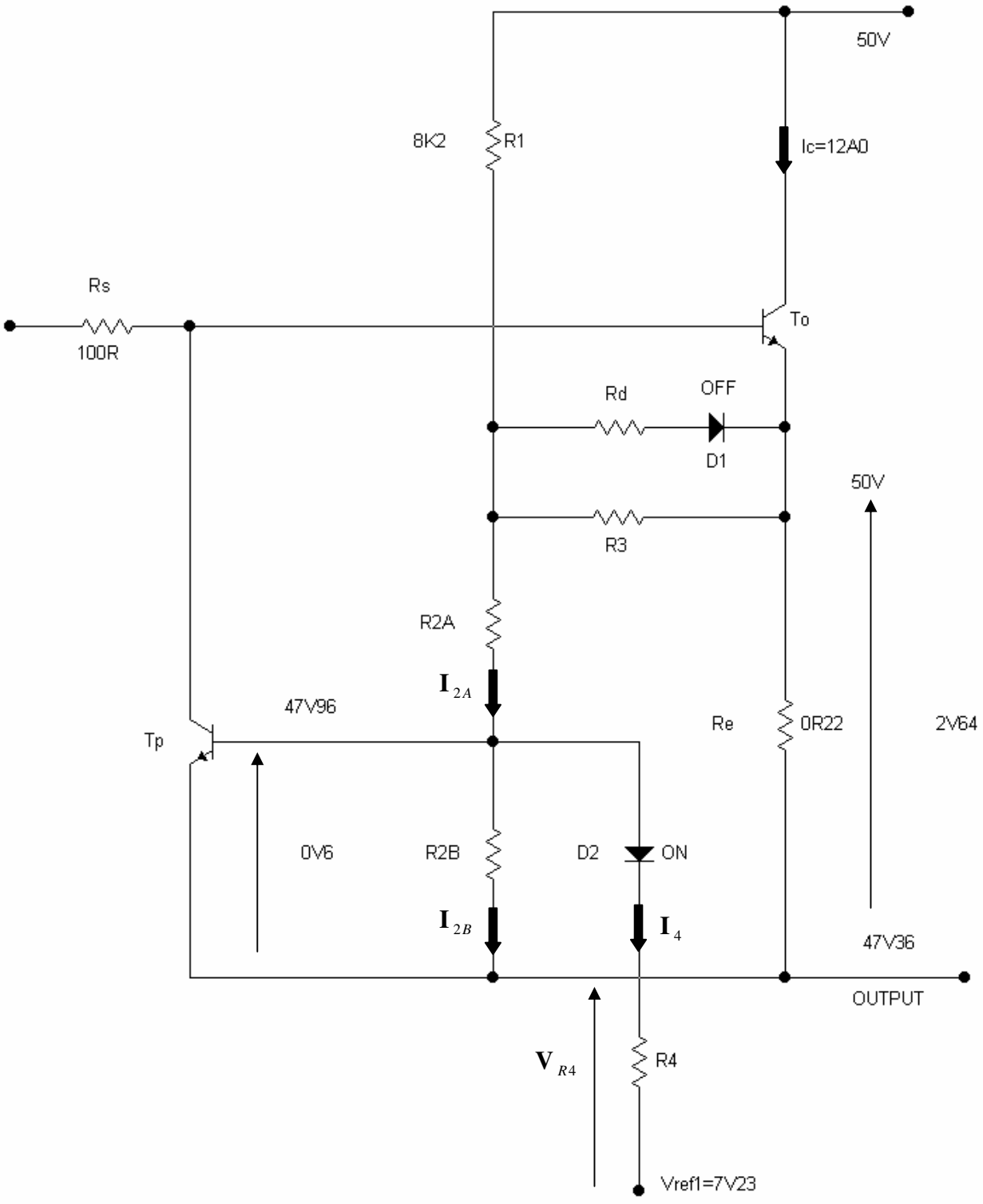

Fig. 47. Output conditions at point A on treble-slope protection locus, A-C-D-F, of figure 43.

The required reference voltage calls for a nominal 42V77 voltage drop across Z_1 and Z_2. As previously recommended the required voltage drop should be realized with multiple low-voltage devices, $(6V \le V_Z \le 12V)$, as a series combination of these should collectively posses a significantly lower series impedance than a single high voltage device. Thus in practice, Z_1 and Z_2 may each consist of five ZPD6.8RL, in series with a single ZPD8.2RL, biased at a nominal quiescent current of 10mA by R_z.

A more elegant, (if rather tedious), approach[22] compensates for variation in zener voltage drop with temperature. This calls for the introduction of typically two to four forward biased diodes in series with the zener diode. The decreasing voltage of the forward biased p-n junctions with increasing temperature, (negative temperature coefficient), tends to counteract the increase in zener voltage with increasing temperature, (positive temperature coefficient), and conversely. Therefore Z_1 and Z_2 may each consist of a series combination of three IN961B 10V zeners, a single ZPD8.2RL 8.2V device, and seven 1N4148 forward biased diodes.

For brevity perhaps, in place of Z_1 and Z_2, the shunt-feedback circuit of figure 48 may be used with a single, temperature compensated zener reference diode, such as the 6.2 volt 1N829A. This circuit permits the synthesis of a high voltage source without recourse to loose-tolerance, high voltage zener diodes, or indeed multiple small-value devices.

However, the variation in zener voltage drop due to current flactuation is invariably more significant than that due to change in temperature. Therefore where cost is no object, R_z may be replaced with a temperature compensated[11, pg.226.] current source/sink, (fig. 49), in the guise of an L.E.D-biased transistor, T_c.

The L.E.D's current limiting resistor, R_c, is split symmetrically into two components, R_{c1}, and R_{c2}, whose intersection[24] is decoupled by capacitor, C_{filter}, to the supply rail. The single-pole filter comprised of C_{filter} and R_{c1} across the L.E.D's internal resistance in series with R_{c2}, improves the regulation of the voltage drop across the L.E.D, by diminishing power supply ripple in the current established by R_{c1}, and R_{c2}. A time constant, $\tau_{filter} = C_{filter} R_{c1}$, of the order of two seconds is sufficient. Connecting C_{filter} directly across the L.E.D is sub-optimal, as a commensurately larger component would then be required for the same time constant. Resistor R_y minimises power dissipation in T_c; a collector-emitter voltage drop of the order of 20V for a collector current of 10mA should suffice with suitable small signal transistors, such as Motorola's 2N5551/2N5401.

Protecting paralleled complementary output transistors.

The emitter resistor, R_e, performes current-voltage conversion for the VI limiter, and promotes thermal stability by maintaining equable current distribution in a paralleled pair output stage. For this reason some designers suggest[1, pg.257.] it is only neccesary to monitor transistor current in a single complementary pair in a multiple pair output stage.

Alternatively, the calculated value of the current sensing resistor, R_3, for a single complementary transistor pair is multiplied by the number, *N*, of paralleled output pairs, with each resistor of value $N.R_3$, used to monitor the current in each transistor as shown in figure 50. Note that using the non-linear limiter of figure 27 in this fashion requires that each resistor of value $N.R_3$ be shunted by a diode in series with a resistor of value $N.R_d$.

An obvious disadvantage inherent in both schemes is that the open-circuit failure of a rogue transistor in one half of the output stage could result in the disastrous alteration of the protectection locus for the remaining devices in that section. With modern power transistors however, this scenerio is unlikely to materialise. The use of an independent V-I limiter for each complementary pair would eliminate this flaw, but is financially indefensible for most commercial designs.

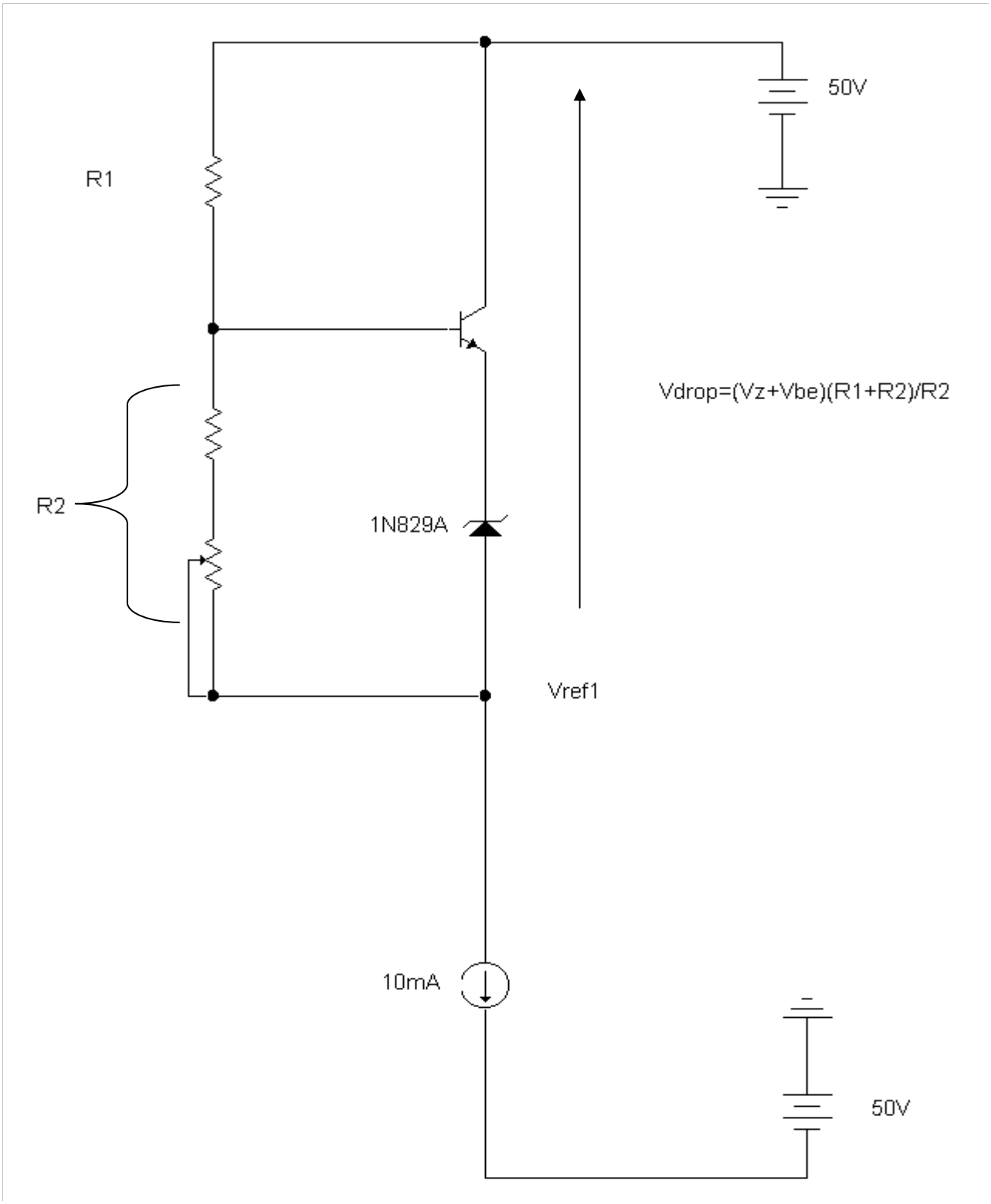

Fig. 48. Shunt feedback voltage generator may be used in place of Z_1 and Z_2, to circumvent the tedium of selecting multiple diodes.

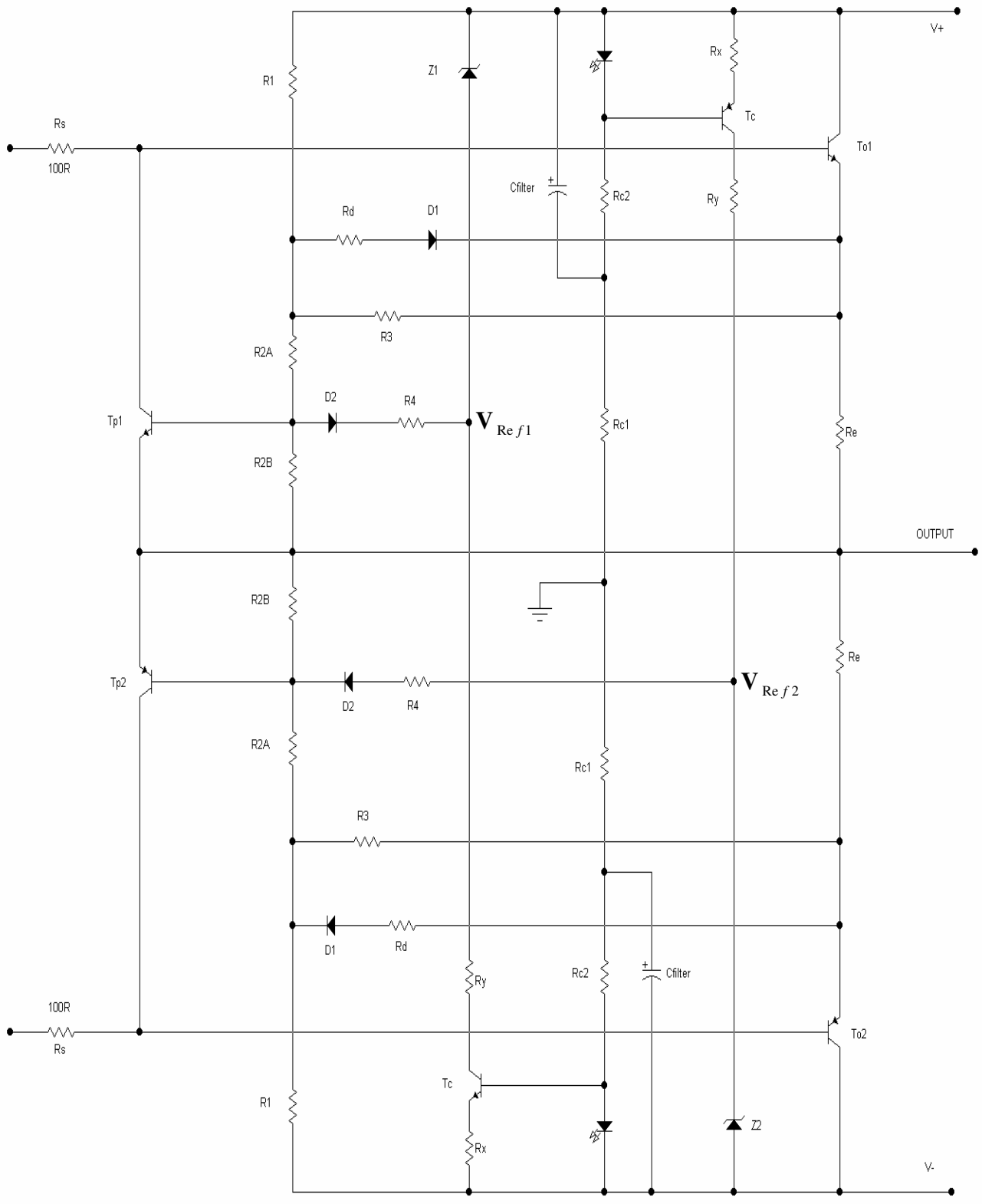

Fig. 49. Treble-slope, dual breakpoint limiter of figure 42, with improved regulation of zener voltage, V_Z, by means of a temperature compensated current source/sink. Such regulation is further enhanced by the introduction of a measure of temperature compensation to Z_1 and Z_2.

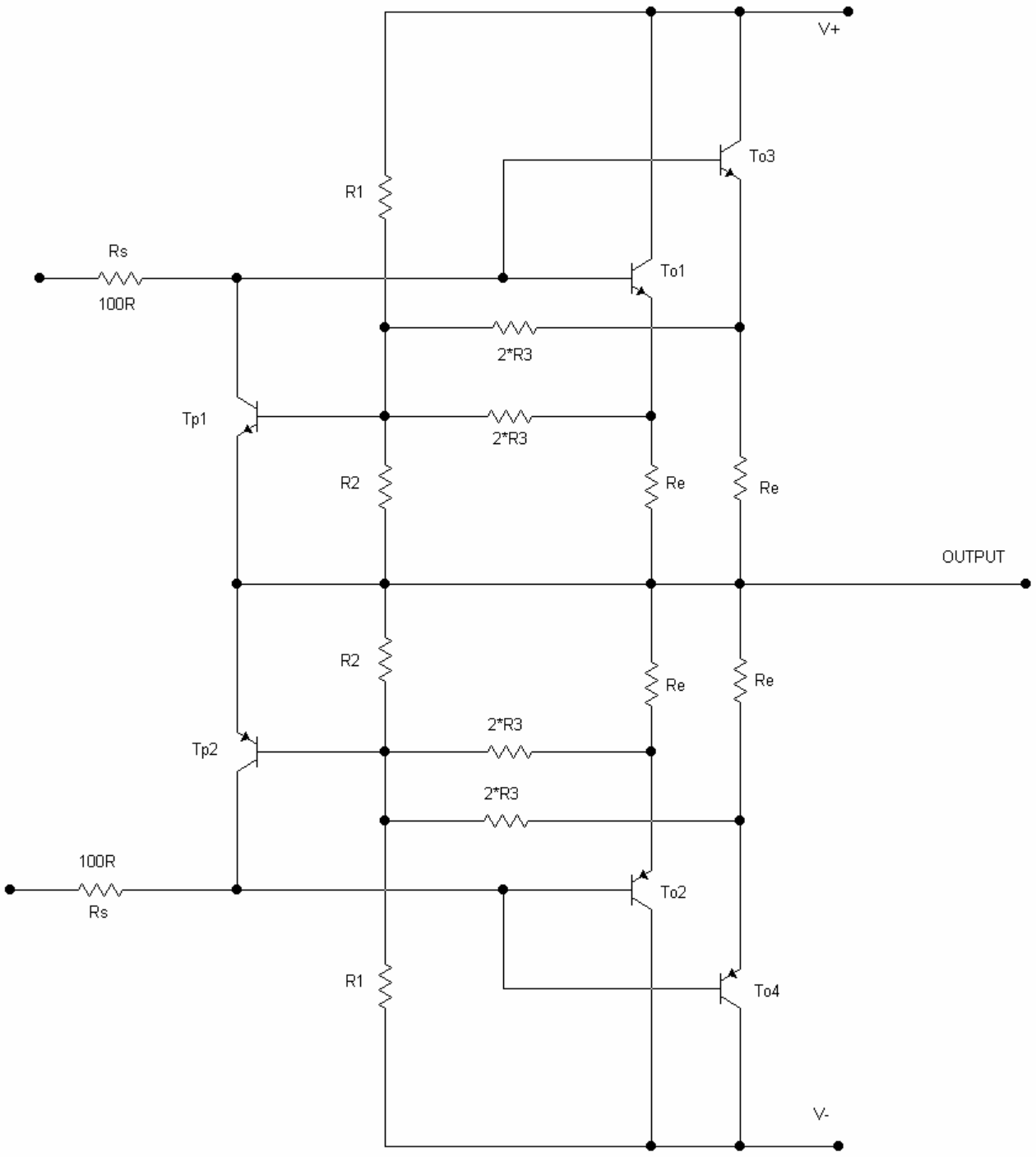

Fig. 50. In this single-slope, linear foldback scheme, voltage signals from multiple current sensing resistors are summed algebraically at the base of the protection transistor.

Conclusion.

On grounds of safety and reliability, it is firmly recommended that all linear, complementary semi-conductor audio power amplifiers incorporate suitable V-I protection. The aversion cultivated by some designers to such is here shown to be wholly illusory. A competently designed V-I limiter will remain demonstrably inert, and therefore completely unobtrusive with virtually all commercial loudspeaker systems, provided the output stage consists of sufficient complementary transistors to safely drive a $\left(4\Omega\angle\pm 60^{0}\right)$ load to the supply rails.

The dual slope circuit of figure 27 represents a significant improvement in efficient SOA utilization relative to the single slope topology of figure 1, with no significant penalty with regard to algebraic complexity. It's characteristic locus, (fig. 26), can be readily optimized to accommodate $\pm 50V$, supply rails with MJL3281A/MJL1302A, transistors. Higher supply rails are not recommended for worst-case reactive loads, as available collector current for these devices falls rapidly below 0A5 for $V_{CE} > 100V$.

Although e-MOSFETs are at least an order of magnitude less linear than bipolar transistors[11, pg.273.], they provide significantly greater scope for reliable design at high device voltages, $\left(2\left|V_{Supply}\right| >> 100V\right)$, with the promise of even greater efficiency in SOA utilization, due to the absence of secondary breakdown. However, there is no need to endure the indignity of e-MOSFET non-linearity, and on-resistance voltage inefficiency in sub-200W into 8Ω designs.

More elaborate protection schemes are possible, with the use of as many diodes as the number of required breakpoints. However the increase in available current in the high voltage region, $\left\{\left|V_{cc}\right| \le V_{ce} < 2\left|V_{cc}\right|\right\}$, where it counts with respect to reactive load drive, is negligible in relation to the circuit complexity thus engendered.

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