Lynx D48 DAC module

For several years in the market of integrated DAC chips are presented products of ESS Technology. DAC chips of this company has very high claimed parameters and versatility. It is known that the DAC of ESS Technology used in various products of the companies like Accuphase, McIntosh, Audiolab, Simaudio, Perreaux, Oppo and in a number of other manufacturers. And the results are very different, at least from what happened to listen, I managed to conclude only one thing - the potential ES9018 / 9012 chipset is quite high, but its implementation has some significant difficulties to overcome that are far from all. This conclusion was confirmed too by familiarity with the production of company Twisted Pear Audio - Buffalo DAC in different versions executed based on ES9008 and ES9018 chips. Unfortunately, developers of that DACs could not get any serious sound results, and their products are use only the simplest functions of ES9008 / 9018 chips. Crafts Chinese farmers are not considered at all - regardless of the type of application components (!) and circuitry (!), their sound subjectively the same boring, unnatural - clamped and does not cause any emoytsy except of wishing to turn off this mess quickly... However, this is defenitely another and big topic ...

To answer the question about the appropriateness of chips ESS Technology for high-quality audio equipment, I decided to make a mockup version of the DAC ES9018. But almost immediately I ran into difficulties not technical but administrative. As it turned out the ES9018 datasheet freely is not available. To get the necessary information, NDA needed to be signed with the representative of the manufacturer company. In the end - all problems has been solved, and I became the owner of the data required and the chips themselves was acquired from Ismosys (http://www.ismosys.com).

From received materials it was immediately clear what the main problem of using the DAC from ESS Technology: a very high output current of the inverter. Dual current amplitude at the output of each channel of eight is about 4mA. That means when operating in dual channel mode (with the summation current of 4 DAC' outputs per channel) we have 16 mA! This means that to obtain a 3 voltage of amplitude at the output of the subtractor (since differential outputs - they must be used carefully in pairs), the inverter current - voltage feedback resistance will have to use about 200 ohms (passive transducers I do not see because of the failure to provide the required accuracy and quality of the conversion). That is, the OpAmp is loaded converter output resistance of the same order - 200 ohms or less (considering the resistance of the external circuits connected to the output). And with such a load impedance the converter must provide a level of its own distortion at least not higher than stated for the DAC chip, ie -120dB. Thus it is desirable to implementation of the scheme would be the sane size, complexity and power consumption. The challenge, though not extremely complicated, but it requires careful approach and selection of possible solutions. In addition, it was found that the DAC ES9018 has a rather complex management and a variety of settable parameters, and all modes of management is provided only on I²C bus, and "efault" setting is not in all cases are optimal. This uniquely determines the application of the control of the microcontroller as the control DAC chip and receiving from it a flow of curent parameter data for further use in display systems.

To study the properties of circuits and debug the controller program I developed an experimental board with the code name Lynx D48V1, which worked out the schematics of current – voltage converter, power supplies, tried out various options of used components and performed initial debugging control of the ES9018 chip itself. The first experiments showed that received from ESS Technology datasheet riddled with errors. Some data on the contents of internal registers do not correspond to reality, the values of the minimum clock frequency (relative to the sampling frequency) proved unreliable. I had to spend a lot of time and effort to compile accurate DAC control registers and identification cards admissible values clock frequency boundaries. After addressing these pressing issues (further work with a chip would have been impossible without such approach) it's time to experiment with chip' environment. Almost immediately it became clear that the operation at voltage output mode can not claim as a high-quality sound (in fact, it is a raw test for "works / not works"), and the only real mode of high quality is the current output mode. To work with current output have been tried several different active current-voltage converter circuits (on the powerful OPA654, AD842, on the composite amplifier AD8610 + AD811, on the OpAmp with
a source of high-power output (OpAmp + KP601) and emitter (OpAmp + 2SC3421) and a repeater on a discrete amplifier with an input stage with a common base). As a result of the comparison both the objective parameters (level of harmonic distortion of the spectral composition, the level of difference tones for dual frequency signal) and subjective properties (overall quality and naturalness of sound at

different musical material) I have concluded that in general the best properties was from active current-voltage converter on the OpAmp AD744, single-ended buffered by emitter follower output with a large quiescent current - the order of 25 ... 30 mA. JFET source follower type KP601 KP903 produced more distortion on the second and fourth harmonics at the resistors in the feedback-circuit below the 300 ... 350 ohms. Slightly worse (in this case) result showed similar cascades of OpAmps type OP42, AD845 and LT1122, as well as high-power OpAmp AD842. Received from a Chinese supplier Utsource IC OPA654 worth more than $ 200 apiece were crappy Chinese fakes, worked very badly and differently each of the three ordered, and as a result were dismantled (three were different in appearance crystals!) and thrown away. As the final version was adopted the converter on AD744 and repeater with active load transistors 2SC3421. Thus regular own output stage output (pin 6) is used in the OpAmp, and the transistors operate with a quiescent current of the order of 30mA and are at the most linear position of specifications. Such a scheme provides a "given" to the output of op-amp load resistance not less than 20 kohms, and accordingly, extremely low distortion amplifier. Generally, from the point of view of their own distortions and the input resistance to high-frequency components, AD744 proved to be exceptionally good, and deservedly found themselves in this application the best.

A similar situation happened with the OpAmp in the filter - subtracter. The most successful was the devices LT1122, AD744 and OP42, slightly worse - LT1468, AD845, OPA827 and ADA4627. Since the output of the subtractor is the output of the DAC, it is also subject to buffering. In the prototyping embodiment subtractor buffer was made in a similar buffer inverters I/U, and in a working embodiment, a transistor follower was replaced by BUF03, and (taking into account the small and sufficient linear input buffer capacity) output signal of AD744 is taken from the output of the voltage amplifier (pin 5) but it provided the possibility of withdrawing from a normal signal, and output circuits (output 6).

During the experiments it was found that the ES9018 is very sensitive to the quality of power modulators. Briefly, it was mentioned in the branded materials on the use of the earlier chip ES9008, but no major recommendations on this issue has not been given. As a result, after a series of experiments and comparisons for the DAC modulators power were used low-noise High Linearity stabilizers structure VoltageReference-NoiseFilter-OpAmp (separate for each of the halves of the DAC chip) similar stabilizers used to supply critical analog circuit and the clock generators with low phase noise.

After multiple adjustments and resolderings component in a process of working with breadboard, it fell into disrepair, and, taking into account the results obtained has been designed and constructed the second version - Lynx D48V2. Since the analog part and the power, in general have been worked out and optimized, the second version served as a testing ground for digital part and timing. As I mentioned above, ES9018 chips have enough strict requirements for the minimum value of the clock frequency. Thus, in the SPDIF inputs of operation, according to the datasheet, the clock frequency must exceed the 386Fs, i.e. if we want to stably receive stream 192 khz, the masterclock should exceed 74,112 MHz. And this is where the problems started. Firstly, ES9018 generally refused to work with 192-kHz stream at frequency 74,115 MHz of masterclock (I originally thought that there is a significant deviation of the clock frequency generator test flow upwards, but the exact frequency measurement showed that the reference frequency is 36.863922 MHz that is different from the ideal value by 0.0002% only). Setting the DAC generator to a frequency of 80 MHz seems solved the problem, but the reception and decoding of the data obtained unstable, with failures and a sharp increase in the level of distortion. Changing the capture range of parameters and keeping the internal PLL, conversion factors forming the counters, and other actions to all possible DAC settings was not gives practically any results. Only the installation of the generator to the frequency of 85 MHz, has completely solved this problem. It should be noted that the effect is practically the same at different instances of the chip including different years of release, ie this is kind of a system error, and not a random defect in a single chip.

After the SPDIF receiver debugging it is time for the synchronous inputs. In the network, I almost did not see the applications ES9008 / 9018 in this mode - all the designs, both industrial and amateur, the same type used the most primitive Buffalo asynchronous mode with SPDIF input. In ES9018 datasheet indicated that the minimum frequency generators when operating in synchronous mode should be higher than 192Fs, i.e. for 192kHz - at least not less than 36,864 MHz. Being taught by bitter experience with high-priced generators for SPDIF mode, I decided not to risk and immediately ordered the generators for frequencies 45.1584 MHz and 49,152 MHz. It must be said that this decision was absolutely correct - because the trial installation of generators at 33.8688 MHz and 36,864 MHz DACs (in synchronous mode for I2S) leaded to refuse working with sampling rates of 176.4 kHz and 192 kHz, respectively. And, again, any changes in DAC internal system settings basically changed nothing. In experiments with generators switching revealed that for ES9018 a continuous clock signal required. Its loss of even a few cycles, followed by reduction often leads to "freeze" the chip and to inoperability of the hardware reset. As it turned out, at the ES9018 has an interesting property - it automatically and "silently" goes into the asynchronous mode when the clock frequency is not multiple to the input sampling. Basically, it allows you to do just one generator at a frequency of 85 ... 100 MHz, but the sound quality will be slightly worse than achievable in the synchronous mode and PLL mode setting may be required for stable operation.

On the board of a second version was made debugging of a program controlled by a microcontroller and an FPGA project for switching and synchronous coordination of inputs, as well as the comparator signals SPDIF receivers. This board was almost completely the finished development. Appearance of the assebled second version is shown in Figure 1:

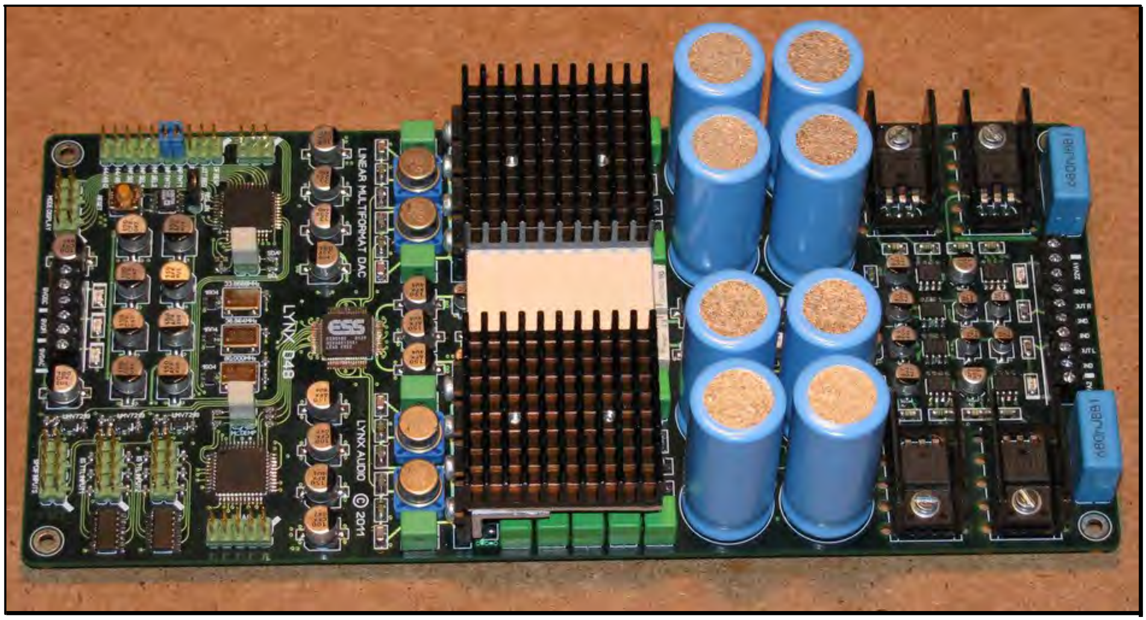

Fig. 1 Experimental board DAC Lynx D48 of the second version

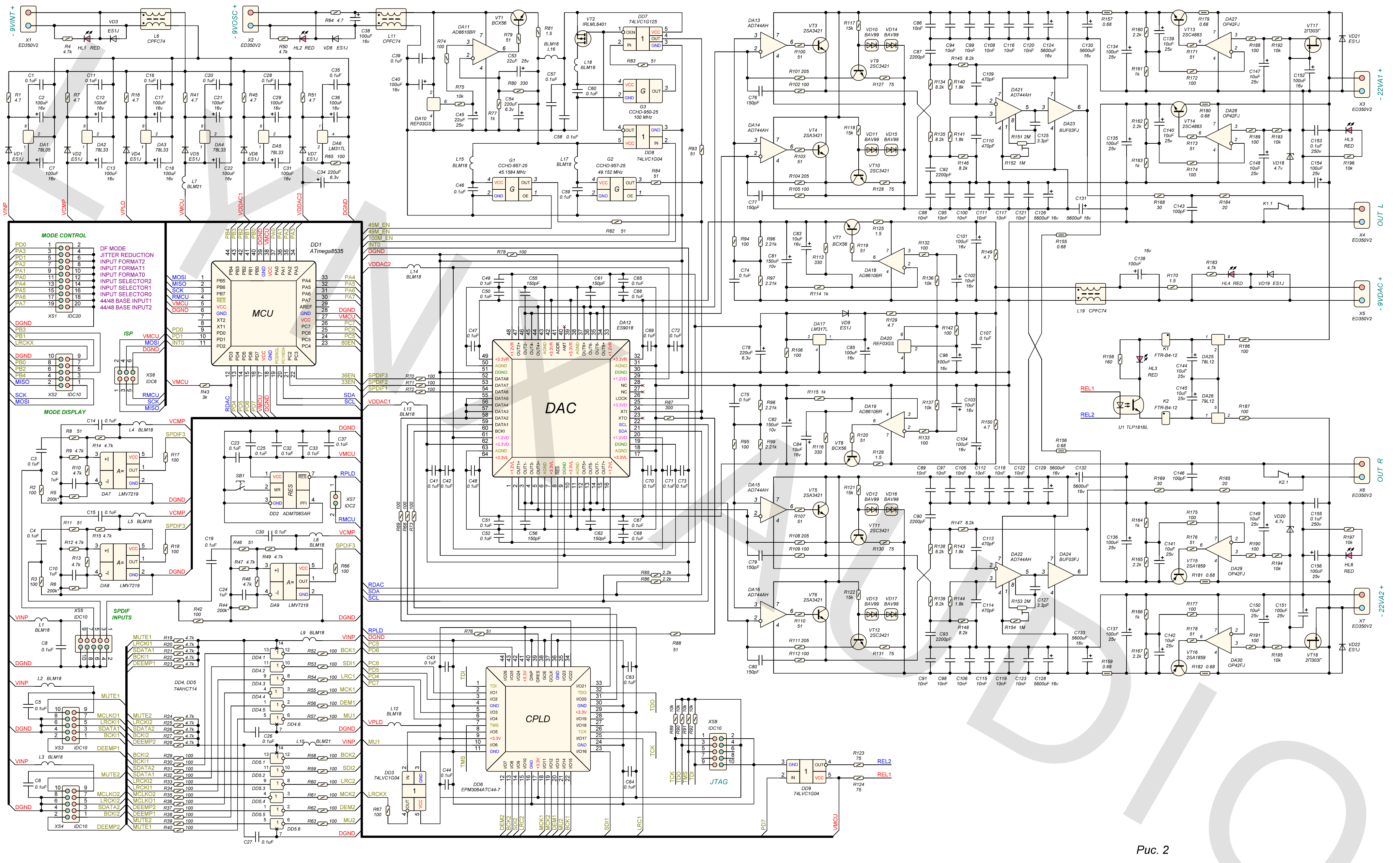

Рис. 2

LYNX AUDIO

LOW DISTORTION DAC LYNX D48V3

05.02.2013

Buffer emitter followers in total dissipate heat output of about 6 watts, and to provide the acceptable board components temperature was possible only by setting the transistors in a cooler with a sufficiently large surface area. Five independent sources are used for the DAC power supply, three of 9V and two of about 20 ... 24V. Stabilizers of digital feeds implemented on integrated voltage regulators 78L33, 78L05 and LM317L, stabilizers of power clock generators, analog part of the DAC chip and afterDAC OpAmps - discrete low noise.

With all of the identified problems and errors in the second version of the DAC, has designed and manufactured a third version, a schematic diagram is shown in Figure 2. The main differences from the second version are: BUF03 used as an output buffer instead of the emitter follower, the use of low-noise generators of Crystek types CCHD950 (100MHz, for operation with inputs SPDIF-) and CCHD957 (45.1584 MHz and 49,152 MHz - for synchronous inputs, to clock the flow rate of the data t source their frequency is divided by 2 in FPGA)), a different organization of the analog power circuits, the use of a sector of earth complex polygon for division and allocation of the common wire currents. It is also important differences in the control program of the controller. View of DAC Lynx D48V3 board is shown in Figure 3. In all versions of the device it is used four-layer printed circuit boards that have no fundamental flaws fatal single- and dual-layer boards. The application of MLB allows to create an optimal topology of the land, signal and power circuits with a minimum of interference and to realize the full shielding of clock circuits, thereby protecting clock circuits with low phase noise from external noise, and dramatically reduce the level of RF interference from these signals to the analog circuit, and also realize transmission of clock signals on lines consistent with a normalized characteristic impedance.

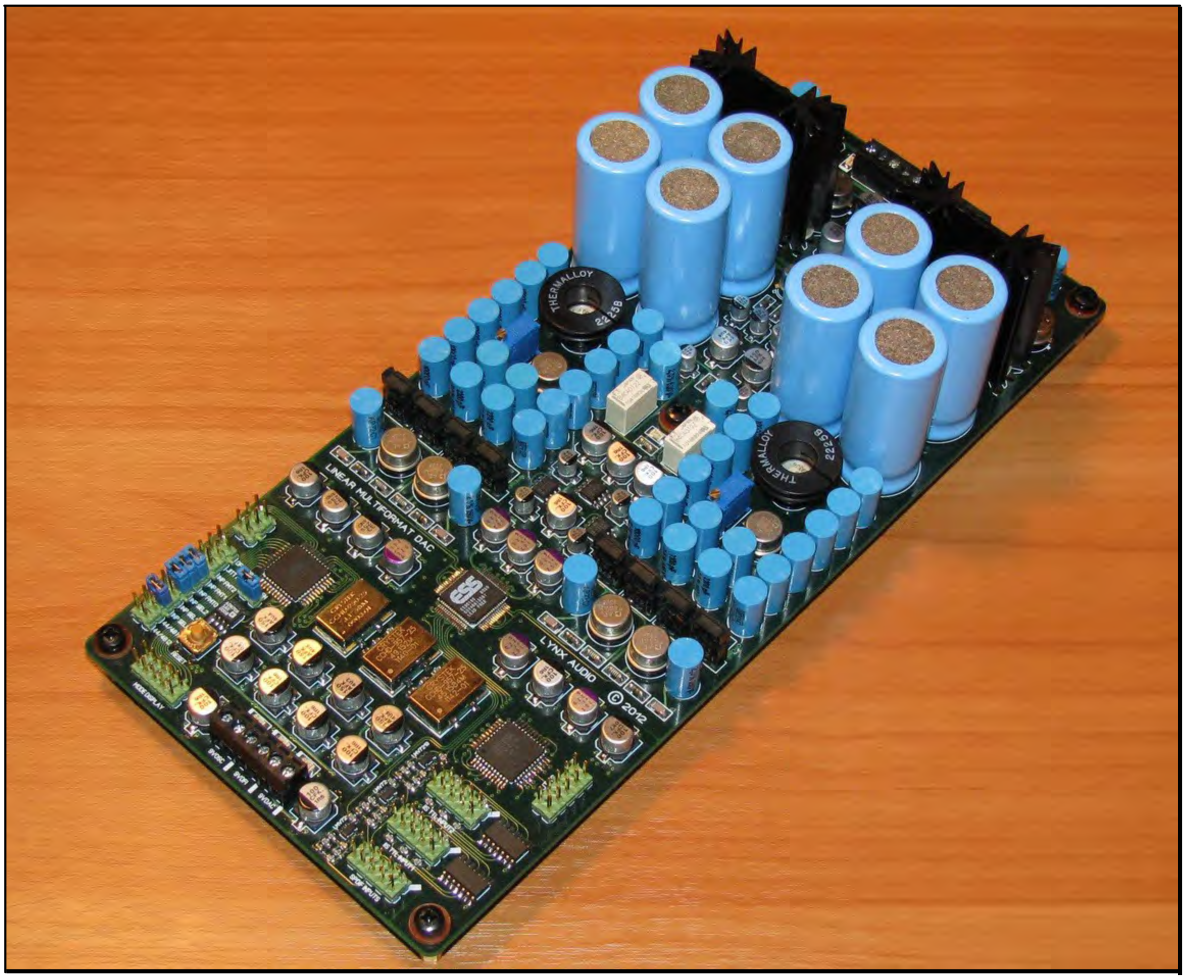

Fig. 3 DAC Lynx D48V3 module board

The board is designed in such a way that permits the use of several components of different types. It is possible to install polypropylene capacitors in analog filters and shunts feeds - ERO and EMZ types of KP1837 and Wima FKP2, different OpAmps types of housings TO-99 (device was checked with using the OpAmp types of OP42, AD744, LM118, TDA1034, OPA627, LT1055, AD711), for the OpAmp subtractor is provided possibility to assemble different balancing schemes by setting relevant resistors, transistors, emitter-followers – in TO-126 and TO-92MOD package. Electrolytic capacitors in analog supply can be of any type with a shell diameter of 16 ... 18 mm and the distance between the terminal of 7.5mm (Cornell Dubilier series 301 on picture). The digital part is mainly used 0603 size resistors and capacitors, only some are 0805 and 1206. The analog circuits are used MELF resistors 0204 and 0207. Electrolytic Capacitors - Panasonic FK and Sanyo SVP SMD type. Ceramic capacitors in bypass feeds ES9018 - 0.1mkF NP0 Murata production.

All power inputs are provided with an indication of voltage and possible reverse polarity protection. From supply sources the DAC consumpt the following currents:

1. + 9VOSC - no more than 100 mA
2. + 9VDF - no more than 350 mA
3. + 9VDAC - 100 mA
4. 22VDC1 - less than 250 mA
5. 22VDC2 - not more than 250 mA

The power sources of analog circuit and DAC (22VDC1, 22VDC2, + 9VDAC) are unstabilized, with the large-capacity filter, the others - with a primary stabilization on chips LM317. The power supply has no fundamental differences from the known module Lynx PWR60.

The circuit DAC board module provides outputs for supplying format of input control signals, input selector, selection for the clock generator (independently for each of the pair of synchronous inputs), the inclusion jitter reduction system and selecting the type of characteristics of the digital filter and data output of the sampling frequency during operation from SPDIF-inputs and from the frequency proportional to the sampling rate - during operation of the synchronous inputs.

Three SPDIF inputs are on single connector, and two synchronous I2S input – on separate connectors. Masterclock output frequency on them is 22.5792 MHz and 24,576 MHz depending from the selected oscillator. Such output frequency ensures compatibility DAC Lynx D48V3 on signals from the audio bus receivers USB-Edel.

The measurements of DAC parameters confirmed the stated manufacturer low distortion for ES9018 chips. At full scale signal, total harmonic distortion (distortion with the current-voltage converter and subtractor) for a frequency of 1 ... 4kHz not exceed -120 ... -122dB (especially for one guy from ixbt.ru in terms of required unliteracy reduction, note that reliable measurements (the difference between the concepts of "measurement" and "estimate" will not be considered, he will be able to find it in any textbook on ESI) such levels of distortion produced by a selective micro voltmeters, rather than the FFT, though, the results are close enough, because of the continuous periodic signals). Intermodulation distortion for a two-frequency signal of 19 kHz + 20 kHz with the peak level of the mixture equal to the full scale transform is also extremely small. Residual signal level does not exceed in this case -132dB. However, it should be borne in mind that for two-frequency signal amplitude of each of the component alone is half the sum of the peak amplitude.

On figs 4 ... 9 shown the spectrogram of the output signal frequency of 1 kHz on different levels and the total frequency of 19 kHz and 20 kHz signal with a peak level of -0.5 dB from full scale.

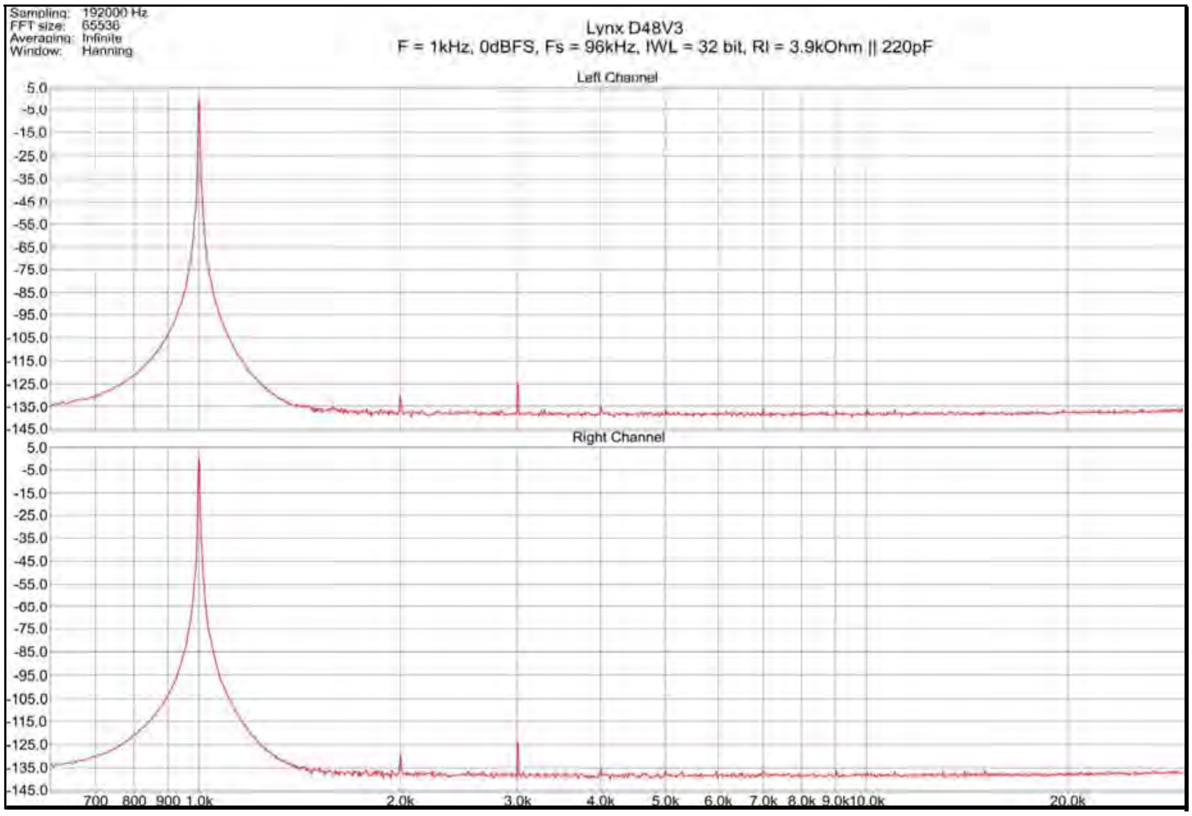

Fig. 4 Spectrum at 0dB level of the output signal

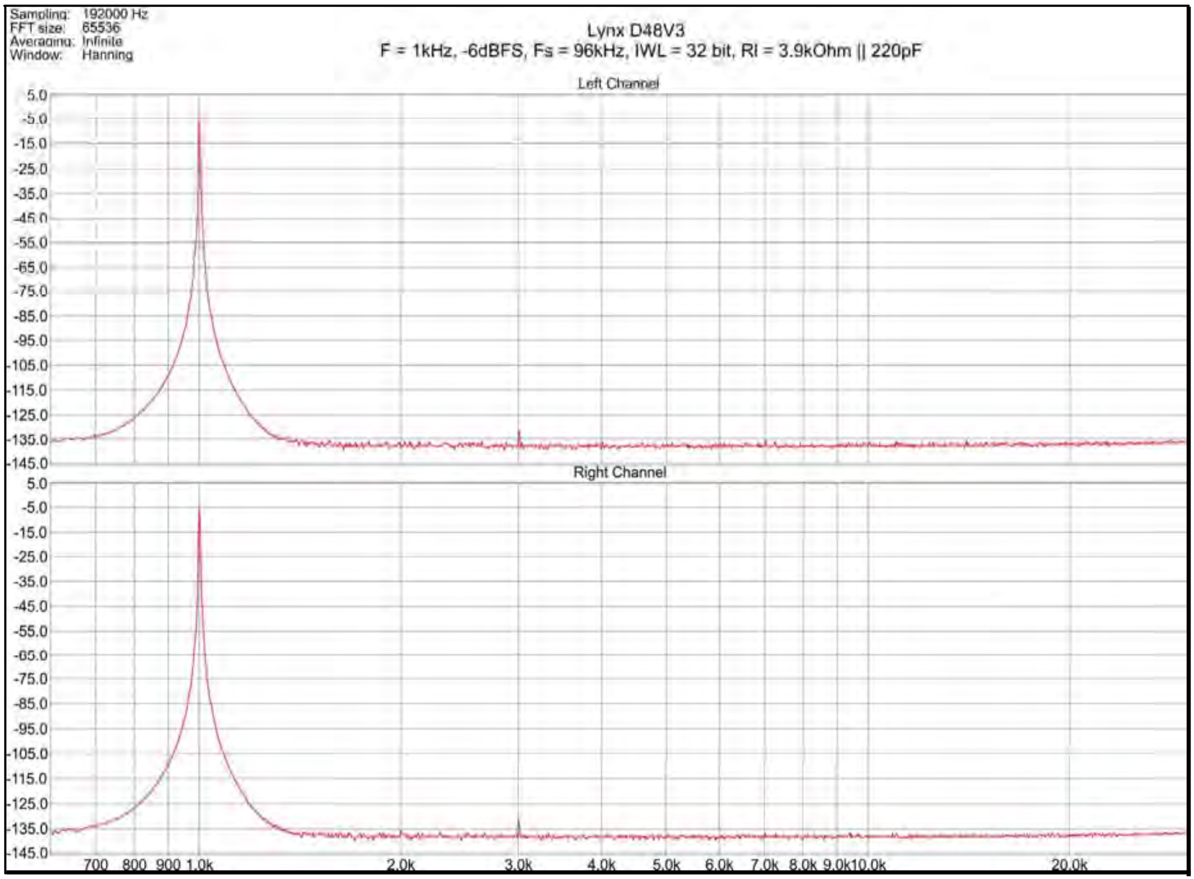

Fig. 5 Spectrum for output level -6dB

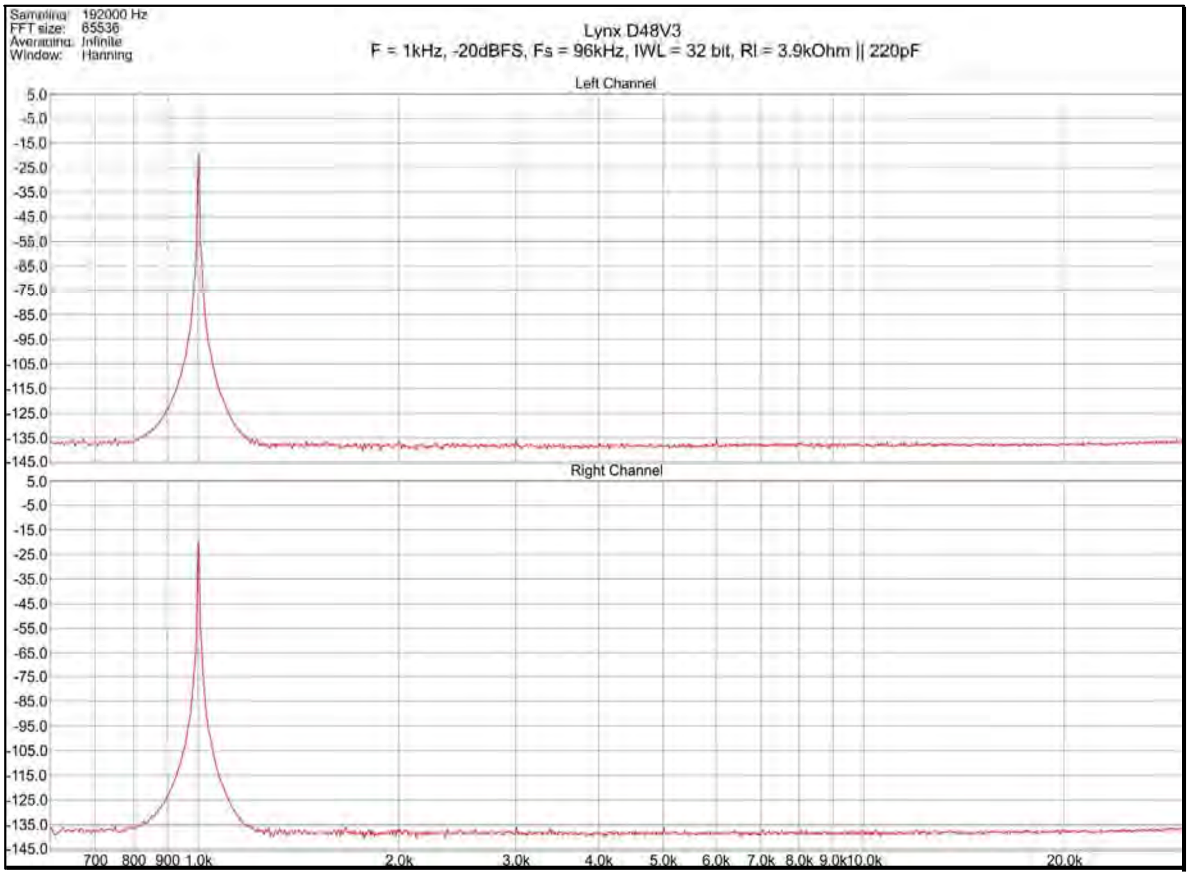

Fig. 6 Spectrum for -20dB level output signal

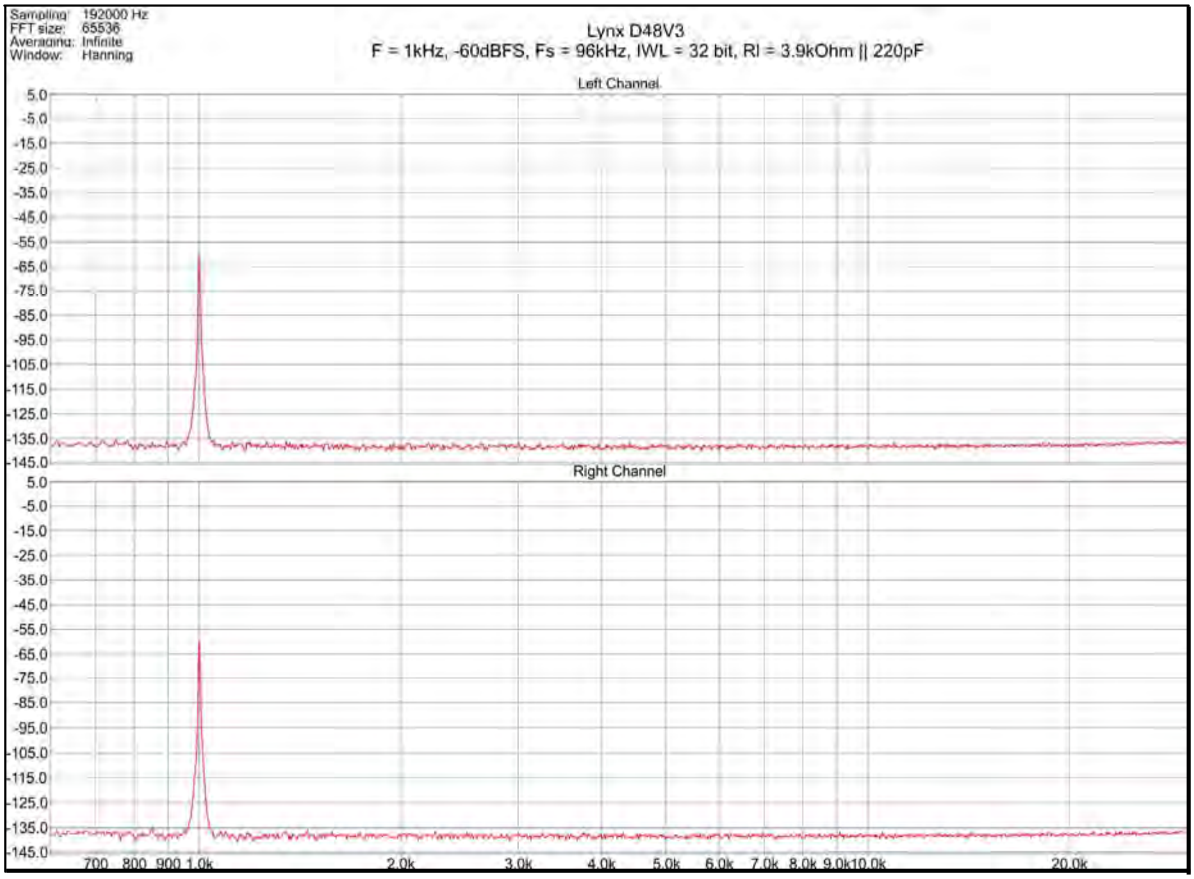

Fig. 7 Spectrum for -60dB level output signal

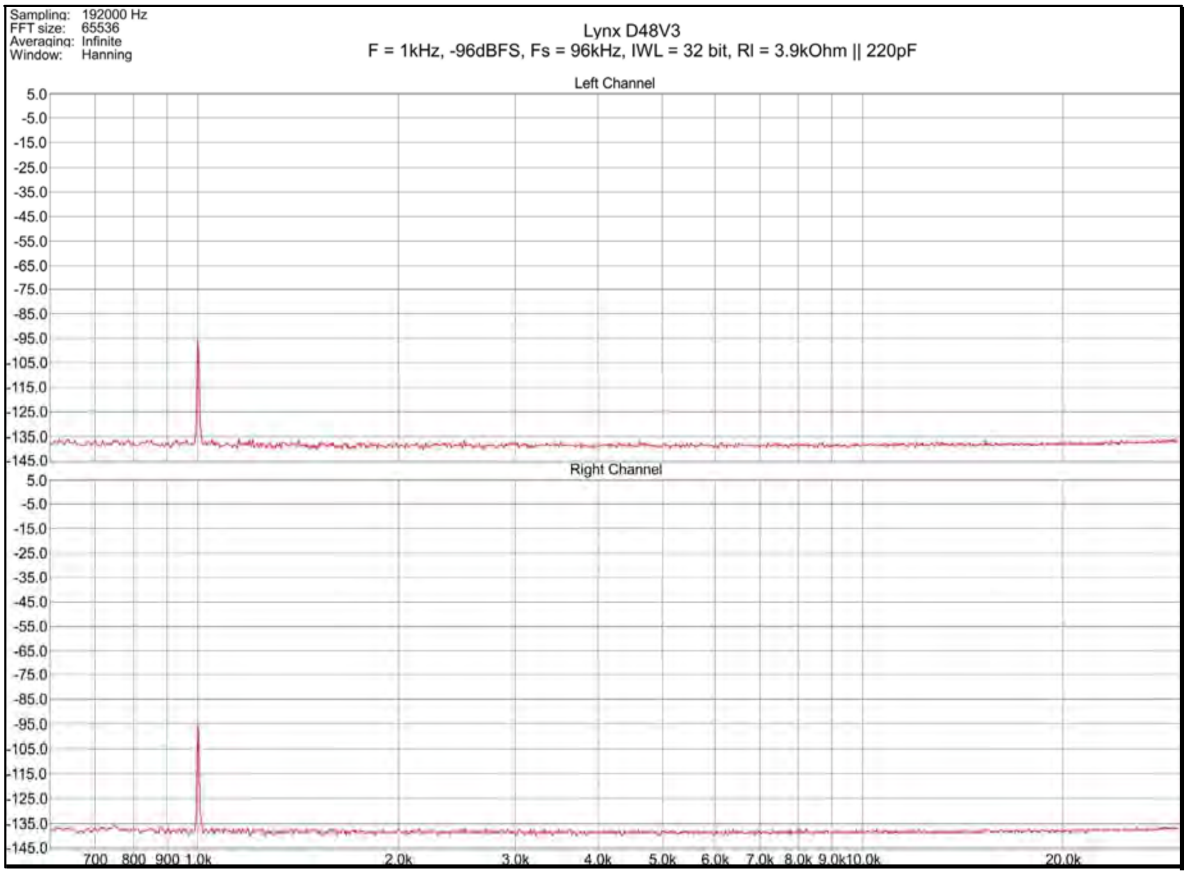

Fig. 8 Spectrum for -96dB level output signal

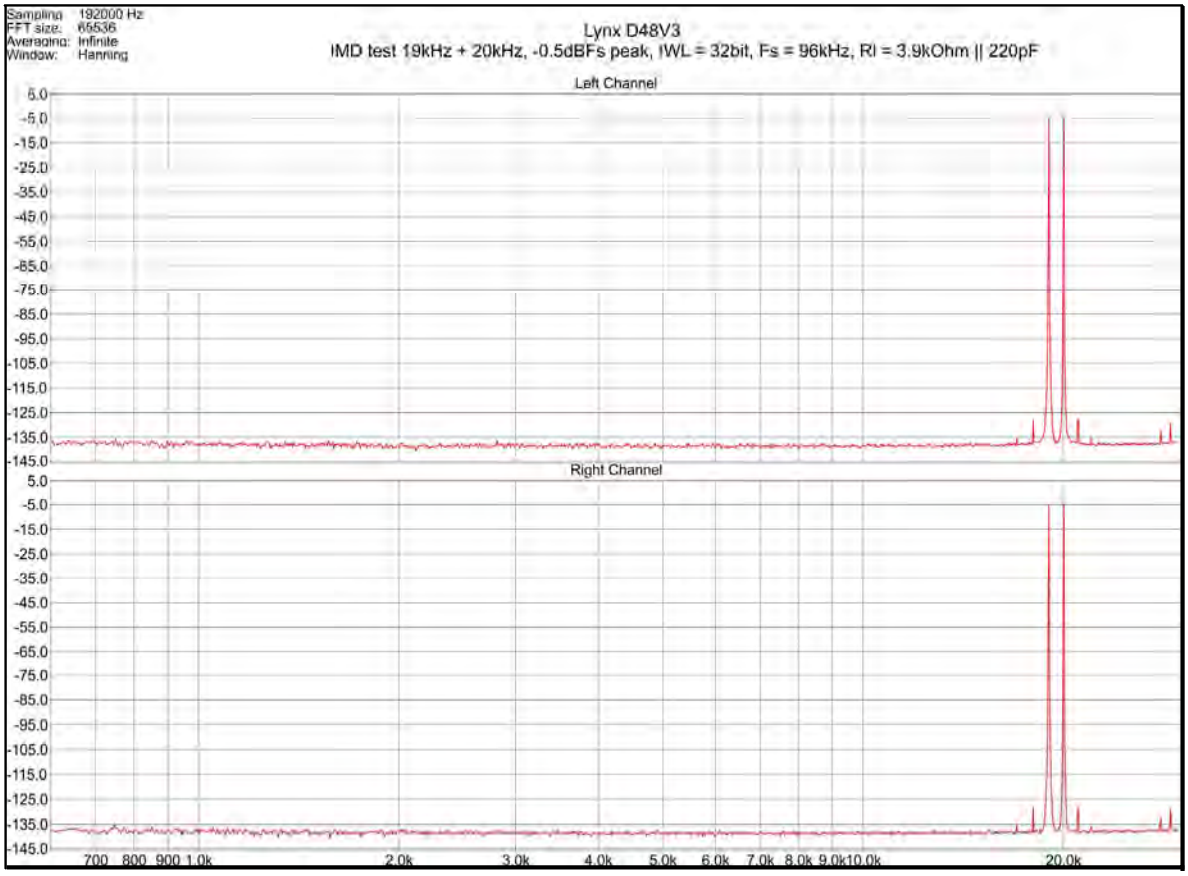

Fig. 9 Spectrum for output signals of two-frequencies 19 kHz + 20 kHz, the peak level of -0.5dB

Fig. 10 Finished DAC block based on Lynx D48V3 module

The first sample of Lynx D48V3 DAC have the following characteristics:

1) nominal output voltage corresponding full scale conversion V (RMS)	2.02
2) relative noise at the output (At zero input signal), dB	under -135
3) relative harmonic distortion and noise in the 48 kHz frequency band for 32-bit signal in Full scale at 1000 Hz, dB	under -122 *
4) relative harmonic distortion and noise in the 48 kHz frequency band for 32-bit signal at 1000 Hz, the level of -6 dB from full scale, dB	under -132 *
5) relative level of intermodulation products, dB	under -120 *
6) interference level in 100 MHz band of the analog output, dB	under -85
7) dynamic conversion range, dB	more than 145

(*) Distortion levels were measured using a selective microvoltmeter

Enough prolonged use of the DAC (both the second and third versions) showed that the product turned out very versatile, capable of working equally well with virtually any musical material. DAC has high resolution and excellent reliability of the transmission of both formal and emotional-psychological components of music. Listening to music with this DAC is very nice and fun. His character sound a little different from most other devices, it is very placid, I would say "quiet" and very "delicate", not liying in anything, but at the same time never annoying. Ideal for easy-listening, club jazz and soul, works great classic rock music and orchestral works.

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