Application 1. Signals and control of Lynx D60

Pin Assignment of connector XS6 “INP1”	
Contact #	Circuit
1	BCKI 1
2	DEEMPHASIS 1 (log.0 = off, log.1 = on)
3	SDATA 1
4	gnd
5	LRCKI 1
6	gnd
7	MCLKO 1
8	gnd
9	+5V/+9V (up to 100mA) power supply of an external device operating on this input
10	MUTE 1 (log.0 = on, log.1 = mute)

Pin Assignment of connector XS5 “INP2”	
Contact #	Circuit
1	BCKI 2
2	DEEMPHASIS 1 (log.0 = off, log.1 = on)
3	SDATA 2
4	gnd
5	LRCKI 2
6	gnd
7	MCLKO 2
8	gnd
9	+5V/+9V (up to 100mA) power supply of an external device operating on this input
10	MUTE 2 (log.0 = on, log.1 = mute)

Pin Assignment of connector XS4 “INP3”*	
Contact #	Circuit
1	LRCKI 3
2	DEEMPHASIS 3 (log.0 = off, log.1 = on)
3	BCKI 3
4	gnd
5	SDATA 3
6	gnd
7	MCLKO 3
8	gnd
9	+5V/+9V (up to 100mA) power supply of an external device operating on this input
10	MUTE 3 (log.0 = on, log.1 = mute)

* INP3 input pin-to-pin compatible with "USB Transport plus" output connector

Pin Assignment of connector XS9 “INP1 CNTR”	
Contact #	Circuit
1	INP SELECT 0
2	gnd
3	MCLKO1 FREQ SELECT (log.0 = 384Fs, log.1 = 768Fs)
4	gnd
5	MCLKO1 ENABLE (log.0 = MCLKO1 enabled, log.1 = MCLKO1 disabled)
6	gnd
7	1x/2x INP1 (log.0 = locked for FS =44/48 kHz, log.1 = locked for FS > 44/48 kHz)
8	gnd
9	44/48 kHz INP1 (log.0 = based on 48 kHz, log.1 = based on 44,1 kHz)
10	gnd

Pin Assignment of connector XS10 “INP2 CNTR”	
Contact #	Circuit
1	INP SELECT 1
2	gnd
3	MCLKO2 FREQ SELECT (log.0 = 384Fs, log.1 = 768Fs)
4	gnd
5	MCLKO2 ENABLE (log.0 = MCLKO2 enabled, log.1 = MCLKO2 disabled)
6	gnd
7	1x/2x INP2 (log.0 = locked for FS =44/48 kHz, log.1 = locked for FS > 44/48 kHz)
8	gnd
9	44/48 kHz INP2 (log.0 = based on 48 kHz, log.1 = based on 44,1 kHz)
10	gnd

Pin Assignment of connector XS11 “INP3 CNTR”	
Contact #	Circuit
1	INP SELECT 2
2	gnd
3	MCLKO3 FREQ SELECT (log.0 = 384Fs, log.1 = 768Fs)
4	gnd
5	MCLKO3 ENABLE (log.0 = MCLKO3 enabled, log.1 = MCLKO3 disabled)
6	gnd
7	1x/2x INP3 (log.0 = locked for FS =44/48 kHz, log.1 = locked for FS > 44/48 kHz)
8	gnd
9	44/48 kHz INP3 (log.0 = based on 48 kHz, log.1 = based on 44,1 kHz)
10	gnd

Pin Assignment of connector XS2 “DISPLAY DATA”	
Contact #	Circuit
1	INP IND 0
2	gnd
3	INP IND 1
4	gnd
5	INP IND 2
6	gnd
7	SAMPLING FREQUENCY IND 0
8	gnd
9	SAMPLING FREQUENCY IND 1
10	gnd
11	SAMPLING FREQUENCY IND 2
12	gnd

Pin Assignment of connector XS1 “AK4115 MODE”	
Contact #	Circuit
1	ACKS (masterclock frequency auto-select: log.0 = off, log.1 = on)
2	gnd
3	DOF0 (output data format: log.0 = Left Justified, log.1 = I2S.)
4	gnd
5	XTL (selection of a method for determining the current sampling rate. Install log. 1)
6	gnd
7	OCK0 (selection of output masterclock frequency for SPDIF receiver 0)
8	gnd
9	OCK0 (selection of output masterclock frequency for SPDIF receiver 1)
10	gnd

Pin Assignment of connector XS8 "DAC MODE"	
Contact #	Circuit
1	DINV – hardware reset (log. 0 – reset, log. 1 – on)
2	gnd
3	DFMD (DF mode: log. 0 –fast fall in frequency response, log. 1 – minimum phase delay)
4	gnd
5	DINF2 (input data format 2)
6	gnd
7	DINF1 (input data format 2)
8	gnd
9	DINF0 (input data format 2)
10	gnd

Pin Assignment of connector XS4	
Contact #	Circuit
1	Power supply for devices connected to synchronous inputs
2	Power supply for devices connected to synchronous inputs
3	+9V
4	+5V

Pin Assignment of connectors XS12 и XS13	
Contact #	Circuit
1	Non-inverting inputs of the low-pass filter op amp
2	Half of DAC reference voltage (+ 2.5V)
3	Non-inverting inputs of the low-pass filter op amp
4	gnd

Control of data output modes and masterclock by SPDIF receiver

1. The mode with a constant masterclock frequency of 22.5792 / 24.576 MHz:
   ACKS (1-XS1) = log. 1
   For single frequencies (44.1/48 kHz) - 512fs For dual
   frequencies (88.2/96 kHz) - 256fs
   For quadruple frequencies (176.4/192 kHz) – 128fs

2. The mode with a constant masterclock frequency in relative to sampling rate:
   ACKS (1-XS1) = log. 0
   OCK0 = 0, OCK1 = 0: 256fs (work with single and double sampling rates)
   OCK0 = 0, OCK1 = 1: 512fs (work with single sampling rates)
   OCK0 = 1, OCK1 = 1: 128fs (work with any valid sampling frequencies)

DAC input selection

INP SELECT0	INP SELECT1	INP SELECT2	Selected input
0	0	0	INP1
1	0	0	INP2
0	1	0	INP3
0	0	1	AES/EBU
1	0	1	SPDIF1
0	1	1	SPDIF2
1	1	1	SPDIF3

For each synchronous input:

384/768fs – n: log.0 = 384fs, log.1 = 768fs;
MCKEN – n: log.0 = mclk enabled, log.1 = mclk disabled;
1x/2x – n: log.0 = single freqs, log.1 = other freqs;
44/48 – n: log.0 = base freq 48kHz, log.1 = base freq 44.1kHz.

Synchronous input data format selection

DINF0	DINF1	DINF2	Selected input
0	0	0	Right Justified 16 bit
1	0	0	Right Justified 20 bit
0	1	0	Left Justified 24 bit
1	1	0	I2S 24 bit
0	0	1	Right Justified 24 bit
1	0	1	Right Justified 32 bit
0	1	1	Left Justified 32 bit
1	1	1	I2S 32 bit