

Process Properties - HDL Options

Category: Synthesis Options, HDL Options, Xilinx Specific Options

Properties are not editable while a process is running.

Switch Name	Property Name	Value
-fsm_extract, -fsm_encoding	FSM Encoding Algorithm	Auto
-safe_implementation	Safe Implementation	No
-vldcase	Case Implementation Style	None
-fsm_style	FSM Style	LUT
-ram_extract	RAM Extraction	<input checked="" type="checkbox"/>
-ram_style	RAM Style	Auto
-rom_extract	ROM Extraction	<input checked="" type="checkbox"/>
-rom_style	ROM Style	Auto
-auto_bram_packing	Automatic BRAM Packing	<input type="checkbox"/>
-shreg_extract	Shift Register Extraction	<input checked="" type="checkbox"/>
-shreg_min_size	Shift Register Minimum Size	2
-resource_sharing	Resource Sharing	<input checked="" type="checkbox"/>
-use_dsp48	Use DSP Block	Auto
-async_to_sync	Asynchronous To Synchronous	<input type="checkbox"/>

Property display level: Advanced ☒ Display switch names Default

OK Cancel Apply Help

Process Properties - Synthesis Options

Category: Synthesis Options, HDL Options, Xilinx Specific Options

Properties are not editable while a process is running.

Switch Name	Property Name	Value
-opt_mode	Optimization Goal	Speed
-opt_level	Optimization Effort	Fast
-power	Power Reduction	<input type="checkbox"/>
-iuc	Use Synthesis Constraints File	<input type="checkbox"/>
-uc	Synthesis Constraints File	...
-keep_hierarchy	Keep Hierarchy	No
-netlist_hierarchy	Netlist Hierarchy	Rebuilt
-glob_opt	Global Optimization Goal	AllClockNets
-rtlview	Generate RTL Schematic	Yes
-read_cores	Read Cores	<input checked="" type="checkbox"/>
-sd	Cores Search Directories	... + ...
-write_timing_constraints	Write Timing Constraints	<input type="checkbox"/>
-cross_clock_analysis	Cross Clock Analysis	<input type="checkbox"/>
-hierarchy_separator	Hierarchy Separator	/
-bus_delimiter	Bus Delimiter	<>
-slice_utilization_ratio	LUT-FF Pairs Utilization Ratio	100
-bram_utilization_ratio	BRAM Utilization Ratio	100
-dsp_utilization_ratio	DSP Utilization Ratio	100
-case	Case	Maintain
set -xsthdpini	Work Directory	/home/ise/Desktop/Valve DAC/LX150/xst
	HDL INI File	...
	Library for Verilog Sources	
-iso	Library Search Order	...
-vlgincdir	Verilog Include Directories	... + ...
-generics	Generics, Parameters	
-define	Verilog Macros	
	Other XST Command Line Options	

Property display level: Advanced ☒ Display switch names Default

OK Cancel Apply Help

Process Properties - Xilinx Specific Options

Category

- Synthesis Options
- HDL Options
- Xilinx Specific Options

Properties are not editable while a process is running.

Switch Name	Property Name	Value
-iobuf	Add I/O Buffers	<input checked="" type="checkbox"/>
-max_fanout	Max Fanout	100000
-bufg	Number of Clock Buffers	16
-register_duplication	Register Duplication	<input checked="" type="checkbox"/>
-equivalent_register_removal	Equivalent Register Removal	<input checked="" type="checkbox"/>
-register_balancing	Register Balancing	Forward
-move_first_stage	Move First Flip-Flop Stage	<input checked="" type="checkbox"/>
-move_last_stage	Move Last Flip-Flop Stage	<input checked="" type="checkbox"/>
-iob	Pack I/O Registers into IOBs	Auto
-lc	LUT Combining	No
-reduce_control_sets	Reduce Control Sets	Auto
-use_clock_enable	Use Clock Enable	Auto
-use_sync_set	Use Synchronous Set	Auto
-use_sync_reset	Use Synchronous Reset	Auto
-optimize_primitives	Optimize Instantiated Primitives	<input type="checkbox"/>

Property display level: Advanced ☒ Display switch names Default

OK Cancel Apply Help

Process Properties - Simulation Model Properties

Switch Name	Property Name	Value
	Simulation Model Target	Verilog
-fn	Retain Hierarchy	<input checked="" type="checkbox"/>
-mhf	Generate Multiple Hierarchical Netlist Files	<input type="checkbox"/>
-tb	Generate Testbench File	<input type="checkbox"/>
-ti	Rename Design Instance in Testbench File to	UUT
	Other NETGEN Command Line Options	
-tm	Rename Top Level Entity to	
-ar	Rename Top Level Architecture To	Structure
-a	Generate Architecture Only (No Entity Declaration)	<input type="checkbox"/>
-extid	Output Extended Identifiers	<input type="checkbox"/>
-tm	Rename Top Level Module To	
-ul	Include 'uselib Directive in Verilog File	<input type="checkbox"/>
-ne	Do Not Escape Signal and Instance Names in Netlist	<input type="checkbox"/>
-ism	Include UNISIM Models in Verilog File	<input type="checkbox"/>
-insert_glbl	Automatically Insert glbl Module in the Netlist	<input checked="" type="checkbox"/>

Property display level: Advanced ☒ Display switch names Default

OK Cancel Apply Help

Process Properties - Translate Properties

Category

- Translate Properties
- Map Properties
- Place & Route Properties
- Post-Map Static Timing Report
- Post-Place & Route Static Timing Report
- Simulation Model Properties

Switch Name	Property Name	Value
-r	Use LOC Constraints	<input type="checkbox"/>
-nt	Netlist Translation Type	Off
-sd	Macro Search Path	...
-a	Create I/O Pads from Ports	<input type="checkbox"/>
-u	Allow Unexpanded Blocks	<input type="checkbox"/>
-ur	User Rules File for Netlist Launcher	...
-aul	Allow Unmatched LOC Constraints	<input type="checkbox"/>
-aut	Allow Unmatched Timing Group Constraints	<input type="checkbox"/>
	Other Ngdbuild Command Line Options	

Property display level: Advanced ☒ Display switch names Default

OK Cancel Apply Help

Process Properties - Map Properties

Category

- Translate Properties
- Map Properties
- Place & Route Properties
- Post-Map Static Timing Report
- Post-Place & Route Static Timing Report
- Simulation Model Properties

Switch Name	Property Name	Value
-ol	Placer Effort Level	High
-xe	Placer Extra Effort	Continue on Impossible
-t	Starting Placer Cost Table (1-100)	1
-xt	Extra Cost Tables	0
-logic_opt	Combinatorial Logic Optimization	<input checked="" type="checkbox"/>
-register_duplication	Register Duplication	On
-r	Register Ordering	4
-global_opt	Global Optimization	Speed
-equivalent_register_removal	Equivalent Register Removal	<input checked="" type="checkbox"/>
-x	Ignore User Timing Constraints	<input type="checkbox"/>
-ntd	Timing Mode	Performance Evaluation
-u	Trim Unconnected Signals	<input checked="" type="checkbox"/>
-ignore_keep_hierarchy	Allow Logic Optimization Across Hierarchy	<input type="checkbox"/>
-detail	Generate Detailed MAP Report	<input type="checkbox"/>
-ir	Use RLOC Constraints	No
-pr	Pack I/O Registers/Latches into IOBs	Off
-c	Maximum Compression	<input type="checkbox"/>
-lc	LUT Combining	Off
-bp	Map Slice Logic into Unused Block RAMs	<input type="checkbox"/>
-power	Power Reduction	Off
-activityfile	Power Activity File	...
-mt	Enable Multi-Threading	Off
	Other Map Command Line Options	

Property display level: Advanced ☒ Display switch names Default

OK Cancel Apply Help

Process Properties - Place & Route Properties

Category

- Translate Properties
- Map Properties
- Place & Route Properties
- Post-Map Static Timing Report
- Post-Place & Route Static Timing
- Simulation Model Properties

Switch Name	Property Name	Value
-r	Place And Route Mode	Route Only
-ol	Place & Route Effort Level (Overall)	High
-xe	Extra Effort (Highest PAR level only)	Continue on Impossible
-x	Ignore User Timing Constraints	<input type="checkbox"/>
-ntd	Timing Mode	Performance Evaluation
	Generate Asynchronous Delay Report	<input type="checkbox"/>
	Generate Clock Region Report	<input type="checkbox"/>
	Generate Post-Place & Route Simulation Model	<input type="checkbox"/>
	Generate Post-Place & Route Power Report	<input type="checkbox"/>
-power	Power Reduction	<input type="checkbox"/>
-activityfile	Power Activity File	...
-mt	Enable Multi-Threading	Off
	Other Place & Route Command Line Options	

Property display level: Advanced ☐ Display switch names Default

OK Cancel Apply Help

Process Properties - Post-Map Static Timing Report Properties

Category

- Translate Properties
- Map Properties
- Place & Route Properties
- Post-Map Static Timing Report
- Post-Place & Route Static Timing
- Simulation Model Properties

Switch Name	Property Name	Value
-v -e	Report Type	Verbose Report
	Number of Paths in Error/Verbose Report	300
-a	Perform Advanced Analysis	<input type="checkbox"/>
-s	Change Device Speed To	-2
-u	Report Unconstrained Paths	<input type="checkbox"/>
-n	Report Paths by Endpoint	3
-fastpaths	Report Fastest Path(s) in Each Constraint	<input checked="" type="checkbox"/>
-nodatasheet	Generate Datasheet Section	<input checked="" type="checkbox"/>
-timegroups	Generate Timegroups Section	<input type="checkbox"/>
-tsi	Generate Constraints Interaction Report	<input type="checkbox"/>

Property display level: Advanced ☐ Display switch names Default

OK Cancel Apply Help

Process Properties - Simulation Model Properties

Switch Name	Property Name	Value
	Simulation Model Target	Verilog
-s	Device Speed Grade/Select ABS Minimum	-2
-fn	Retain Hierarchy	<input checked="" type="checkbox"/>
-mhf	Generate Multiple Hierarchical Netlist Files	<input type="checkbox"/>
-tp	Bring Out Global Tristate Net as a Port	<input type="checkbox"/>
	Global Tristate Port Name	GTS_PORT
-gp	Bring Out Global Set/Reset Net as a Port	<input type="checkbox"/>
	Global Set/Reset Port Name	GSR_PORT
-tb	Generate Testbench File	<input type="checkbox"/>
-ti	Rename Design Instance in Testbench File to	UUT
-insert_pp_buffers	Insert Buffers to Prevent Pulse Swallowing	<input checked="" type="checkbox"/>
	Other NETGEN Command Line Options	
-ar	Rename Top Level Architecture To	Structure
-tpw	Tristate On Configuration Pulse Width	0
-rpw	Reset On Configuration Pulse Width	100
-a	Generate Architecture Only (No Entity Declaration)	<input type="checkbox"/>
-extid	Output Extended Identifiers	<input type="checkbox"/>
-tm	Rename Top Level Module To	
-ul	Include 'uselib Directive in Verilog File	<input type="checkbox"/>
-sdf_anno	Include sdf_annotate task in Verilog File	<input checked="" type="checkbox"/>
-sdf_path	Path Used in sdf_annotate task	Default
-ne	Do Not Escape Signal and Instance Names in Netlist	<input type="checkbox"/>
-ism	Include SIMPRIM Models in Verilog File	<input type="checkbox"/>
-insert_glbl	Automatically Insert glbl Module in the Netlist	<input checked="" type="checkbox"/>

Category: Translate Properties
Map Properties
Place & Route Properties
Post-Map Static Timing Report
Post-Place & Route Static Timing Analysis
Simulation Model Properties

Property display level: Advanced ☒ Display switch names Default

OK Cancel Apply Help

Process Properties - Post-Place & Route Static Timing Report Properties

Category

- Translate Properties
- Map Properties
- Place & Route Properties
- Post-Map Static Timing Report
- Post-Place & Route Static Timing Report Properties**
- Simulation Model Properties

Switch Name	Property Name	Value
-v -e	Report Type	Verbose Report
	Number of Paths in Error/Verbose Report	300
-a	Perform Advanced Analysis	<input type="checkbox"/>
-s	Change Device Speed To	-2
-u	Report Unconstrained Paths	
-n	Report Paths by Endpoint	3
-fastpaths	Report Fastest Path(s) in Each Constraint	<input checked="" type="checkbox"/>
-nodatasheet	Generate Datasheet Section	<input checked="" type="checkbox"/>
-timegroups	Generate Timegroups Section	<input type="checkbox"/>
-stamp	Stamp Timing Model Filename	...
-tsi	Generate Constraints Interaction Report	<input type="checkbox"/>

Property display level: Advanced ☒ Display switch names Default

OK Cancel Apply Help

Process Properties - Translate Properties

Switch Name	Property Name	Value
-r	Use LOC Constraints	<input type="checkbox"/>
-nt	Netlist Translation Type	Off
-sd	Macro Search Path	... + ...
-a	Create I/O Pads from Ports	<input type="checkbox"/>
-u	Allow Unexpanded Blocks	<input type="checkbox"/>
-ur	User Rules File for Netlister Launcher	...
-aul	Allow Unmatched LOC Constraints	<input type="checkbox"/>
-aut	Allow Unmatched Timing Group Constraints	<input type="checkbox"/>
	Other Ngdbuild Command Line Options	

Property display level: Advanced ☒ Display switch names Default

OK Cancel Apply Help

Process Properties - Map Properties

Switch Name	Property Name	Value
-ol	Placer Effort Level	High
-xe	Placer Extra Effort	Continue on Impossible
-t	Starting Placer Cost Table (1-100)	1
-xt	Extra Cost Tables	0
-logic_opt	Combinatorial Logic Optimization	<input checked="" type="checkbox"/>
-register_duplication	Register Duplication	On
-r	Register Ordering	4
-global_opt	Global Optimization	Speed
-equivalent_register_removal	Equivalent Register Removal	<input checked="" type="checkbox"/>
-x	Ignore User Timing Constraints	<input type="checkbox"/>
-ntd	Timing Mode	Performance Evaluation
-u	Trim Unconnected Signals	<input checked="" type="checkbox"/>
-ignore_keep_hierarchy	Allow Logic Optimization Across Hierarchy	<input type="checkbox"/>
-detail	Generate Detailed MAP Report	<input type="checkbox"/>
-ir	Use RLOC Constraints	No
-pr	Pack I/O Registers/Latches into IOBs	Off
-c	Maximum Compression	<input type="checkbox"/>
-lc	LUT Combining	Off
-bp	Map Slice Logic into Unused Block RAMs	<input type="checkbox"/>
-power	Power Reduction	Off
-activityfile	Power Activity File	...
-mt	Enable Multi-Threading	Off
	Other Map Command Line Options	

Property display level: Advanced ☒ Display switch names Default

OK Cancel Apply Help

Process Properties - Place & Route Properties

Switch Name	Property Name	Value
-r	Place And Route Mode	Route Only
-ol	Place & Route Effort Level (Overall)	High
-xe	Extra Effort (Highest PAR level only)	Continue on Impossible
-x	Ignore User Timing Constraints	<input type="checkbox"/>
-ntd	Timing Mode	Performance Evaluation
	Generate Asynchronous Delay Report	<input type="checkbox"/>
	Generate Clock Region Report	<input type="checkbox"/>
	Generate Post-Place & Route Simulation Model	<input type="checkbox"/>
	Generate Post-Place & Route Power Report	<input type="checkbox"/>
-power	Power Reduction	<input type="checkbox"/>
-activityfile	Power Activity File	...
-mt	Enable Multi-Threading	Off
	Other Place & Route Command Line Options	

Property display level: Advanced ☒ Display switch names Default

OK Cancel Apply Help

Process Properties - General Options

Category

General Options
Configuration Options
Startup Options
Readback Options
Encryption Options
Suspend/Wake Options

Switch Name	Property Name	Value
-d	Run Design Rules Checker (DRC)	<input checked="" type="checkbox"/>
-j	Create Bit File	<input checked="" type="checkbox"/>
-g Binary:	Create Binary Configuration File	<input type="checkbox"/>
-b	Create ASCII Configuration File	<input type="checkbox"/>
-g IEEE1532:	Create IEEE 1532 Configuration File	<input type="checkbox"/>
-g Compress	Enable BitStream Compression	<input type="checkbox"/>
-g DebugBitstream:	Enable Debugging of Serial Mode BitStream	<input type="checkbox"/>
-g CRC:	Enable Cyclic Redundancy Checking (CRC)	<input checked="" type="checkbox"/>
-g reset_on_error:	Retry Configuration if CRC Error Occurs	<input type="checkbox"/>
	Other Bitgen Command Line Options	

Property display level: Advanced ☒ Display switch names Default

OK Cancel Apply Help

Process Properties - Configuration Options

Category

General Options

Configuration Options

Startup Options

Readback Options

Encryption Options

Suspend/Wake Options

Switch Name	Property Name	Value
-g ConfigRate:	Configuration Rate	12
-g ProgPin:	Configuration Pin Program	Pull Up
-g DonePin:	Configuration Pin Done	Pull Up
-g TckPin:	JTAG Pin TCK	Pull Up
-g TdiPin:	JTAG Pin TDI	Pull Up
-g TdoPin:	JTAG Pin TDO	Pull Up
-g TmsPin:	JTAG Pin TMS	Pull Up
-g UnusedPin:	Unused IOB Pins	Pull Down
-g UserID:	UserID Code (8 Digit Hexadecimal)	0xFFFFFFFF
-g ExtMasterCclk_en:	Enable External Master Clock	<input type="checkbox"/>
-g ExtMasterCclk_divide:	Setup External Master Clock Division	1
-g SPI_buswidth:	Set SPI Configuration Bus Width	1
-g TIMER_CFG:	Watchdog Timer Value	0xFFFF
	Place MultiBoot Settings into Bitstream	<input type="checkbox"/>
-g next_config_reboot:	MultiBoot: Insert IPROG CMD in the Bitfile	Enable
-g next_config_addr:	MultiBoot: Starting Address for Next Configuration	0x00000000
-g next_config_new_mode:	MultiBoot: Use New Mode for Next Configuration	<input checked="" type="checkbox"/>
-g next_config_boot_mode:	MultiBoot: Next Configuration Mode	001
-g golden_config_addr:	MultiBoot: Starting Address for Golden Configuration	0x00000000
-g failsafe_user:	MultiBoot: User-Defined Register for Failsafe Scheme	0x0000

Property display level: Advanced

☒ Display switch names

Default

OK

Cancel

Apply

Help