The LT1122 Fast Settling JFET Op Amp

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The LT1122 is a new, high performance JFET input op amp. Optimized around high speed and fast settling performance, the LT1122 uses a modified bipolar-FET process. The performance resulting is a combination of not just excellent AC parameters, but low input currents and DC precision, achieved within a junction-isolated process.

Unity-gain stable, the LT1122 features a 14MHz gain bandwidth and a typical 80V/µs slew rate (SR) with controlled symmetry. For a 10V step, it settles to 1mV at the sum node in 340ns(typ), or 540ns max. The LT1122's excellent DC accuracy specifications include an open-loop gain of 500V/mV(typ) into a 2k load, (250V/mV into 600 ohms), input bias/offset currents of 75 and 40pA(max) respectively, and an input offset voltage of 0.6mV(max). For driving difficult loads, the LT1222 has a 40mA current limit, and can drive 600 ohm loads to ±12V(min).

The LT1122 achieves these combined parameters with a unique polygate JFET. In conventional FET technology, the gate contact is tens of micrometers away from the actual channel of the FET, creating a response pole due to the gate implant series resistance and capacitance, thereby limiting bandwidth. In the LT1122 JFET design, a polysilicon layer provides a gate contact directly over the channel, eliminating this pole. In addition, the circular structure and small drain diffusion used minimizes gate-drain capacitance.

Atop these and other speed related circuit improvements, the LT1122 has very low audio range distortion. For example, THD at an inverting gain of 10 is 0.001% or less to 20kHz, with non-inverting performance only slightly worse. For IM distortion via the CCIF method, the LT1122 has performance as much as 2 orders of magnitude better than typical industry JFET amplifiers such as 156/356 types. The low total distortion is largely due to two design factors. One is the LT1122 SR which is not only high at 80V/µs, but which also is intrinsically symmetrical. This factor eliminates the even order distortion effects present in a topology with asymmetric transconductance. Another factor is the linear all NPN output stage, which features high output current and very high speed.

This LT1122 output stage is shown in Figure 1 in simplified form, and has several features which contribute to high linearity. One is the local loop which controls the idle current in Q12 (I_i). This loop is comprised of Q12, R9, Q9, R6, J6, Q10 and Q13, and it causes the output follower Q12 to always conduct the idle current or more, so providing a low output impedance. Without precautions however, this type of stage can also distort for some conditions. If for example, Q12 sources load current greater than I_i, the control loop turns off, and Q13 can then no longer return to sinking load current immediately. If unchecked, this would lead to crossover glitches, when the output must quickly change from sourcing to sinking load current. Here however, the problem is solved by Q7, an additional main loop drive input which can provide the short term sink current required. This allows Q13 to turn back on more slowly, but without adding distortion.

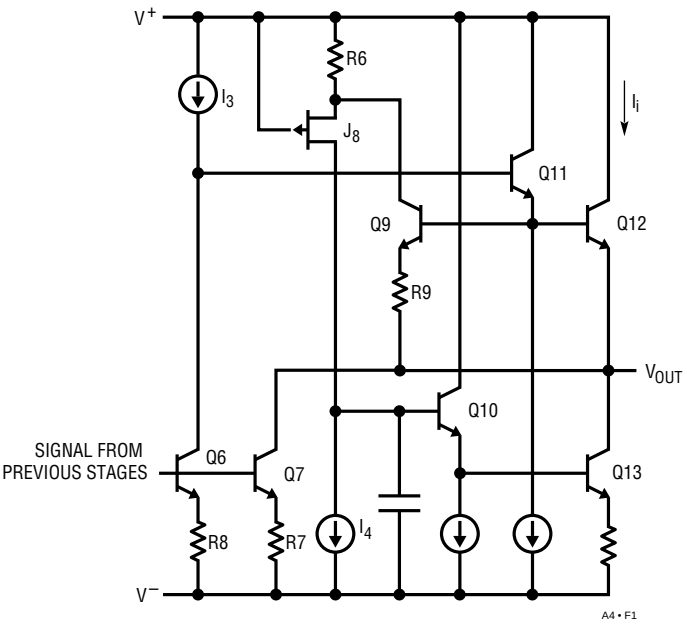

Figure 1. LT1122 Output Stage

Fast settling is the main feature of the LT1122, and is 100% tested in a settling time test fixture described on the data sheet. The LT1122 is available in 4 electrical grades, 2 premium (A & B) and 2 standard (C & D). Of these, the A & C parts are 100% tested for settling, with the others (B & D) sample tested. LT