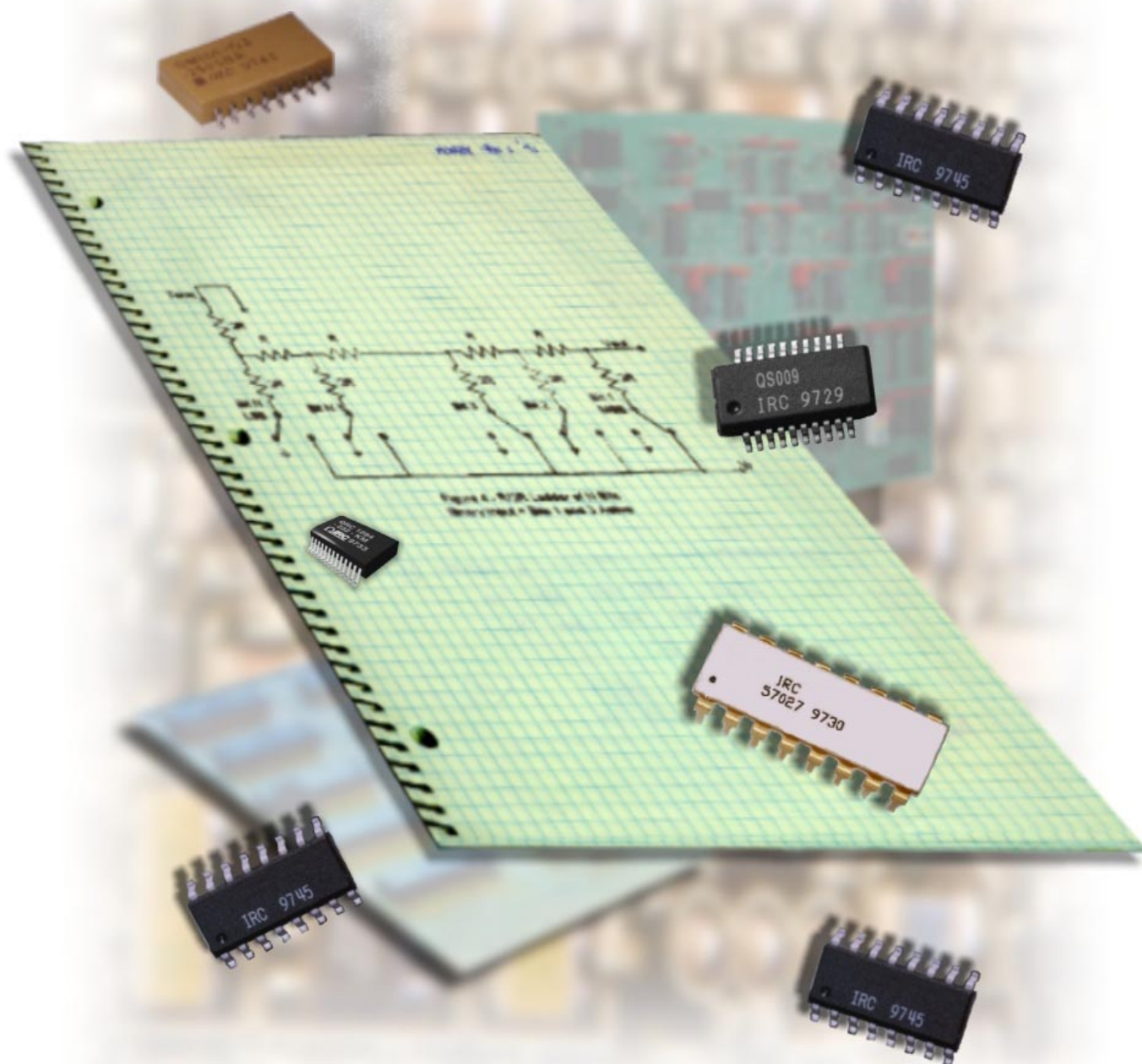**ISO-9001 Registered**

R/2R LADDER NETWORKS

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References:

IRC R/2R Data Sheet
IRC QS009 Data Sheet

R/2R Ladder Networks

Issue

R/2R ladder networks provide a simple means to convert digital information to an analog output. Although simple in design and function, applying an R/2R resistor network to a real application requires attention to how the device is specified. Output errors due to resistor tolerances are often overlooked in the design of the digital to analog conversion (DAC) circuit and in the selection of the R/2R ladder itself. This application note identifies these issues, provides methods for calculating R/2R resolution and accuracy and a means to better specify R/2R ladder networks.

Background

Resistor ladder networks provide a simple, inexpensive way to perform digital to analog conversion (DAC). The most popular networks are the binary weighted ladder and the R/2R ladder. Both devices will convert digital voltage information to analog, but the R/2R ladder has become the most popular due to the network's inherent accuracy superiority and ease of manufacture.

Figure 1 is a diagram of the basic R/2R ladder network with N bits. The "ladder" portrayal comes from the ladder-like topology of the network. Note that the network consists of only two resistor values; R and 2R (twice the value of R) no matter how many bits make up the ladder. The particular value of R is not critical to the function of the R/2R ladder.
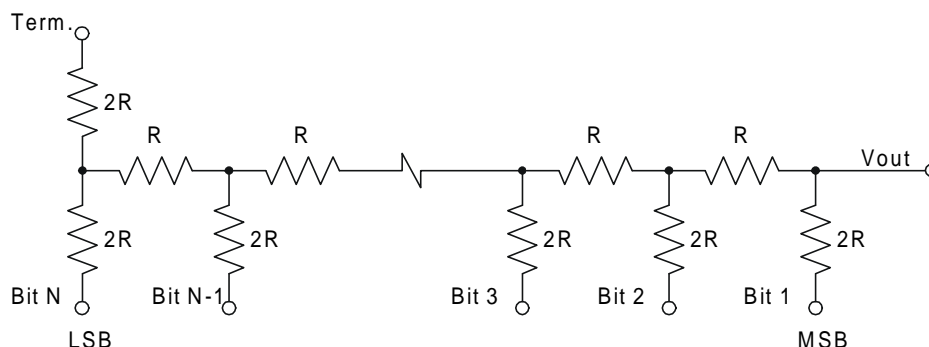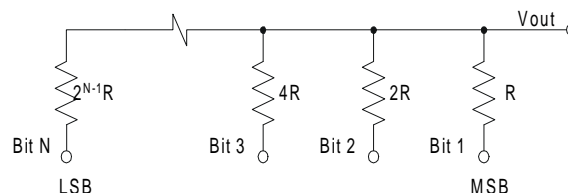

Figure 2. Binary Weighted Ladder

The binary weighted ladder shown in Figure 2 requires double multiples of R as the number of bits increase. As the ratios of the resistors become more and more obtuse in a binary weighted network, the ability to trim the resistors to accurate ratio tolerances becomes diminished. More accurate ratios can be obtained in a resistor network with consistent, similar values as in the R/2R network. The R/2R network provides the most accurate method of digital to analog conversion.

Discussion

R/2R Function

Let's take a look at how an R/2R ladder works. Term. is the termination resistor and is connected to ground. The termination resistor assures that the Thevenin resistance of the network as measured to ground looking toward the LSB (with all bits grounded) is R as shown in Figure 3. The Thevenin resistance of an R/2R ladder is always R – regardless of the number of bits in the ladder.
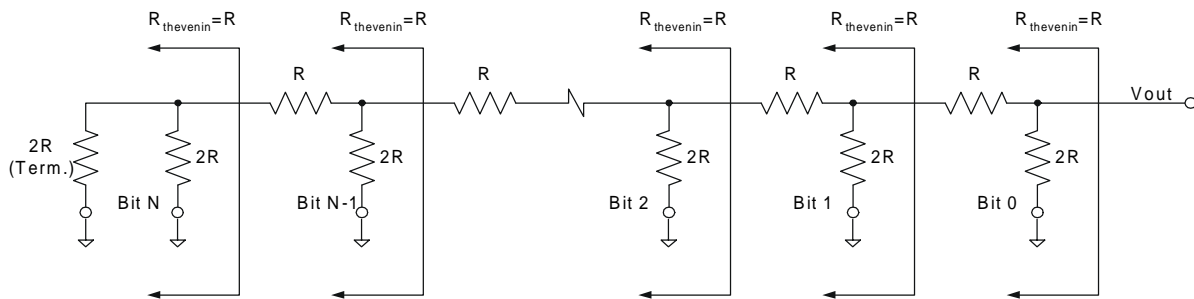

Figure 1. R/2R Ladder of N Bits

Figure 3. Thevenin Resistance

Digital information is presented to the ladder as individual bits of a digital word switched between a reference voltage (Vr) and ground (Figure 4).

Depending on the number and location of the bits switched to Vr or ground, Vout will vary between 0 volts and Vr. If all inputs are connected to ground, 0 volts is produced at the output, if all inputs are connected to Vr, the output voltage approaches Vr, and if some inputs are connected to ground and some to Vr then an output voltage between 0 volts and Vr occurs. These inputs (also called bits in the digital lingo) range from the Most Significant Bit to the Least Significant Bit. As the names indicate, the MSB, when activated, causes the greatest change in the output voltage and the LSB, when activated, will cause the smallest change in the output voltage. If we label the bits (or inputs) bit 1 to bit N the output voltage caused by connecting a particular bit to Vr with all other bits grounded is:

$$Vout = Vr/2^N$$

where N is the bit number. For bit 1, Vout $=Vr/2$, for bit 2, Vout $= Vr/4$ etc. The table shows the

Bit #	Vout
1 MSB	$Vr/2$
2	$Vr/4$
3	$Vr/8$
4	$Vr/16$
5	$Vr/32$
6	$Vr/64$
7	$Vr/128$
8	$Vr/256$
9	$Vr/512$
10	$Vr/1024$
11	$Vr/2048$
12	$Vr/4096$
N LSB	$Vr/2^N$

effect of individual bit locations to the Nth bit. Notice that since bit 1 has the greatest effect on the output voltage it is designated the Most Significant Bit.

Since an R/2R ladder is a linear circuit, we can apply the principle of superposition to calculate Vout. The expected output voltage is calculated by summing the effect of all bits connected to Vr. For example, if bits 1 and 3 are connected to Vr with all other inputs grounded, the output voltage is calculated by:

$$Vout = (Vr/2)+(Vr/8)$$

which reduces to

$$Vout = 5Vr/8.$$

The R/2R ladder is a binary circuit. The effect of each successive bit approaching the LSB is 1/2 of the previous bit. If this sequence is extended to a ladder of infinite bits, the effect of the LSB on Vout approaches 0. Conversely, the full-scale output of the network (with all bits connected to Vr) approaches Vr as shown in equation (1).
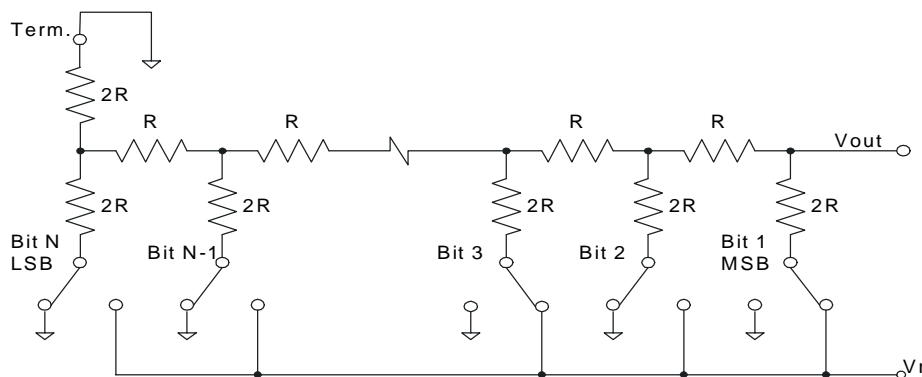

Figure 4. R/2R Ladder of N Bits

$$\lim_{N \to \infty} (Vr) \sum_{i=1}^{N} \frac{1}{2^i} = Vr \qquad (1)$$

The full-scale output is less than Vr for all practical R/2R ladders, and for low pin count devices the full-scale output voltage can be significantly below the value of Vr. Equation (2) can be used to calculate the full-scale output of an R/2R ladder of N bits.

$$\text{Full Scale Output Voltage} = (Vr) \sum_{i-1}^{N} \frac{1}{2^i} \qquad (2)$$

An R/2R ladder of 4 bits would have a full-scale output voltage of $1/2 + 1/4 + 1/8 + 1/16 = 15Vr/16$ or 0.9375 volts (if Vr=1 volt) while a 10 bit R/2R ladder would have a full-scale output voltage of 0.99902 (if Vr=1 volt).

Resolution and Accuracy

The number of inputs or bits determines the resolution of an R/2R ladder. Since there are two possible states at each input, ground or Vr, (also designated as "0" or "1" in digital lingo for positive logic) there are 2^N combinations of Vr and ground to the inputs of an R/2R ladder. The resolution of the ladder is the smallest possible output change for any input change to the ladder and is given by $1/2^N$ where N is the number of bits. This is the output change that would occur for a change in

the least significant bit. For a 10bit R/2R there are 2^N or or 1024 possible binary combinations at the inputs. The resolution of the network is 1/1024 or .0009766. A change in state at the LSB input should change the output of the ladder by .09766% of the full scale output voltage.

The output accuracy of the R/2R ladder is typically specified in terms of full-scale output ± some number of least significant bits. R/2R ladders are usually specified with output accuracies of ±1 LSB or ±1/2 LSB. For example, a ±1/2 LSB specification on a 10 bit ladder is exactly the same as ±0.04883% full-scale accuracy.

> *R/2R Ladders are usually specified with output accuracies of ±1 or ±½ LSB.*

The ladder function is not affected by the value of R (within normal resistance ranges). This would indicate that the absolute tolerances of the resistors making up the ladder are of minimal importance. Then what controls the accuracy of the ladder output?

The ladder operates as an array of voltage dividers whose output accuracies are solely dependent on how well each resistor is matched to the others. Ideally, resistors within the ladder are matched so that the voltage ratio for a given bit is exactly half of that for the preceding bit.
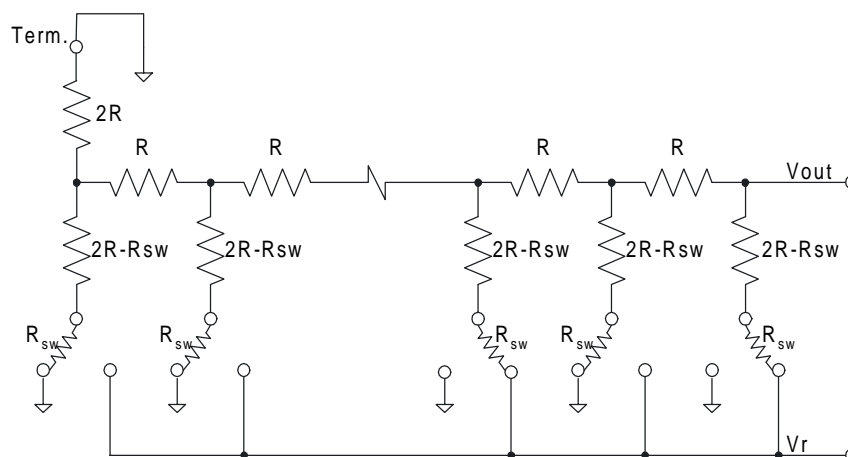
Figure 5. R/2R Ladder with Switch Compensation

Resistors constructed in network form, on the same substrate, which are deposited and processed together, have very similar electrical characteristics. R/2R ladders manufactured as thin film, monolithic networks have an inherent accuracy advantage over discrete solutions because of the tight ratio tolerances and nearly identical resistor characteristics achieved.

Consider an 8-bit ladder specified so that there is solely a ±1.0% absolute tolerance on the resistors. The full resolution of the ladder may not be realized. Ratios within the network could be as poor as almost ±2.0% yielding a ladder, which, although manufactured with 8 bits, may only provide accurate outputs to the 6th or 7th bit. Adding an accuracy specification in terms of ±1 or ±1/2 LSB would ensure 8-bit performance.

Switch Resistance

R/2R inputs are switched between ground and Vr in order to create the digital word that is converted to an analog voltage output. In real applications, these switches (usually solid state) carry some nominal resistance as shown in Figure 5. Actual switch resistances can be as high as 50 ohms in some CMOS devices. Since the switch is connected in series to the 2R resistor, the switch resistance (Rsw) affects the value of the 2R leg of the circuit and thus, the output accuracy of the ladder. The 2R legs of the ladder can be adjusted during the manufacturing process to compensate for the effect of Rsw. Using highly automated laser trim

equipment, 2R legs of the ladder can be individually trimmed, even if the swich resistances are different for each leg! This allows the DAC circuit designer a means to create a much more accurate functional circuit.

Summary:

When specifying an R/2R ladder, consideration must be given to the accuracy of the ladder output as well as the resolution of the ladder in bits. Both the ratio tolerances of the individual resistors within the ladder and the resistance of the switches used at the ladder inputs can affect DAC output accuracy. R/2R ladders have inherent accuracy advantages over other digital to analog conversion circuits such as binary weighted ladders. Thin film monolithic R/2R networks are intrinsically superior to discrete R/2R solutions due to the tight ratio tolerances that can be achieved with resistors on the same substrate. IRC offers R/2R networks in several different bit counts and packages.

Solutions:

IRC offers monolithic R/2R ladders in 8 bit, 10 bit and 12 bit resolution in 16 pin SOIC, 20 pin QSOP and 20 pin DIP packages. Other packages, bit counts and schematics are available upon request.

For more information on ceramic or silicon based devices or to discuss your particular application, check out the IRC web site at www.irctt.com or contact the factory at 512-992-7900.