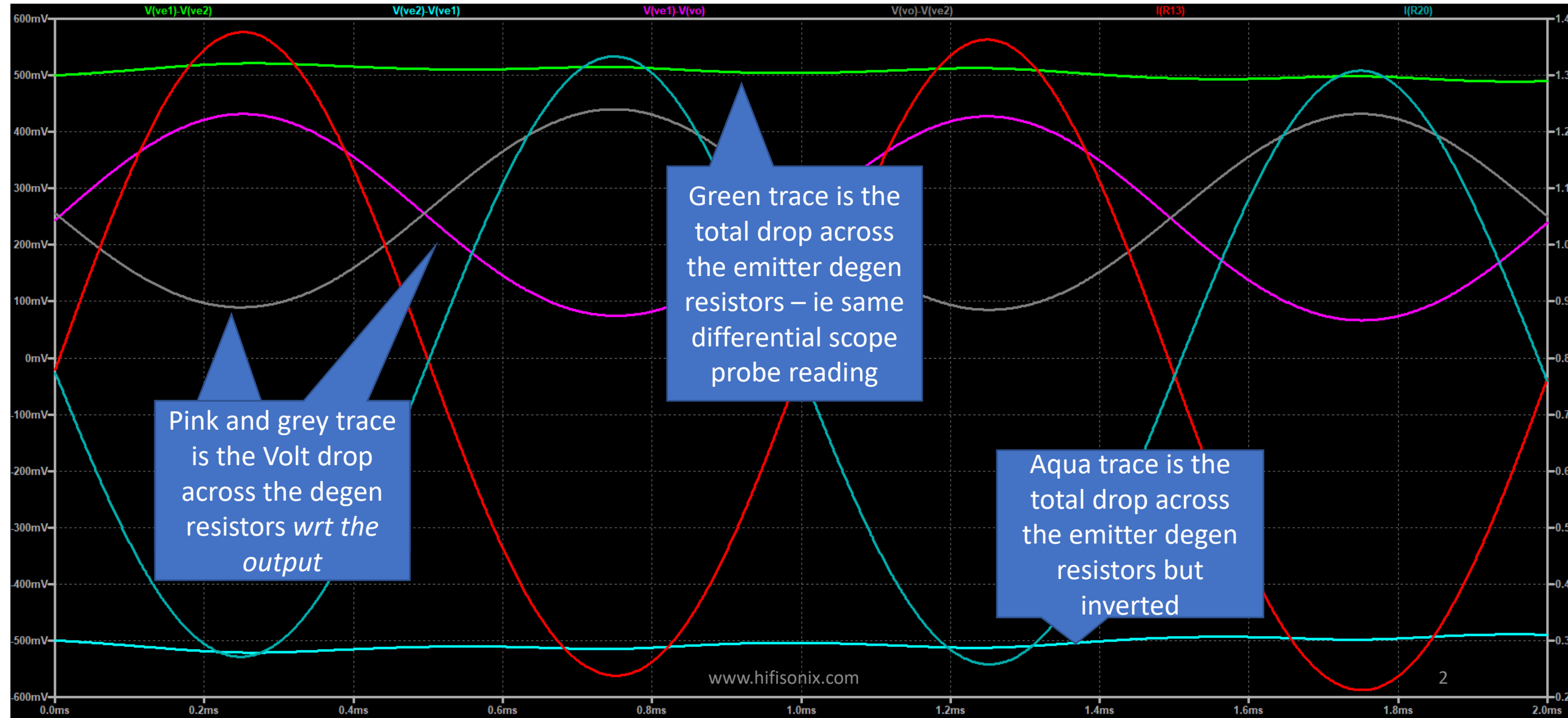


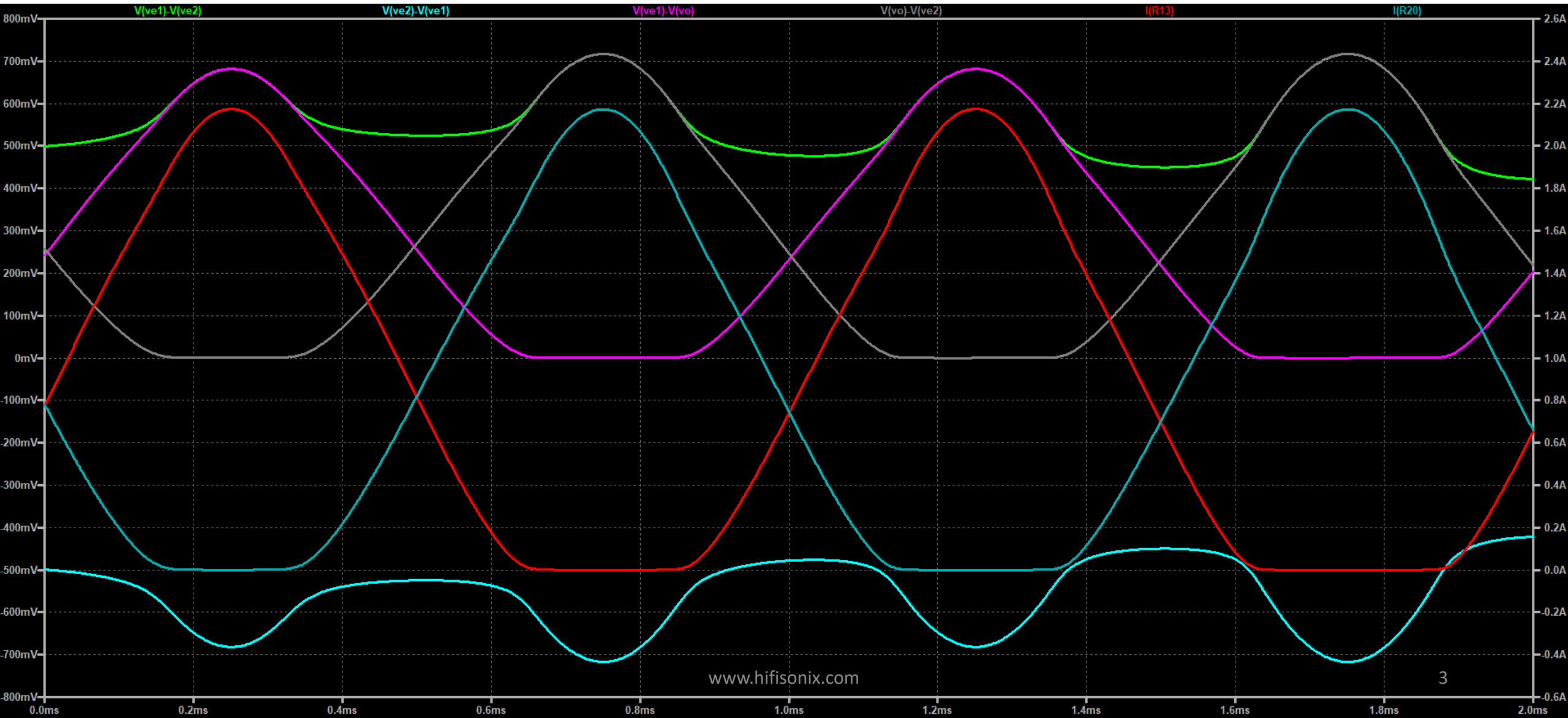
Notes and Observations – kx-Amp Bias Controller

- The voltages as measured across both emitter degeneration resistors at the same time as for example with a differential scope probe are correct as measured and are not always a perfect sine wave. Small output offsets or non-ideal current sharing between transistor pairs can exacerbate differences with this measurement as shown in the previous sims (slides 1-4)
- Wrt the bias controller regulation (slides 5-7), it does vary slightly with the input signal, but given the use of a simple single transistor bias controller and the high class A (AAB) bias currents this is to be expected. In class B, it is of no consequence since one of the output halves of the amplifier are switching off anyway.
- Another option to reduce the ripple across the bias controller is to increase C5 from 10uF to 100uF, however, this requires a settling time for the bias controller of about 6 ms. It is highly unlikely that this has any effect on the sound quality. In class B, there is a very long bias voltage tail, but as mentioned this is of no consequence and it is very small (a few tens of mV)
- The sensitivity of the class A standing current to bias controller ripple is 1.5mA per mV of ripple. Given the high standing current of 600-800mA *per pair* in class A, this is negligible and will not affect class A operation.
- Some improvement in the short term 6 ms settling time of the controller to a perturbation can be had by adding C17 (100uF). However, It is highly doubtful that the settling time of c. 6ms has any impact on the sound (real world signal) and neither does it show up any steady state distortion anomalies in simulation (13ppm 20kHz 16V pk into 8 Ohms class A for C17 = 1pF or 100uF)
- My recommendation is that the circuitry around the bias controller is left as is. There are trade-offs in all designs and a few mV ripple is not going to make any material difference to the overall measured performance of the amplifier.

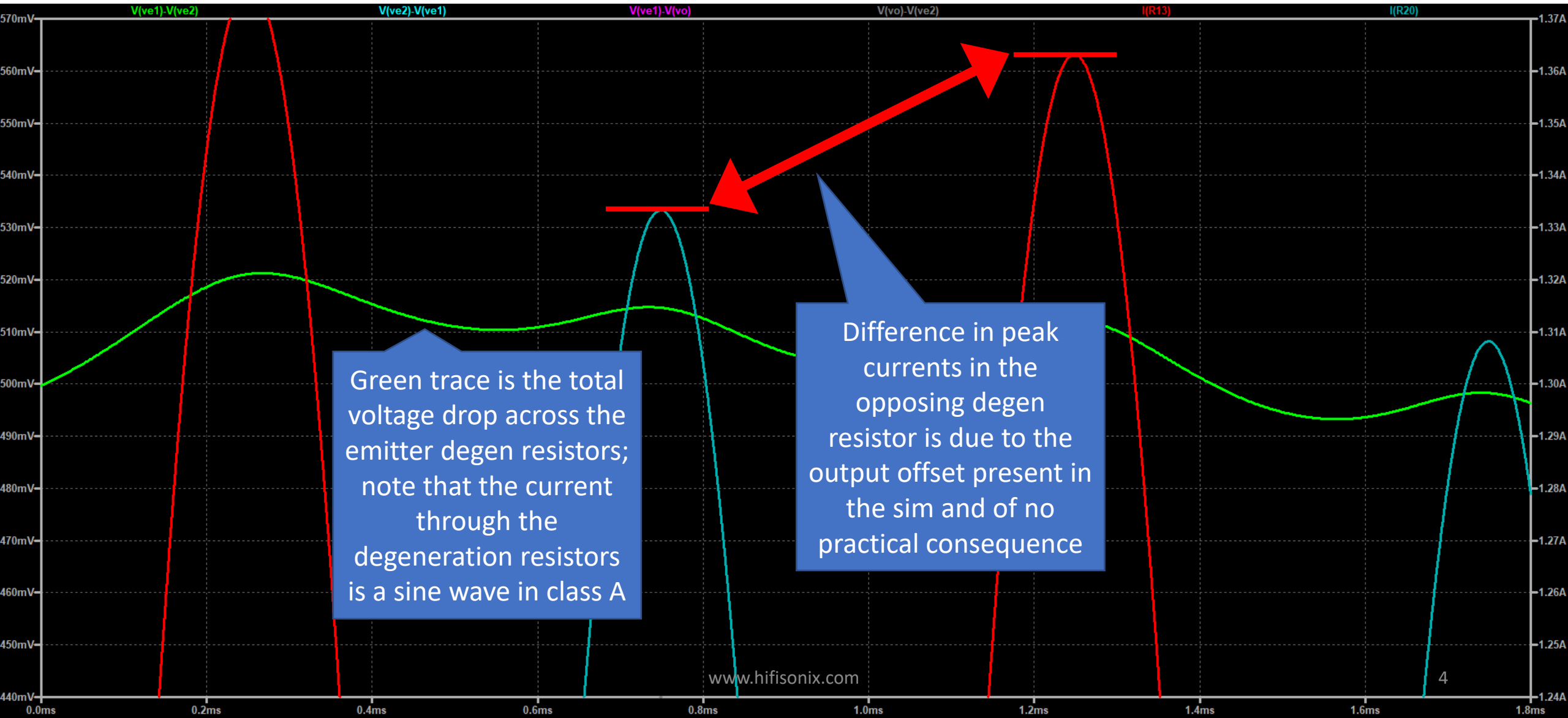
1V input signal, 16.75V pk output into 8 Ohms; Iq per transistor pair is ~750mA. Note that the Red and light green traces – the current through each emitter degen resistor – is a sine wave in class A; C17 = 0uF other caps per kx-Amp circuit diagram



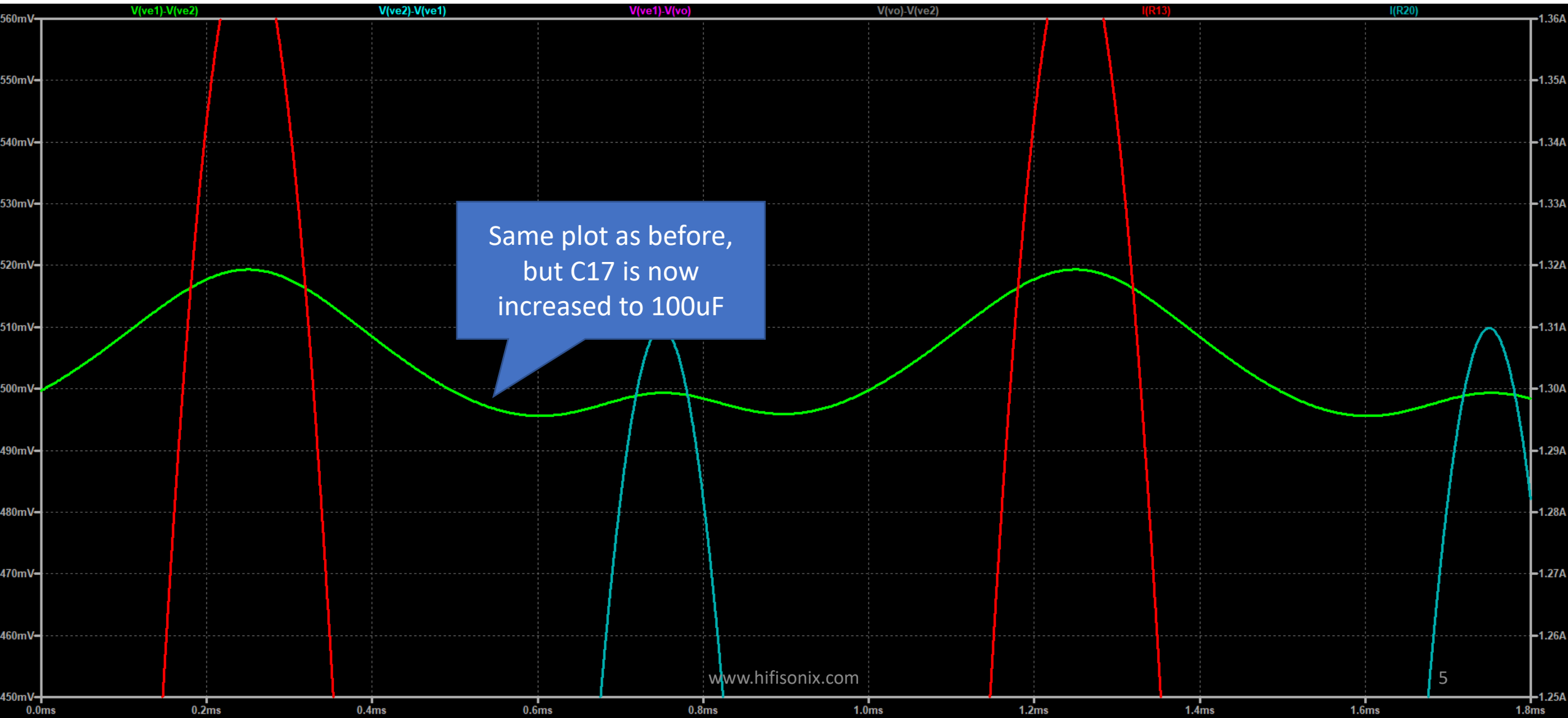
Same as previous slide, but Rload is now 4 Ohms, so amp transitioning to class B



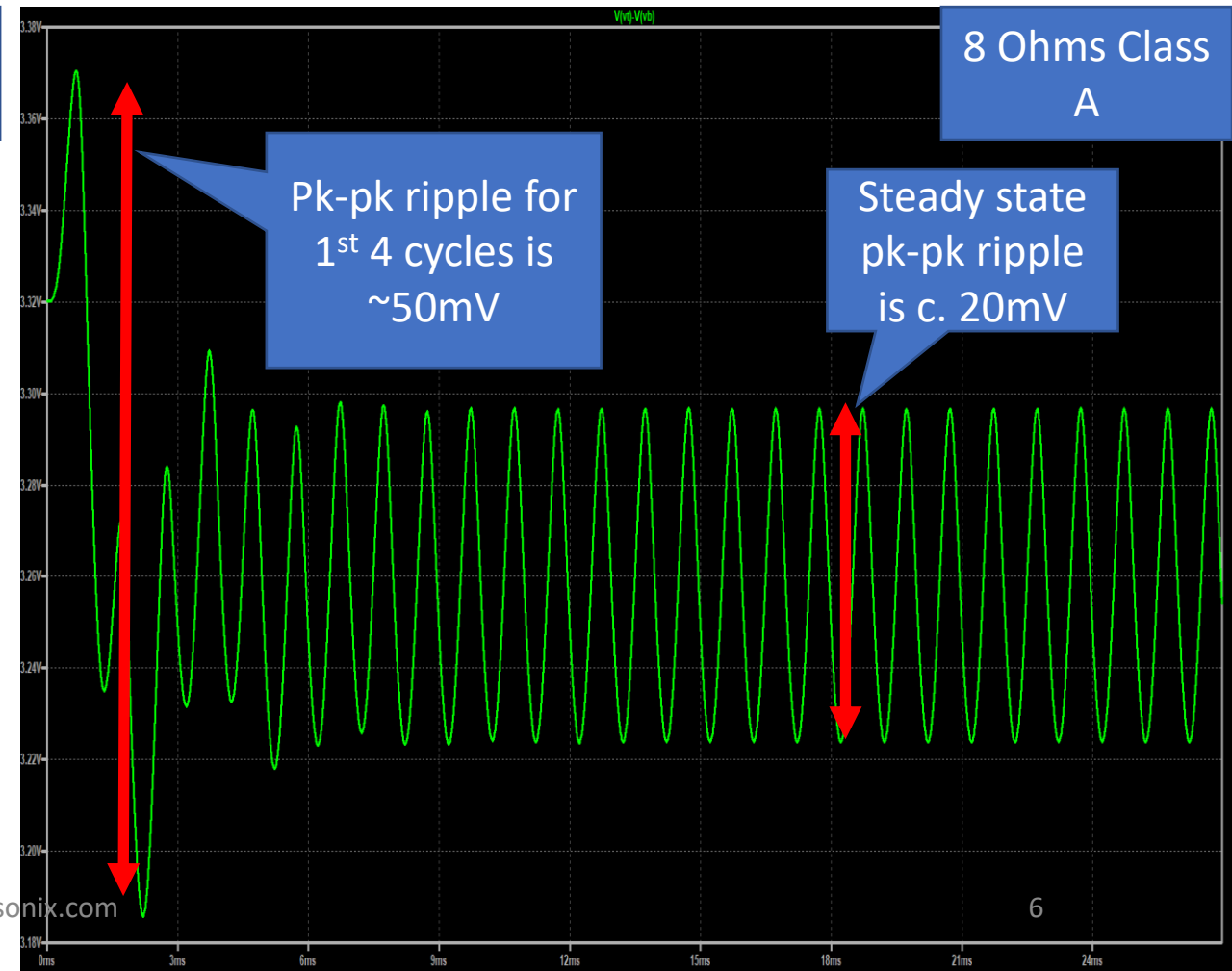
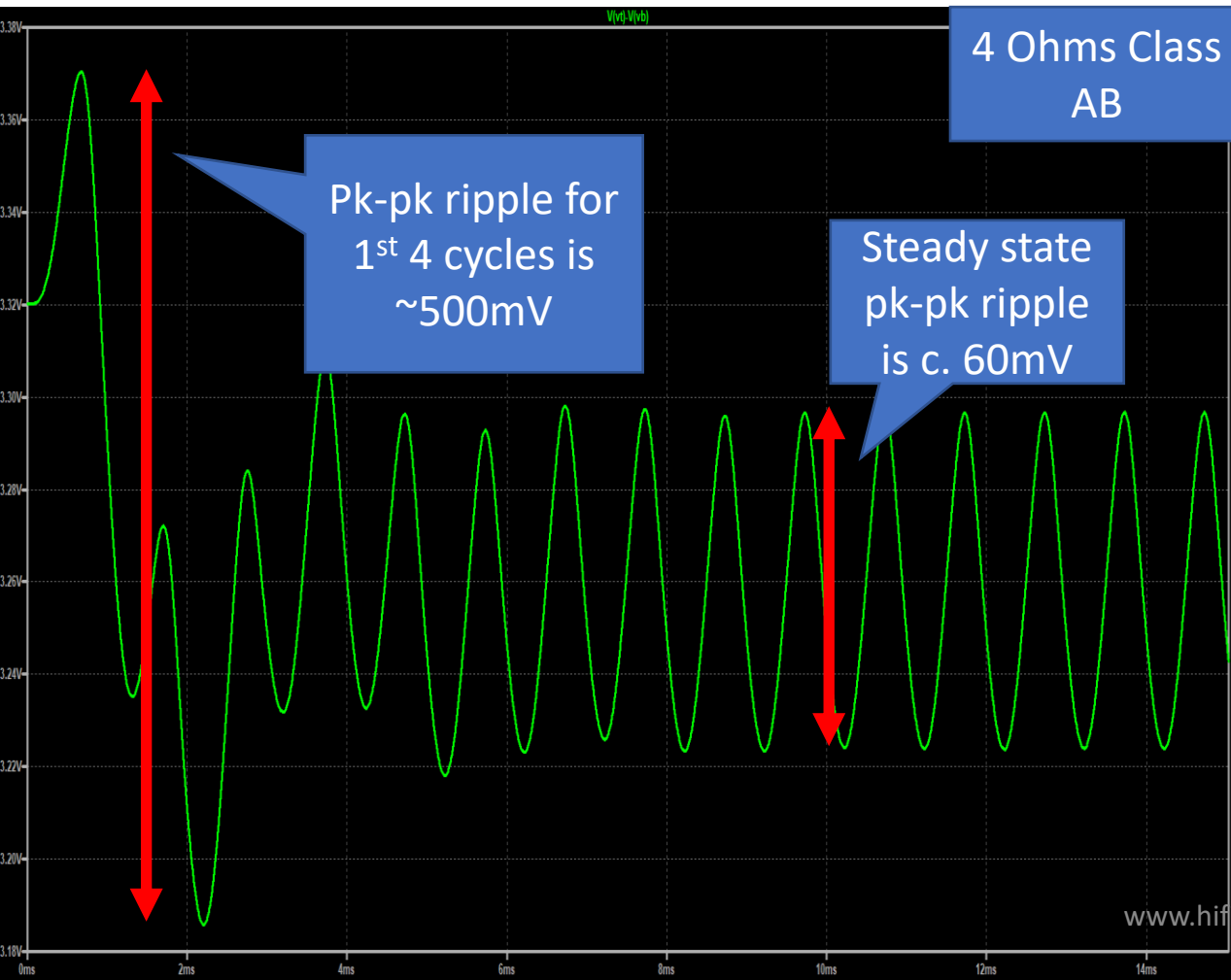
We go back to slide 1 but zoom into the differential voltage across the emitter degen resistors – this is the green trace below



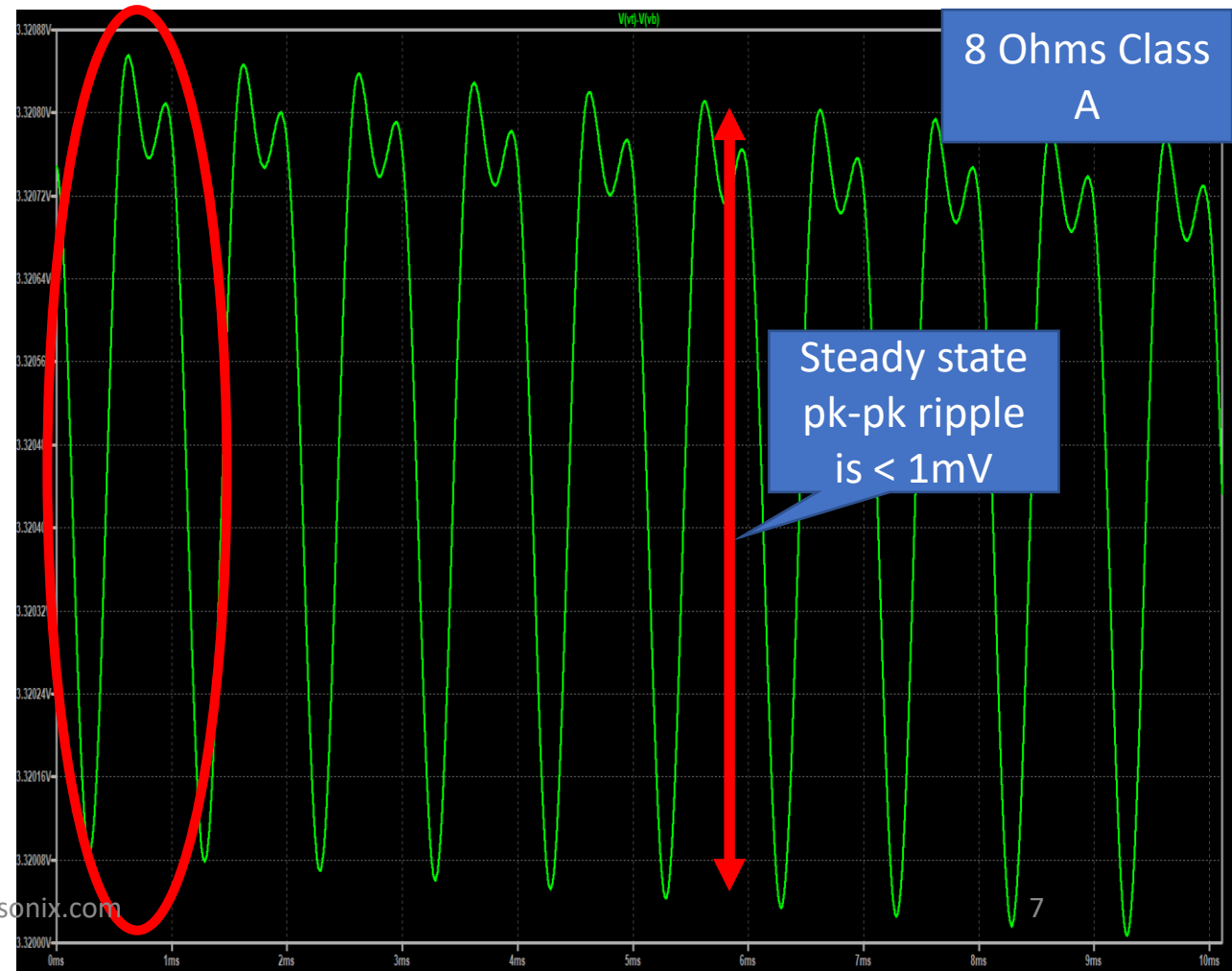
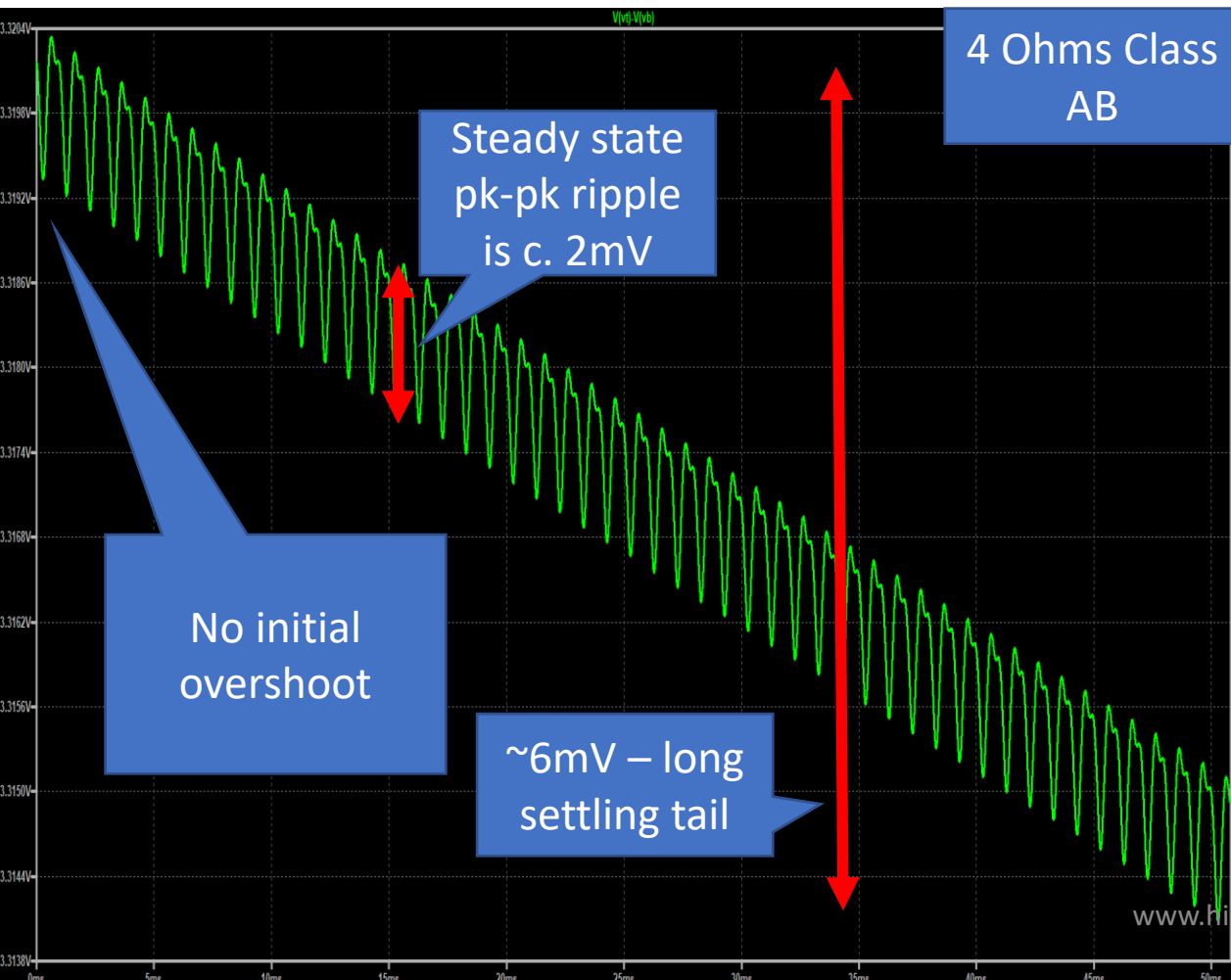
We go back to slide 1 but zoom into the differential voltage across the emitter degen resistors – this is the green trace below with C17 = 100uF (vs 0uF in the design)



We go back to slide 1 but zoom into the differential voltage across the bias controller C-E (Q3) C17 = 0uF (vs 0uF in the design)



We go back to slide 1 but zoom into the differential voltage across the bias controller C-E (Q3) C17 = 100uF (vs 0uF in the design). There is a small (about 7ppm at 20 kHz) distortion penalty with the addition of C17 = 100uF



As per the previous slide but C17 is now set to 0 pF again, but C5 is increased from 10uF to 100uF

