Why Miller effect does not necessarily increase the input capacitance of feedback amplifiers much

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Suppose you make a feedback amplifier with series feedback at the input, with a JFET input stage (although most of this document applies equally to bipolar junction transistors and triodes) and with lots of gain in the other stages of the active part of the amplifier for all signal frequencies of interest (lots of voltage, current, transadmittance and transimpedance gain to be precise). Suppose you are particularly interested in the input capacitance (or more generally the input admittance) of the amplifier over the signal frequency range of interest.

One might be inclined to take the opposite of the open-loop gain of the first stage, add one and multiply the gate-drain capacitance of the JFET by this number. That is, one might be inclined to use the Miller effect of the open-loop input stage to calculate the impact of the gate-drain capacitance on the closed-loop input impedance of the amplifier. As will be shown, this would be quite incorrect.

When the gain of the other stages is high enough, you can treat them as a nullor, also known as an ideal op-amp. That is, the input signal voltage and current of the second stage will then be negligibly small for any output signal level that doesn't cause clipping or slew-rate limiting, so that the input signal voltage and input signal current of the second stage can be approximated as zero. This leads to the two configurations shown in figure 1.

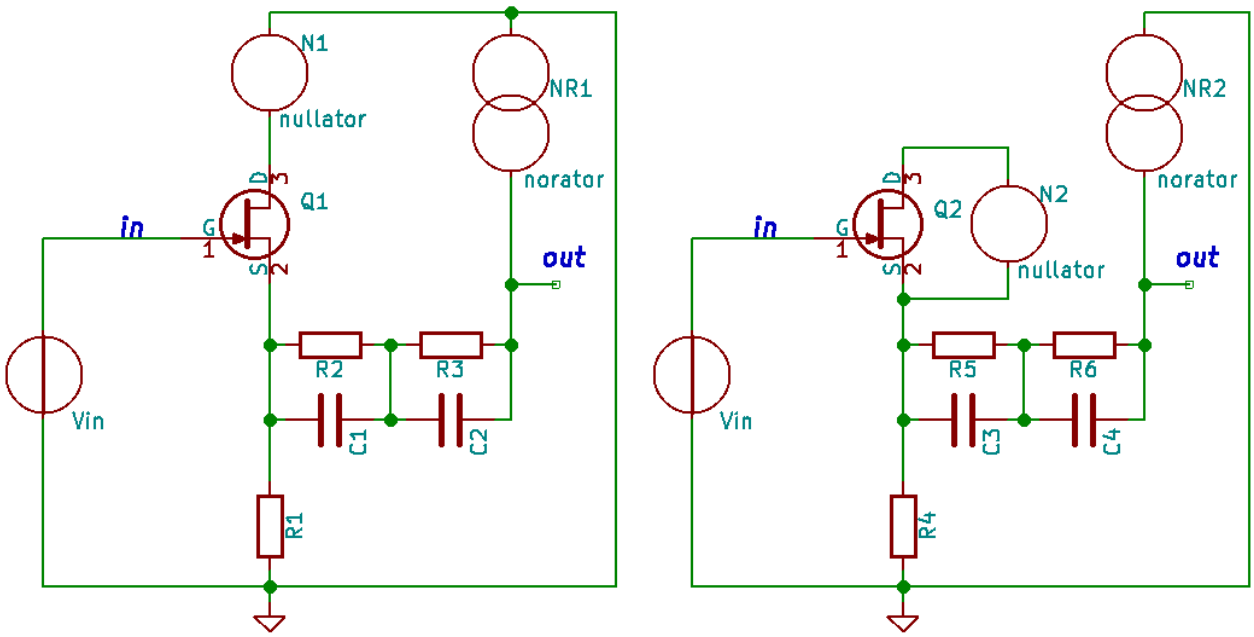

Figure 1. Two examples of feedback amplifiers of which the second and later stages are assumed to have nullor (ideal op-amp) behaviour. These are signal schematics, meaning that anything related to DC biasing is left out for simplicity. The nullators have zero voltage across them and conduct zero current (like an ideal op-amp input port), while the norators can have any voltage across them and conduct any current (like the output of an ideal op-amp). The JFETs are the input stages and the RC-networks are the feedback networks.

Looking at the left circuit, it is clear that the gate of Q_1 carries a signal voltage V_{in}. Its drain must be at a signal voltage of 0, because nullator N_1 has no voltage across it by definition. Hence, the signal voltage across the gate-drain capacitance of Q_1 is simply the input signal voltage, not an amplified version of it. The gate-drain capacitance of Q_1 does load the input, but without any Miller effect.

The gate-source capacitance of Q_1 has a small but non-zero loading effect on the input. Due to the overall feedback loop, the voltage at the source of Q_1 follows the voltage at its gate, but not perfectly due to channel length modulation of Q_1 (among other things). Hence, only a small fraction of the input voltage occurs between gate and source of Q_1, so the current through its gate-source capacitance is only a small fraction of $sC_{gs}V_{in}$. Stated otherwise, only a small fraction of Q_1's gate-source capacitance is seen at the input.

The right circuit has an even smaller input capacitance, theoretically even zero. Due to the different connection of the nullator, there is no signal voltage occuring between Q_2's drain and source and no signal current flowing through its drain. That means that Q_2 has no signal excursions at all, so its gate-source and gate-drain voltages also have to remain constant. Hence, there is no signal current flowing into its gate.

Impact of finite gain

So far the assumption has been made that the second and later stages behave as a nullor. Things get more complicated and less ideal when they have a large but finite gain. For simplicity, we will only consider a finite voltage gain. That implies that the input signal current of the second stage will remain zero.

The closed-loop transfer from the amplifier input to its output will be called $H_{cl}(s)$. The open-loop gain of the second and further stages will be called $-G_{2+}(s)$, where the minus sign is a reminder that the second and further stages will have to invert to get negative rather than positive feedback.

In this finite-gain case, the voltage at the drain of Q_1 will be $-V_{in}H_{cl}(s)/G_{2+}(s)$ rather than zero. This follows from a simple anti-causal calculation: dividing the output voltage $V_{in}H_{cl}(s)$ of the amplifier by the gain of the second and further stages $-G_{2+}(s)$. Hence, the voltage across the gate-drain capacitance will be $V_{in} - (-V_{in}H_{cl}(s)/G_{2+}(s)) = V_{in}\,(1 + H_{cl}(s)/G_{2+}(s))$ and the current through it will be $sC_{gd}V_{in}\,(1 + H_{cl}(s)/G_{2+}(s))$.

When $H_{cl}(s)$ and $G_{2+}(s)$ have a frequency-independent ratio, the contribution of Q_1's gate-drain capacitance to the amplifier's input capacitance will increase from C_{gd} to $C_{gd}(1 + H_{cl}(s)/G_{2+}(s))$. There is a kind of Miller effect, but it is determined by the ratio of the closed-loop gain to the open-loop gain of the second and further stages, rather than by the open-loop gain of the first stage.

To a decent approximation, a similar story applies to Q_2. The contribution of Q_2's gate-drain capacitance to the right amplifier's input capacitance will increase from 0 to approximately $C_{gd}H_{cl}(s)/G_{2+}(s)$ when the open-loop voltage gain of the second and later stages is finite.

It should be noted that the extra input admittance term need not be capacitive. When the ratio between $H_{cl}(s)$ and $G_{2+}(s)$ is not frequency independent, $sC_{gd}H_{cl}(s)/G_{2+}(s)$ is not a capacitive admittance. As an example, suppose we are interested in the input impedance of a RIAA amplifier at audio frequencies above the highest RIAA corner frequency (which is approximately 2122 Hz, or

exactly $1/(2\ \pi\ 75\ \mu s)$) and that $G_{2+}(s)$ is approximately constant and equal to $G_{2+}(0)$ over the audio band. The RIAA response is approximately inversely proportional to frequency above the highest RIAA corner frequency, so $H_{cl}(s) \approx K/s$ with K being some constant. In this case, $sC_{gd}H_{cl}(s)/G_{2+}(s) \approx C_{gd}K/G_{2+}(0)$, which corresponds to a resistor with value $G_{2+}(0)/(C_{gd}K)$ in parallel with the input.

It should also be noted that the calculation methods in this document are useless when you want to calculate the loop gain of an amplifier, as they only apply to the closed-loop behaviour.