Short Papers

An Improved FET Model for Computer Simulators

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Abstract—**An alternative simple description of FET drain current provides the flexibility of an extra parameter which can be chosen to approximate the Shockley expression or general power law. An empirical polynomial expression which uses only integer powers is used to provide computational efficiency. The new expression gives the designer a more accurate FET model which is consistent for both large- and small-signal simulations.**

The JFET and level 1 MOSFET dc models in SPICE [1] use a simple square-law relation which often does not precisely fit real device transfer characteristics. The predicted small-signal behavior is valid only in regions where the square-law matches measured large-signal behavior. Designers using SPICE often have to make adjustments to circuit bias points or device parameters to reconcile any differences. Better results can be achieved with general power law relations [2] or the Shockley equation [3], but these are not desirable in software simulators because they are computationally intensive expressions. Thus there is a need for an expression which is computationally simple and yet provides an accurate fit to measured data.

Here we describe an improved simple description of FET drain current which provides the flexibility of an extra parameter that can be chosen to approximate the Shockley expression. This parameter is easily fitted to measured data in the same way as the exponent in Richer and Middlebrook's general power law relation [2]. The new expression gives the designer a more accurate FET model which is consistent for both large- and small-signal simulations.

Recall that the basic FET has between source and drain electrodes a doped semiconductor channel which is controlled by depleting the channel region under a gate electrode with a gate–source bias, V_{gs}. The device operates in three modes. In the linear mode, the drain–source current, I_{ds}, is proportional to the drain–source voltage, V_{ds}. As V_{ds} increases, the device enters the saturated mode where the current ceases to rise, because at the drain end, the channel is completely depleted, or pinched-off. The third mode is a cutoff mode where no current flows because the channel is completely depleted.

As used in the Shichmann–Hodges model [4], Shockley's expression is generally accepted as the standard description of FET drain current. The drain current in the linear mode is

$$I_{ds} = \beta(\phi_b - V_{to})^2\{3(d^2 - s^2) - 2(d^3 - s^3)\} \quad (1)$$

where $s = \sqrt{(\phi_b - V_{gs})/(\phi_b - V_{to})}$ and $d = \sqrt{(\phi_b - V_{gs} + V_{ds})/(\phi_b - V_{to})}$ are the extents of channel depletion at the source and drain ends, respectively, V_{to} (volts) is the gate–source potential required to deplete the whole channel of carriers, and ϕ_b is the gate junction built-in potential (volts). The use of a half-power-law for the terms s and d is derived by assuming uniform doping profile in the channel.

An alternate model is the general power law of order n. The drain current in the saturated mode is empirically derived, and is justified by its flexibility and good fit to real devices [2]:

$$I_{ds} = \beta\{V_{gs} - V_{to}\}^n. \quad (2)$$

The exponent term gives the degree of freedom required to fit the model to nonuniform doping profile. Like the Shockley relation, this requires a nonintegral power function which renders it unattractive for software circuit simulators.

The simple three-mode model used in SPICE is based on a square-law function of gate bias which can be derived by assuming the electric field is constant along the channel [5]:

cutoff mode, $V_{to} \geq V_{gs}$,

$$I_{ds} = 0 \quad (3a)$$

linear mode, $V_{to} < V_{gs}$ and $V_{ds} \leq (V_{gs} - V_{to})$,

$$I_{ds} = \beta(1 + \lambda V_{ds})V_{ds}\{2(V_{gs} - V_{to}) - V_{ds}\} \quad (3b)$$

saturated mode, $V_{to} < V_{gs}$ and $V_{ds} > (V_{gs} - V_{to})$,

$$I_{ds} = \beta(1 + \lambda V_{ds})(V_{gs} - V_{to})^2 \quad (3c)$$

where $\beta(A \cdot V^{-2})$ is a transconductance parameter and $\lambda(V^{-1})$ is a channel-length modulation parameter. This expression is computationally efficient but does not provide as good an agreement, with real devices as a general power law or the Shockley expression.

Our alternative model is derived from the Shockley expression by applying a third-order Taylor expansion to the radical terms, d^3 and s^3, in (1). Like terms are collected and their coefficients replaced by constants A and B. The result is a simple extension to the SPICE relation:

cutoff mode, $$I_{ds} = 0 \quad (4a)$$

linear mode, $$I_{ds} = \beta(1 + \lambda V_{ds})V_{ds}\{B(2V_g - V_{gs}) + A[V_{ds}^2 + 3V_g(V_g - V_{ds})]\} \quad (4b)$$

saturation mode, $$I_{ds} = \beta(1 + \lambda V_{ds})V_g^2\{B + AV_g\} \quad (4c)$$

where $V_g = V_{gs} - V_{to}$, $A = (1 - B)/(\phi_b - V_{to})$, and $0 \leq B \leq 1.2$ is a fitting parameter. The range of B is restricted to eliminate regions of alternate transconductance.

A convenient degree of freedom is provided by the term, B, which can be considered as the "doping profile parameter" because it allows deviation from Shockley's uniform doping assump-

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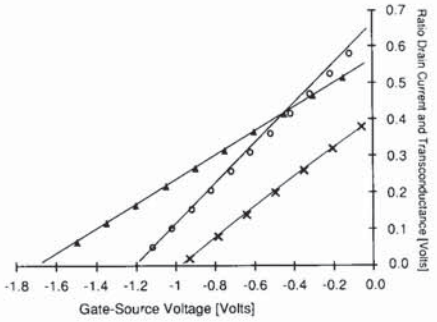

Fig. 1. The similarity of the new model to a general power law, solid lines, is shown for $n = 3$; (▲), $n = 2.4$; (×), and $n = 1.8$; (○). In all cases, $\phi_b = 0.7$ V, although the sensitivity to this parameter is very low.

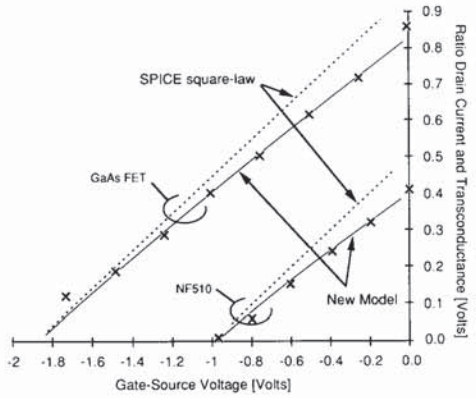

Fig. 2. The new model is a much better fit to experimental data: (×), than the square-law SPICE model. The FET's shown in Figs. 3 and 4, follow power laws with exponents, $n = 2.34$ and 2.39 and pinch-off potentials, $V_{to} = -1.89$ and -0.98 V, respectively.

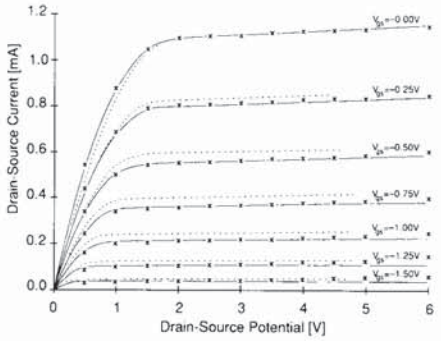

Fig. 3. The experimental data: (×), is shown for a GaAs FET with gate length 100 μm and width, 200 μm. The new model (4) is shown by solid lines with parameters $\beta = 330\ \mu A \cdot V^{-2}$, $V_{to} = -1.89$ V, $B = 0.66$, $\lambda = 13\ mV^{-1}$, and $\phi_b = 0.7$ V. This provides a better fit than the square-law SPICE model, (· · · · ·), with parameters $\beta = 299\ \mu A \cdot V^{-2}$, $V_{to} = -1.89$ V, and $\lambda = 13\ mV^{-1}$.

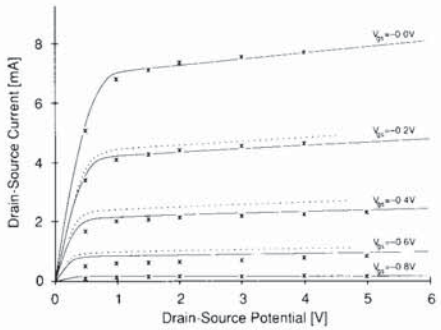

Fig. 4. The experimental data, (×), is shown for a silicon FET type NF510. The new model, (4), is shown by solid lines with parameters β = 9.15 mA · V^{-2}, V_{to} = −0.95 V, B = 0.623, λ = 30 mV^{-1}, and ϕ_b = 0.7 V. The square-law SPICE model: (· · · · · ·), uses parameters β = 7.68 mA · V^{-2}, V_{to} = −0.95 V, and λ = 30 mV^{-1}.

tion. When B is set to 1, the original SPICE square law is exactly implemented and when B is set to 0.60, the model is a very close approximation to the Shockley expression. Typical values of B range from 0.3 to 0.4 for a doping profile with an extended tail, through 0.6 for a uniform profile, to 0.9–1.1 for a negative gradient profile.

The essential features of a FET model are present in the new expression. The model is a well-behaved differentiable function and crosses the device's operating mode boundaries smoothly. The drain conductance at saturation and the transconductance at pinch-off are zero as expected. Also, the small-signal transconductance, g_m, and zero bias drain–source conductance, G_{dso}, are equal so the model still obeys the known result that "the transconductance at zero-gate voltage is equal to the total channel conductance in the absence of the gate structure" [4]:

$$g_m = G_{ds}\big|_{V_{ds}=0} = \beta V_g\{2B + 3AV_g\}. \tag{5}$$

In fact, the new expression for saturated drain current, (4c), very closely follows a general power law relation of order $n = (3 - B)$. This can be demonstrated with a property of a general power law expression that Richer and Middlebrook [2] used and supported with measured data. That is, the ratio of the saturated drain current and transconductance is a linear function of gate bias:

$$\frac{I_{ds}}{g_m} = \frac{\beta V_g^2\{B + AV_g\}}{\beta V_g\{2B + 3AV_g\}} \approx \frac{1}{3 - B}(V_{gs} - V_{to}). \tag{6}$$

As shown in Fig. 1 the approximation (6) is very close. Thus the validity of the new model is substantiated by its resemblance to the already justified general power law. The advantage of the new expression is that it does not use a computationally intensive radical function.

When applying the new model to measured data, the necessary parameters can be easily determined once the effects of drain and source parasitic resistances are removed. The pinch-off voltage and doping profile parameters can be graphically determined from a plot of the ratio of drain current to transconductance [2]. The channel-length modulation parameter can be determined from the saturated mode drain–source conductance and the transconductance parameter chosen for best fit.

Application of both the SPICE square-law model and the new model to measured data is shown in Figs. 3 and 4. A silicon FET type NF510 and a Gallium Arsenide (GaAs) Schottky barrier FET (MESFET) of planar construction with gate dimensions 100 μm long by 200 μm wide were used. The ratio of saturated drain current and transconductance of these device is shown in Fig. 2 and from this, the doping profile and pinch-off parameters were determined. Note that the departure of the ratio from the straight line near pinch-off is due to drain leakage current.

It can be seen that applying the new model gives an excellent fit to the experimental data. The square-law model is not as good but still provides a reasonable large-signal model. Of more significance is the inability of the square law to properly relate the small-signal transconductance to drain current as shown in Fig. 2. To use the square-law model, it is necessary before performing a simulation to select the pinch-off potential and transconductance parameters to suit the purpose of the simulation. A best fit to the large-signal behavior can correctly predict the operating point but not necessarily the small-signal gain at that point. Before performing a small-signal analysis the model parameters must be adjusted or the bias point moved to a region with correct small-signal gain.

The advantage of the new model over the square-law model is that it can more accurately fit the large-signal behavior of a device, and therefore, consistently predict small-signal behavior over an extended operating range. It can correctly relate the small-signal transconductance to drain current and so eliminate the need for inconvenient juggling between large- and small-signal model parameters.

In summary, an improved JFET model suitable for computer simulators has been presented. It uses a simple polynomial extension of the existing SPICE model which allows a very good fit to the standard Shockley expression and also features the flexibility of a general power-law without using a computationally intensive radical function. There is an extra degree of freedom in the form of the "doping profile parameter" which allows the model to correctly relate small- and large-signal behavior.

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