

Distortion in JFET Amplifiers

by Kenneth A. Kuhn
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Introduction

This note discusses distortion in JFET amplifiers and how to operate a JFET amplifier with low distortion. JFETs are typically used in the first stage of an amplifier where the signal amplitude is so small (microvolts up to maybe a few millivolts) that nonlinear effects are negligible. The distortion becomes significant at larger amplitudes where JFETs are not normally used – at least in open-loop applications. It is important to understand the operating conditions that separate the preferred linear from non-linear regions.

JFET transfer function

A JFET has a square-law transfer function that is not linear as shown in Equation 1 which has been normalized to be more general than the usual equation.

$$\frac{I_D}{I_{DSS}} = \left(1 - \frac{V_{GS}}{V_P} \right)^2 \quad \text{Eq. 1}$$

where

I_D is the drain current

I_{DSS} is the drain saturation current

V_{GS} is the voltage between the source and gate terminals

V_P is the pinch-off voltage

It should be noted that (I_D/I_{DSS}) varies from 0 to 1 as (V_{GS}/V_P) varies from 1 to 0.

The transfer gain is the derivative of the output current with respect to the input voltage and has units of transconductance, abbreviated as gm. The normalized derivative (several steps are omitted as those are discussed in another note) of Equation 1 is

$$\frac{g_m}{g_{mo}} = 1 - \frac{V_{GS}}{V_P} \quad \text{Eq. 2}$$

where

g_m is the transconductance gain of the JFET

g_{mo} is the transconductance gain (highest gain possible) of the JFET at zero bias

It should be noted that (g_m/g_{mo}) varies from 1 to 0 as (V_{GS}/V_P) varies from 0 to 1.

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A plot of Equation 1 and Equation 2 is shown in Figure 1. Note that the gain is a function of the bias voltage. This means that if the input signal is of significant amplitude then the gain will vary with the input signal thus causing distortion. For very small signals this effect is negligible but becomes significant for larger signals and distortion is the result. It is useful to know how much distortion occurs with a given signal amplitude.

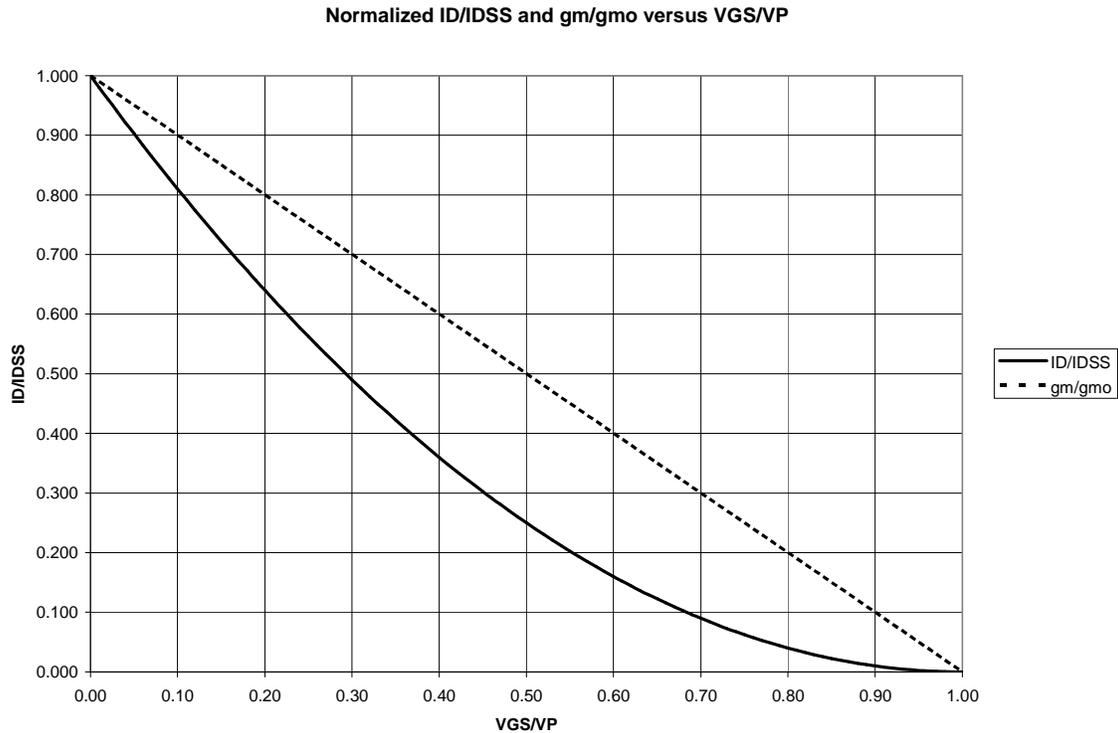


Figure 1: Normalized transfer functions of a JFET

The following series of plots show the normalized drain current in response to a sine wave input signal. The normalized bias line (I_D/I_{DSS}) is shown for reference. The signal amplitude shown is such that V_{GS} goes to zero (i.e. I_D goes to I_{DSS}) at the negative peak of the sine wave. This is the largest possible signal and which will have the most distortion for a given bias level (V_{GS}/V_P) not greater than one half. For higher bias levels (i.e. lower drain current) the limit would have to be such that V_{GS} did not exceed V_P . Thus, in all examples the peak drain current is I_{DSS} (which has been normalized to 1.0). Obviously, using a smaller amplitude signal would result in lower distortion but the purpose here is to show distortion.

The theoretical undistorted sine wave output is shown for reference and the difference (i.e. distortion) between the actual and the reference is shown at the bottom of the plot. The distortion signal here is purely second order (i.e. at twice the fundamental frequency). A real JFET has an exponent of roughly two (as opposed to exactly two as used in the mathematical model) and will show higher order distortion signals but the second order term remains dominant.

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Distortion (in percent) is calculated as:

$$\text{Distortion} = \frac{\text{rms amplitude of distortion signal}}{\text{rms amplitude of undistorted signal}} * 100\% \quad \text{Eq. 3}$$

This definition is analogous to the notch filter method of measuring distortion in which the amplitude of the signal with the fundamental notched out is divided by the amplitude of the signal including the fundamental. The approach used here is because the data is readily available in the spreadsheet. The amplitude of the undistorted signal is not directly available in the real world.

The first example shown in Figure 2 is the extreme with one hundred percent modulation of the drain current. It helps to refer to Figure 1 and imagine an operating point at $(V_{GS}/V_P) = 0.5$ and a sine wave signal with a peak-peak amplitude of 1.0 at the gate. Thus, the normalized gate voltage will swing from 0 to 1 (note: V_{GS}/V_P will always be a positive value) and the normalized drain current will swing from 1 down to 0 as shown on the transfer curve. The distortion signal is the difference between the actual and the theoretical undistorted drain current. Distortion is very obvious here and computes to be 25 percent – the theoretical undistorted sine wave has a peak-peak value of 1.0 and the distortion signal has a peak-peak value of 0.25. In reality the rms values are used (the only way to do it correctly) but the peak-peak values are easily seen here.

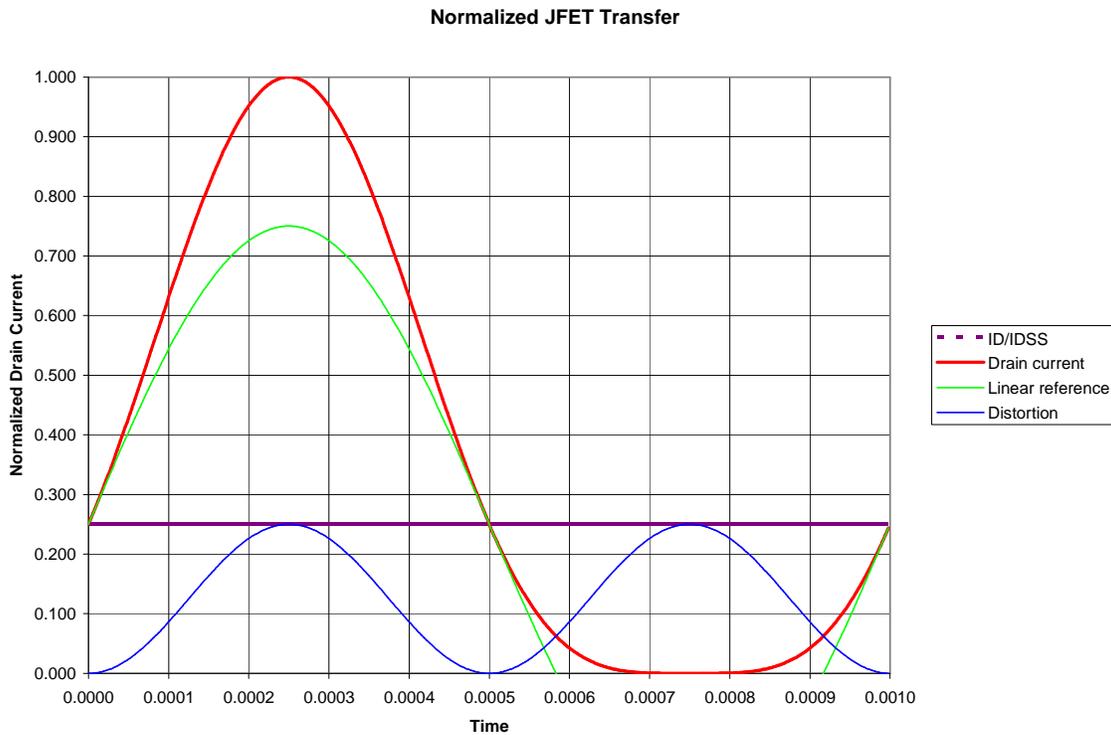


Figure 2: Fully modulated drain current. Distortion is 25%

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Figure 3 shows a less extreme case but the distortion is still in the considerable range. Note the non-symmetry of the sine wave peaks. Ten percent distortion is very visible. Anybody should be able to observe that the waveform is not purely sinusoidal.

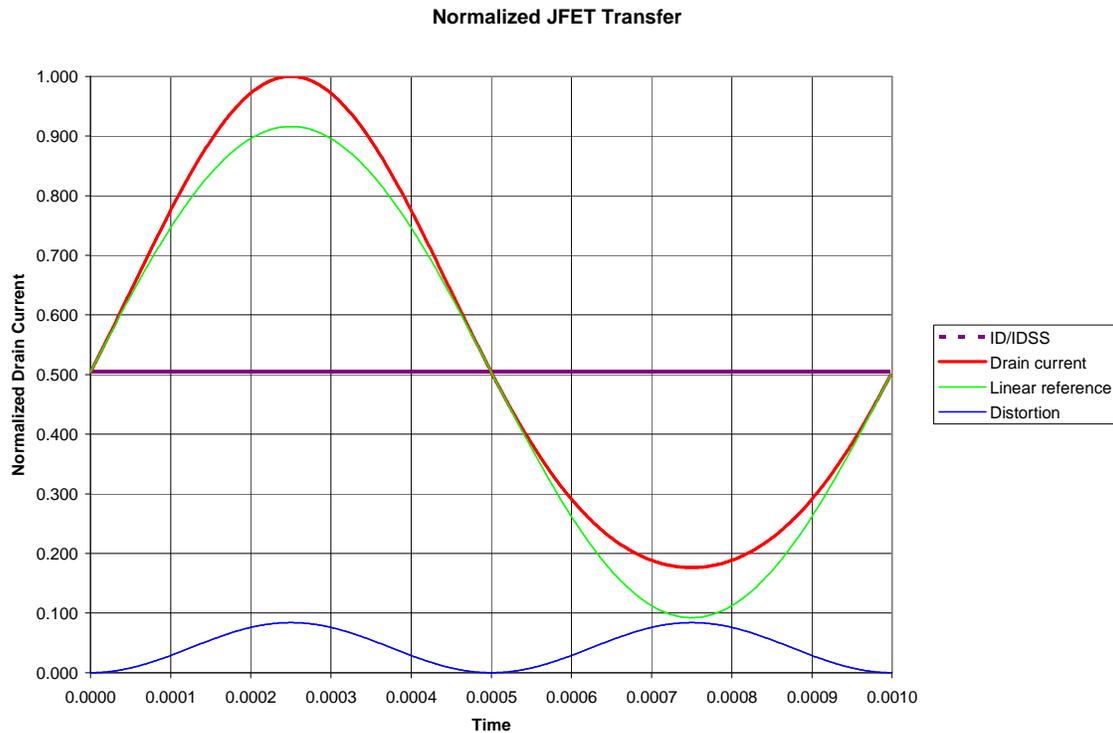


Figure 3: JFET operating at 50% I_{DSS} drain current. Distortion is 10%

Figures 4 and 5 show lower distortion as the bias point is moved towards I_{DSS} . Note that the distortion in Figure 4 is not visually discernable to most people but the level of four percent is definitely audible although it might not be troublesome to many people. Very few people can visually identify the distortion in Figure 5. A distortion of two percent (-34 dB) is audible to most people with sine wave testing but is not usually considered bothersome except to purists. It takes a trained ear or special scenarios to detect distortion of this level in musical or voice waveforms. Audio is generally considered to be high quality when the distortion is -50 dB or better. Purists advocate more than -80 dB but it is debatable whether anyone (including purists) can reliably detect distortion at the -50 dB level in real music. With trained ears and specially rigged tests it is possible to detect distortion at extreme low levels.

The drain currents shown in Figures 4 and 5 are the typical design values in real amplifiers. That is – design for around 80 percent, give or take, of I_{DSS} . This value of drain current permits adequate linear signal swing while providing most of the available gain of the JFET.

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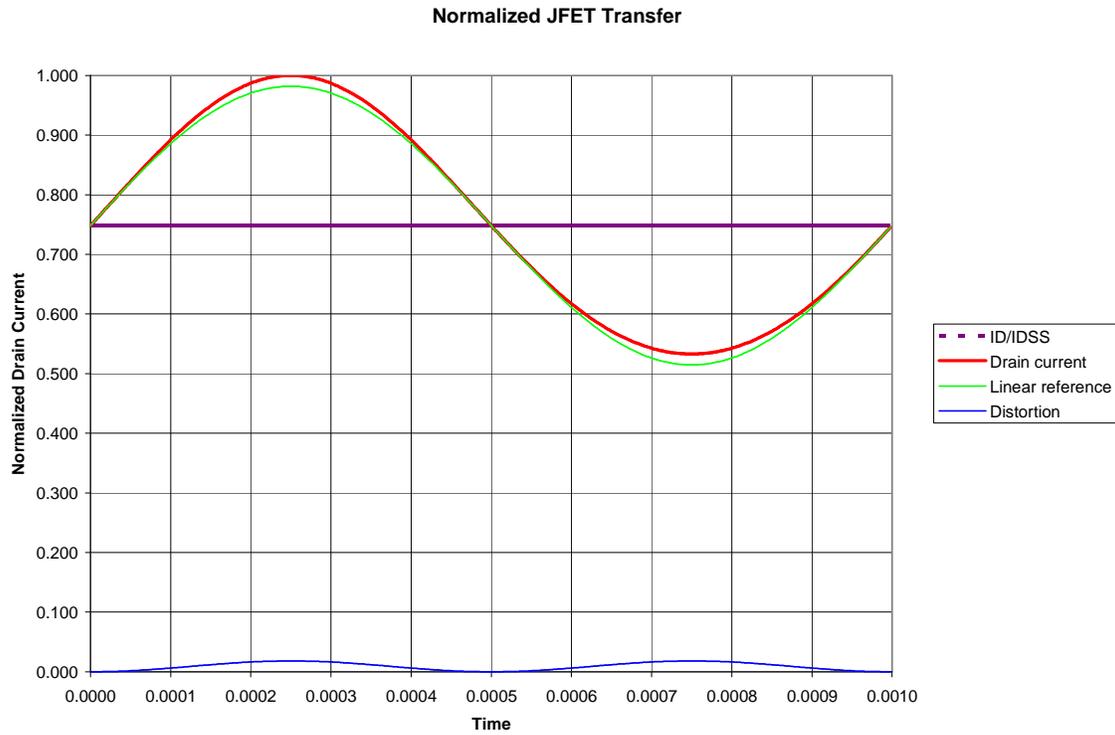


Figure 4: JFET operating at 75% IDSS drain current. Distortion is 4%

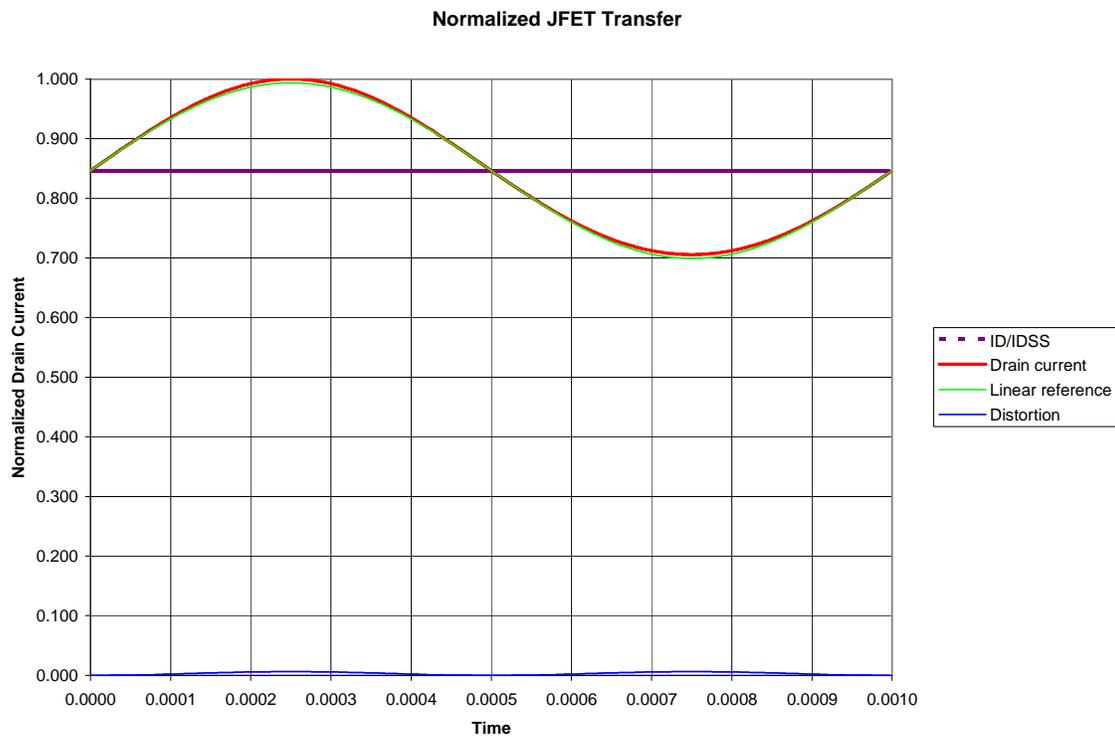


Figure 5: JFET operating at 85% IDSS drain current. Distortion is 2%

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The following plots show the waveform at the drain terminal of a common-source amplifier with various levels of distortion. Note that the waveforms are inverted from the current waveforms in previous figures to take into account what happens with the drain current through the drain resistor. These waveforms are shown because that is where distortion is usually observed. View these figures to calibrate your eye.

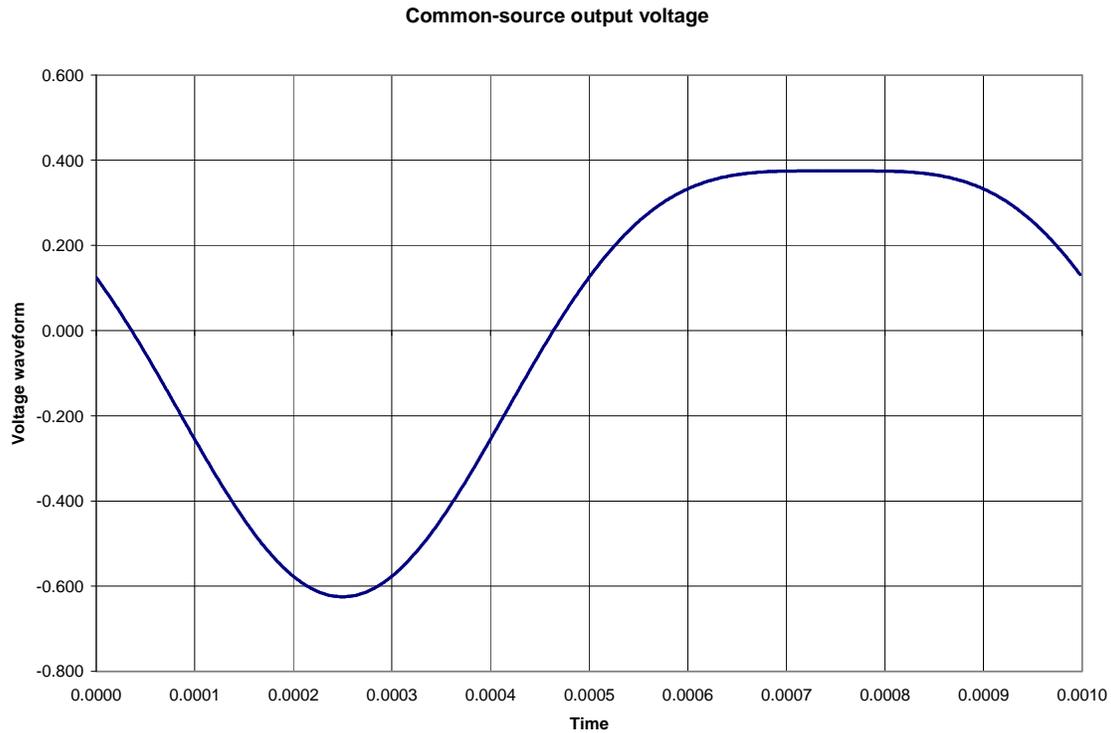


Figure 6: Drain voltage waveform at 25% distortion

The example in Figure 6 is the extreme as discussed earlier. The ten percent distortion in Figure 7 should be very obvious. It may take a little practice to reliably spot distortion at the five percent level shown in Figure 8 but the key is to observe the squashed appearance of one of the sine wave peaks while observing that the other peak is sharper than a pure sine wave. The three percent distortion shown in Figure 9 is definitely visible to a trained eye. The one percent distortion shown in Figure 10 is generally too small to detect by the majority of people even with trained eyes.

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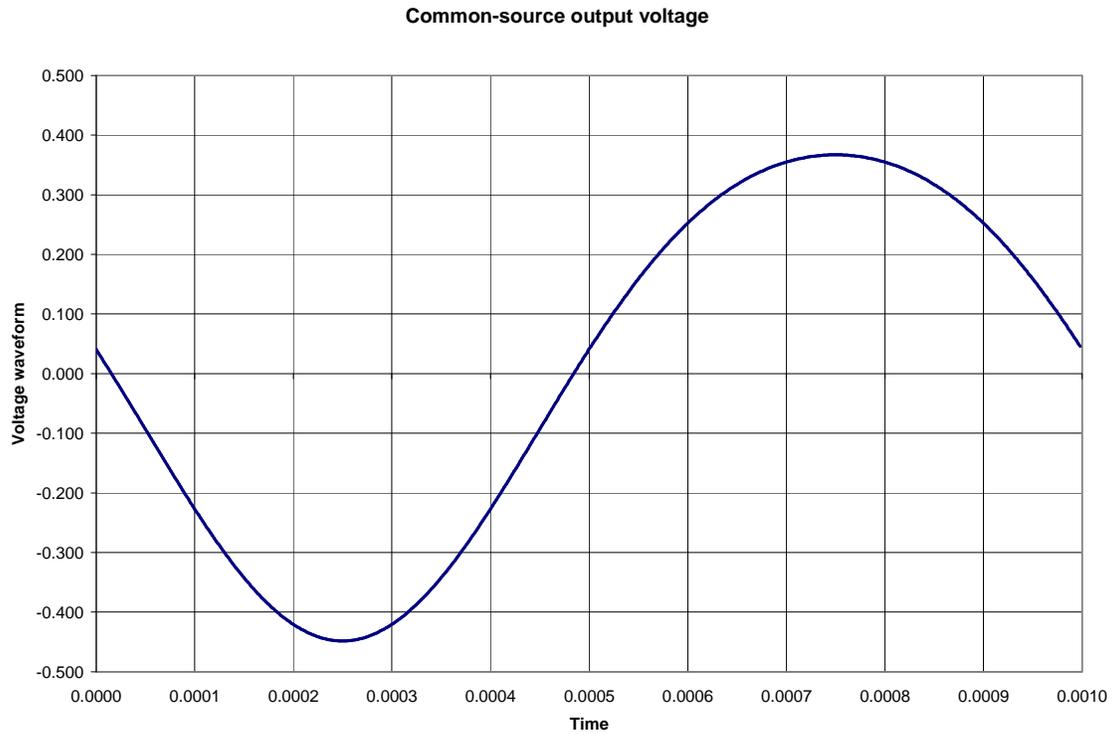


Figure 7: Drain voltage waveform at 10% distortion

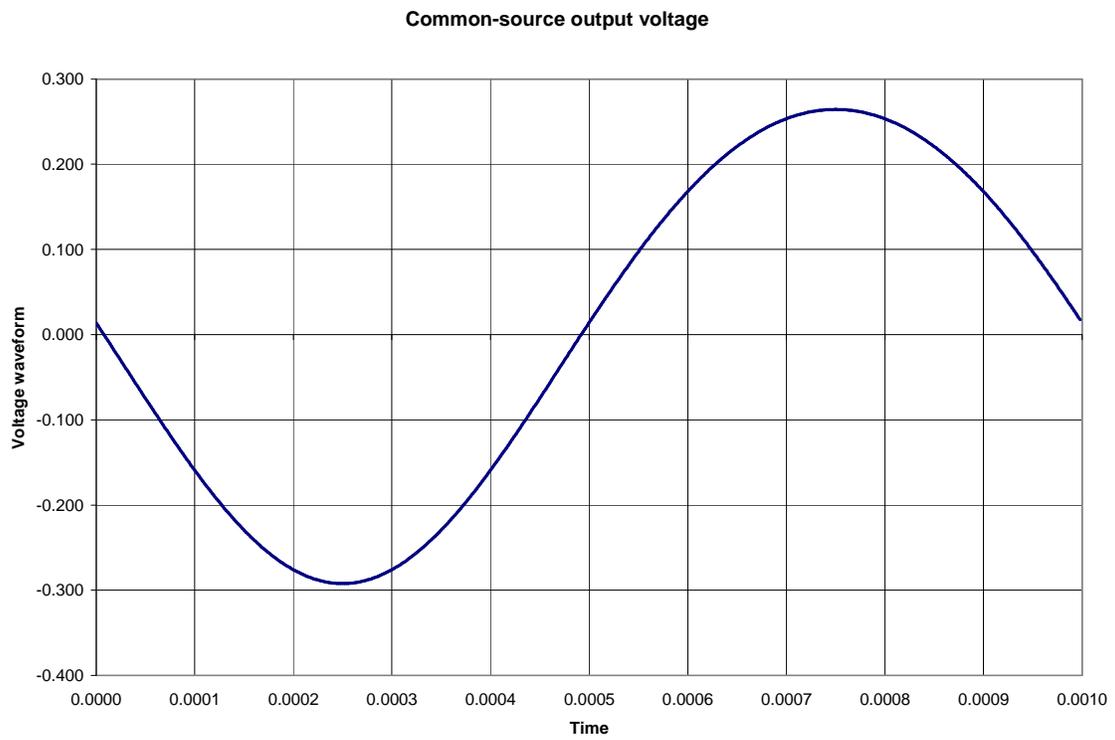


Figure 8: Drain voltage waveform at 5% distortion

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Figure 9: Drain voltage waveform at 3% distortion

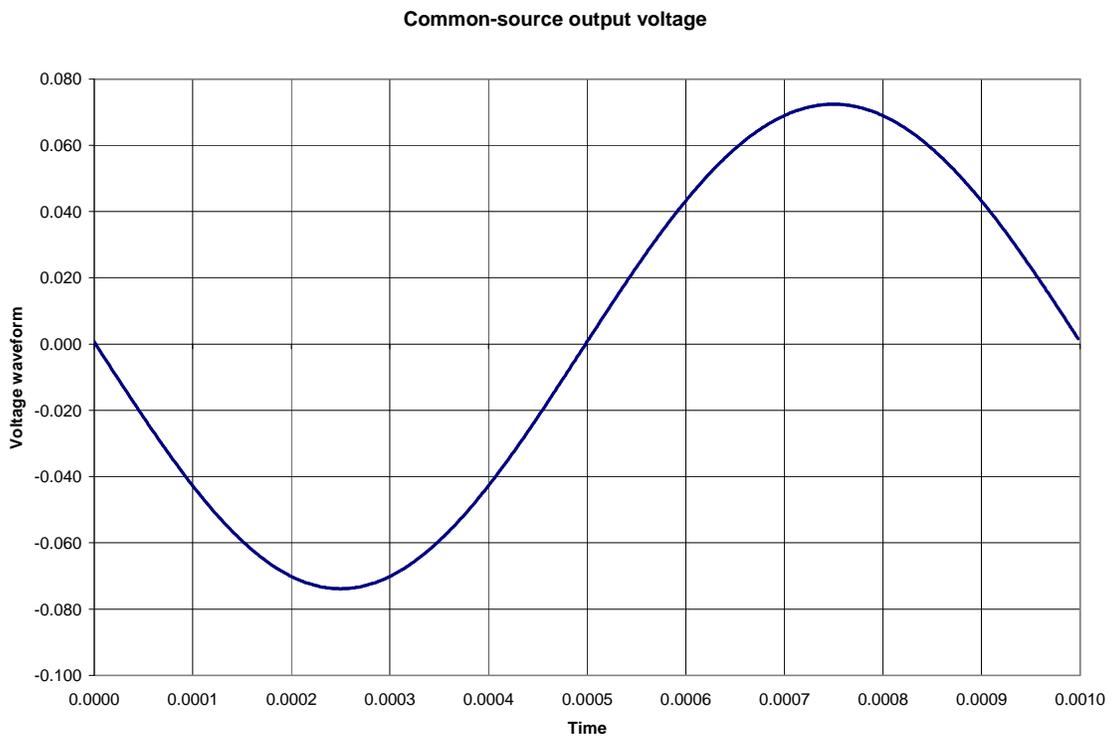


Figure 10: Drain voltage waveform at 1% distortion

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Figure 11 shows the distortion that occurs with a full amplitude signal as a function of the bias factor, V_{GS}/V_P . This curve suggests that the bias factor should be in the 0.1 range which corresponds to a quiescent drain current of about 80 percent of I_{DSS} .

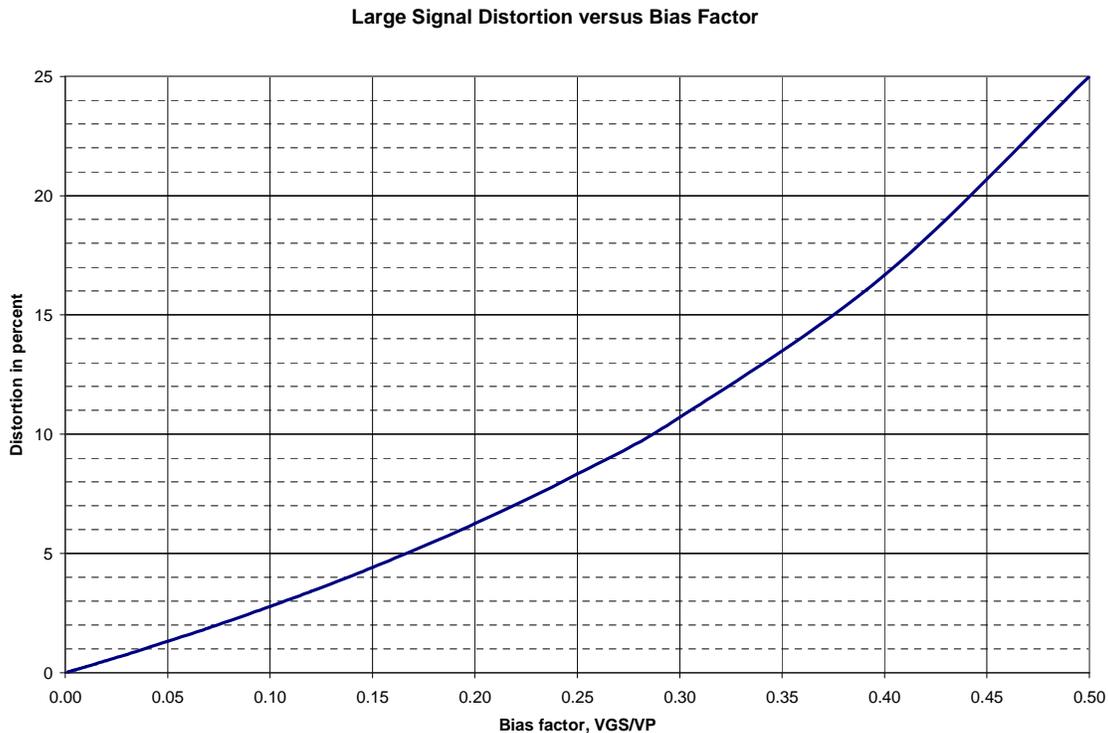


Figure 11: Large signal distortion versus bias factor

Figure 12 shows the maximum input signal (as a ratio of V_{inpp} to V_P) that can be applied to a JFET amplifier for a given level of distortion and as a function of the bias factor. The signal amplitude is limited on the left hand side so that V_{GS} does not exceed zero. The curve shows that the optimum bias points for large signals with minimum distortion is for V_{GS}/V_P to be in the 0.1 to 0.3 range. This corresponds to I_D/I_{DSS} in the 0.8 to 0.5 range. An important result from Figure 12 is that the peak-peak signal across the gate-source junction should be less than one tenth of V_P to keep distortion low.

Figure 13 shows the corresponding output peak-peak current factor on I_{DSS} . This chart is very useful for estimating the maximum output signal for a given distortion level. This chart is intended for common-source amplifiers and the peak-peak output voltage can be obtained by multiplying the peak-peak drain current by the resistance of the drain resistor in parallel with the load resistor.

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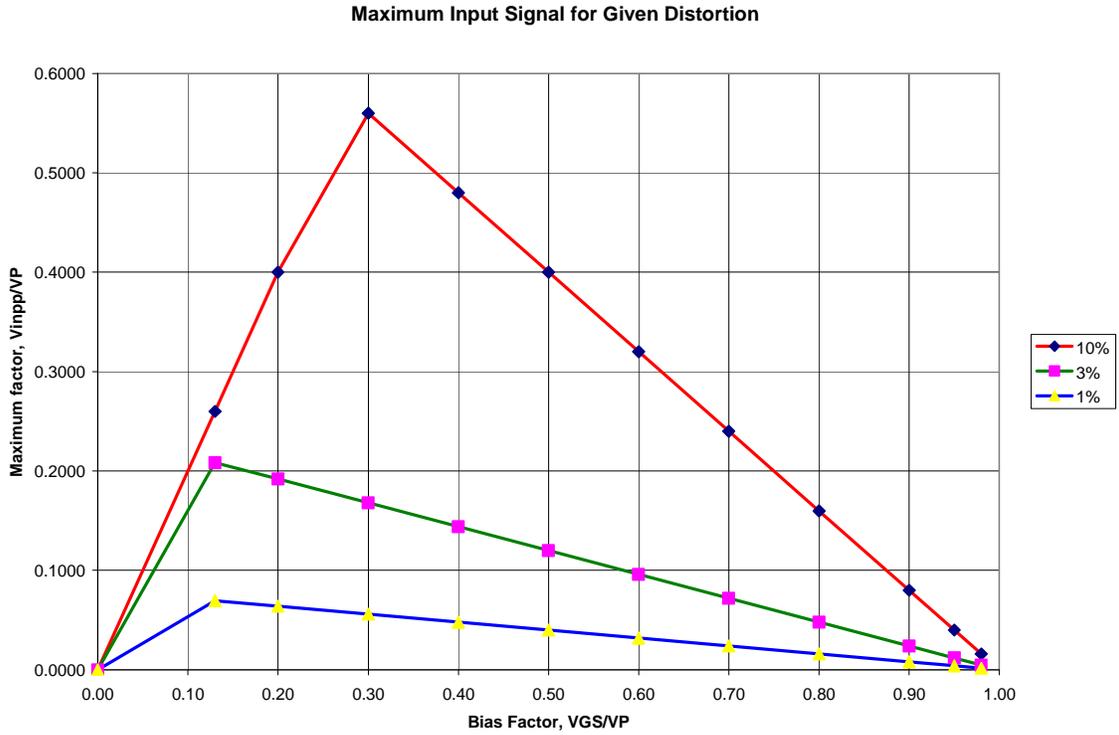


Figure 12: Maximum Input Signal for Given Distortion

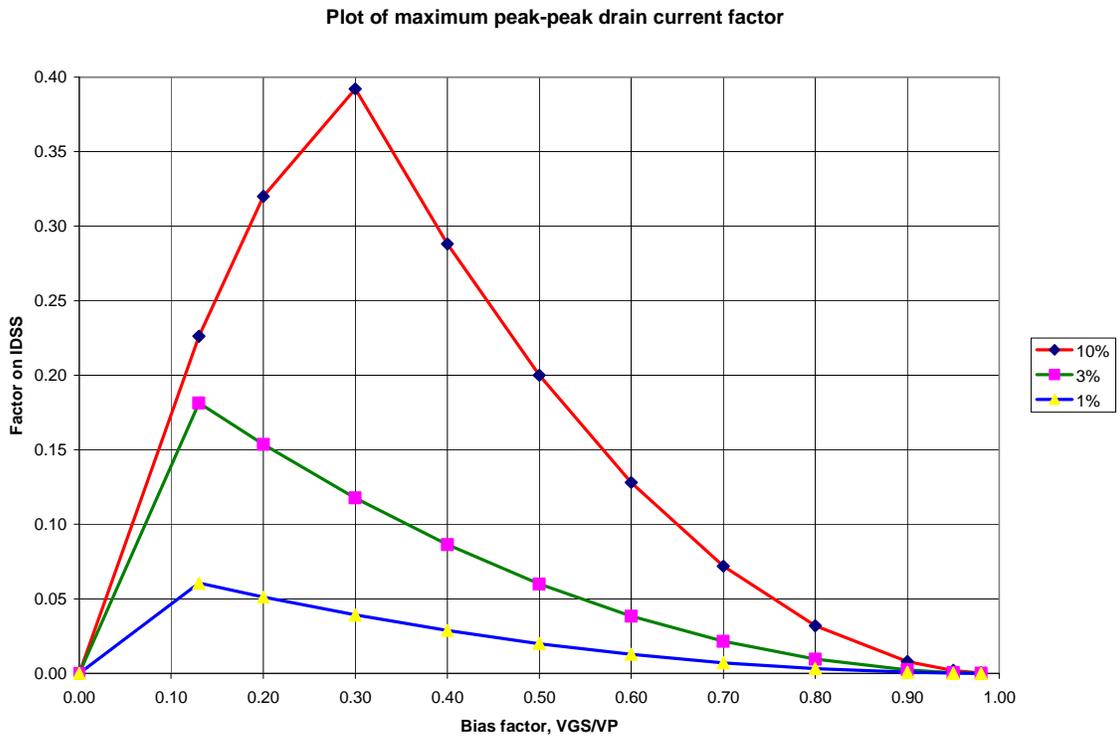


Figure 13: Maximum peak-peak Drain Current Factor on IDSS for Given Distortion

Distortion in JFET Amplifiers

Example design

Where is a good operating point for a JFET that has an I_{DSS} of 10 mA and a V_P of -3 volts if the goal is large output signal swing with low distortion? Answer: Rounded to convenient values, choose $V_{GS} = -0.3$ to -0.9 volts (10% to 30% of -3 volts) or $I_D = 8$ to 5 mA (80% to 50% of 10 mA). Lower distortion at the expense of output amplitude occurs at the higher quiescent drain currents. From Figure 13, the maximum peak-peak drain signal current for low distortion (1%) is around 500 microamperes and around 1.5 mA for the higher distortion of 3%. If the drain resistor were 2K and the load resistance were 1K, then the maximum load signal at 3% distortion would be around 1 volt peak-peak. This example assumes that the drain bias voltage is sufficiently high enough to keep the JFET in the saturated region of operation for any signal in the indicated range.