An Oversampled Digital PWM Linearization Technique for Digital-to-Analog Conversion

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An Oversampled Digital PWM Linearization Technique for Digital-to-Analog Conversion

Jin-Whi Jung and Malcolm J. Hawksford

***Abstract*—An algorithmic-based linearization process for uniformly sampled digital pulsewidth modulation (PWM) is described. It is shown that linearization of the intrinsic distortion resulting in uniformly sampled PWM can be achieved by using a fractional delay digital filter embedded within a noise shaping re-quantizer. A technique termed direct PWM mapping is proposed as a pre-compensation filter scheme for applications in high-resolution digital-to-analog conversion.**

***Index Terms*—Digital-to-analog (D/A) conversion, pulsewidth modulation (PWM), sigma–delta modualtion (SDM).**

I. Introduction

TIME-DISCRETE pulsewidth modulation (PWM) has a natural synergy with digital circuitry used within both digital systems and more general very large-scale integrated (VLSI) devices. Since MASH [6], the amalgamation of low-bit uniformly sampled PWM and noise shaping re-quantization has invited considerable research, not least because it relaxes the problem of quantizer saturation encountered in two-level quantization sigma–delta modulatoion (SDM). However, the intrinsic nonlinearity of uniformly sampled PWM is a well-known problem that can produce significant levels of in-band distortion whereas naturally sampled PWM, as commonly used in analog PWM systems, is linear within the baseband frequency range. Consequently, uniformly sampled PWM is subject to spectral distortion implying the filtered output signal is partially corrupted, see Craven [3], Rowe [11], and Leigh [12] for detailed discussions.

Several research papers that address the subject of linearization in PWM have been reported. Mellor *et al.*, [5] and Leigh [12] introduced a method using time-domain interpolation, while Goldberg [2] and Goldberg and Sandler [4] presented a more refined interpolation technique to approximate uniformly sampled PWM to natural sampling. Hawksford [1] developed a novel uniformly sampled PWM distortion compensation technique for uniformly sampled PWM that was later adapted to embrace multilevel, multiwidth PWM [10]. Craven [3] then proposed a similar compensation technique but where error correction was implemented using negative feedback incorporated within a noise shaping loop.

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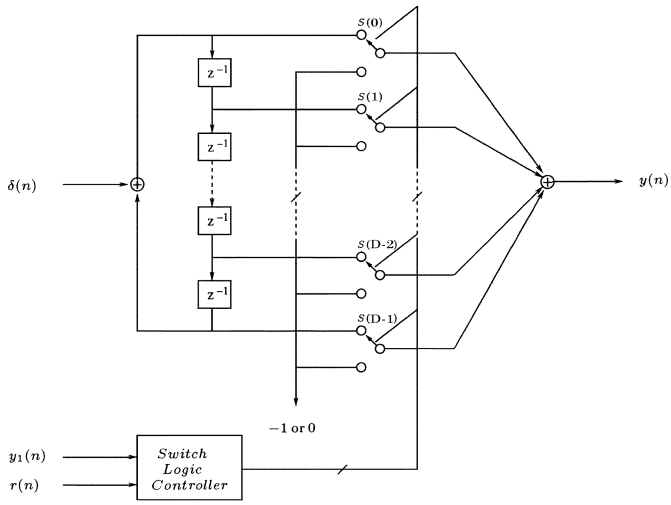

Fig. 1. Implementation of digital PWM in which 2-level quantizers s_i are connected within circular formation and gated by the switch logic controller according to α, where D is the PWM resolution bits, $\delta(n)$ is the unit impulse, $r(n)$ is the PWM reference signal, $y_1(n)$ is the output of the noise shaping re-quantizer, and $y(n)$ PWM output.

This paper presents a fractional sample interpolation scheme to reduce the intrinsic distortion resulting from the uniformly sampled PWM. The technique designated direct PWM mapping (DPM), exploits a Farrow structure fractional delay finite-impulse response (FIR) digital filter employing third-order Lagrange interpolation. The principal feature of the DPM scheme is that the normalized fractional sample grid of the Farrow structure directly generates the digital PWM time base defining the PWM output-wave transitions. It is shown here that a 3-tap Farrow structure FIR filter is sufficient for linearization and as such contributes to the simplicity of the overall PWM system.

II. Digital PWM and Intrinsic Distortion

Fig. 1 shows the proposed digital PWM where the modulating signal α is derived from a logic combination of both the quantized output signal $y_1(n)$ and the PWM reference signal $r(n)$. Let α be scaled to an integer value i so that $i \in (0, D-1)$ where $i \in \mathbb{Z}$ and D is derived from the pulse-repetition period $T_D = DT_s$, i.e., integer multiples D of the sampling period $T_s = 1/f_s$. The signal α addresses a switch state control circuit where s_1 and s_0 denote the on-state and off-state switches, respectively. The PWM time-domain sequence $h(\alpha, n)$ is therefore given as

$$h(\alpha,n) = h(\alpha,n-D) + s_1(0)\cdot\delta(n) + s_1(1)\cdot\delta(n-1) + \cdots + s_1(\alpha-1)\cdot\delta(n-\alpha+1)$$

$$+ s_1(\alpha)\cdot\delta(n-\alpha) + s_0(\alpha+1)\cdot\delta(n-\alpha-1) + \cdots + s_0(D-1)\cdot\delta(n-D+1). \quad (1)$$

Alternatively, in z domain, $h(\alpha, n)$ is expressed as

$$H(\alpha,z) = \frac{1}{1-z^{-D}}\cdot\left(\sum_{i=0}^{\alpha} s_1(i)\cdot z^{-i} + \sum_{i=\alpha+1}^{D-1} s_0(i)\cdot z^{-i}\right). \quad (2)$$

The last term of (2) is required for zero padding in order to represent the logic state 0 within a pulse-repetition period for unipolar leading-edge PWM; also, if s_0 is set to -1 it represents negative magnitude padding in bipolar leading-edge PWM.

Expressions (1) and (2) provide an intuitive understanding of digital PWM.

1) The sampled data z^{-i} is gated by corresponding 2-level quantizers and connected within a circular formation.
2) While the sampled data $z^{-\alpha}$ relates to pulse-position modulation (PPM) where the summation of impulses from 0 to α constitutes a rectangular pulse having pulsewidth α.

In this manner, the denominator $R(z) = 1/(1-z^{-D})$ determines the PWM pulse repetition with D roots.

For the purpose of illustration, if the allocation of α and D are chosen arbitrarily, noting that all the logic states of the switches $s_1(i)$ are asserted 1, then the periodic impulse response sequence will appear as

$$h = \begin{bmatrix} s_1(0) & s_1(1) & \cdots & s_1(\alpha) & 0 & \cdots & 0 \\ s_1(0) & s_1(1) & s_1(2) & \cdots & s_1(\alpha) & \cdots & 0 \\ s_1(0) & \cdots & s_1(\alpha) & 0 & 0 & \cdots & 0 \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ s_1(0) & s_1(\alpha) & 0 & 0 & 0 & \cdots & 0 \end{bmatrix} = \begin{bmatrix} 1 & 1 & \cdots & 1 & 0 & \cdots & 0 \\ 1 & 1 & 1 & \cdots & 1 & \cdots & 0 \\ 1 & \cdots & 1 & 0 & 0 & \cdots & 0 \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ 1 & 1 & 0 & 0 & 0 & \cdots & 0 \end{bmatrix}. \quad (3)$$

Note also that the transfer function of the digital PWM can be expanded in an infinite geometric series

$$H(\alpha,z) = (1+z^{-1}+\cdots+z^{-\alpha}+0+\cdots+0)\cdot(1+z^{-D}+z^{-2D}+\cdots). \quad (4)$$

The pulse-repetition period D has a base of $1-z^{-D}$, hence there exist D frequencies within the Nyquist interval with D roots of unity. In this notation each PWM bit corresponds to the delays at each sampling instant. Defining $\omega_i = (2\pi f_i/f_s) = (2\pi i/D)$, the roots of $H(\alpha,z)$ are obtained by solving $z^D = 1$ for D solutions, that is D roots of unity in the digital PWM system. The zeros of the denominator $R(z)$ that constitute dips in spectral response form D roots of unity on the unit circle, where if D corresponds to the PWM bit resolution, then, generally, $D = 2^M$ where M is even integer.

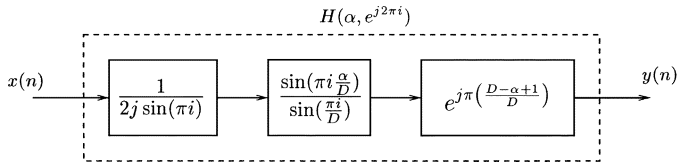

Fig. 2. Uncompensated PWM system represented as a nonlinear magnitude response and a variational delay response, derived from (5).

Hence, from (2), the transfer function $H(\alpha, \exp[j2\pi i])$ may be derived as

$$H(\alpha,e^{j2\pi i}) = \frac{1}{1-e^{-j2\pi i}}\cdot\frac{1-e^{-j2\pi i\frac{\alpha}{D}}}{1-e^{-j\frac{2\pi i}{D}}} = \frac{1}{2j\sin(\pi i)}\cdot\frac{\sin\left(\pi i\frac{\alpha}{D}\right)}{\sin\left(\frac{\pi i}{D}\right)}\cdot e^{j\pi i(\frac{D-\alpha+1}{D})}. \quad (5)$$

The transfer function (5) represents conventional uncompensated digital PWM that is characterized in the frequency domain by a nonlinear magnitude response, see Fig. 2. As such, this process can be compared to a similar result given previously by Hawksford [1], where the linear magnitude component of a PWM pulse is multiplied by a nonlinear transfer function, i.e., $H(\alpha, \exp[j2\pi i]) = \alpha\cdot H(\exp[j2\pi i])$ that results from modulating the pulsewidth, also [10] extended this discussion to include multilevel digital PWM.

For large values of D, the transfer function of $H(\alpha, \exp[j2\pi i])$ in (5) becomes

$$H(\alpha,e^{j2\pi i}) = \frac{1}{2j\sin(\pi i)}\cdot\frac{\sin\left(\pi i\frac{\alpha}{D}\right)}{\frac{\pi i}{D}}\cdot e^{j\pi i(\frac{D-\alpha+1}{D})} \quad (6)$$

where (6) shows that transfer function $H(\alpha, \exp[j2\pi i])$ has an α-dependent nonlinearity of the form $\sin(\alpha x)/x$ that describes deterministically the nonlinear modulation process inherent in uniformly sampled digital PWM. From (6), it follows that for sufficiently small α, the transfer function $H(\alpha, \exp[j2\pi i])$ approximates to

$$H(\alpha,e^{j2\pi i}) = \frac{\alpha}{2j\sin(\pi i)}\cdot e^{j\pi i(\frac{D-\alpha+1}{D})}. \quad (7)$$

The spectral distortion described by (5) can be calculated directly using computer simulation, where over a bandwidth of 192 kHz, Fig. 3 reveals a typical spectrum for uniformly sampled PWM. The intermodulation components that occur at the multiples of sampling frequency of 48 kHz can also be calculated using the mathematical results in [11], they are observed for each harmonic of the pulse-repetition frequency, where their magnitudes become lower and spectra broaden as frequency increases. Also, reflected distortion components can be seen within the baseband close to the fundamental frequency of 750 Hz. Both these classes of distortion are exploited in this study to assess the performance of PWM linearization and are estimated by simulation.

1) *Harmonic distortion:* With an input signal of frequency $f = 6$ kHz sampled initially at 48 kHz and using four times upsampling, PWM for both 6-bit leading-edge sampling Fig. 4(a) and 7-bit double edge sampling Fig. 4(b) are simulated to observe the reflected spectral distortion appearing within baseband. Harmonics $2f$ and $3f$ are the

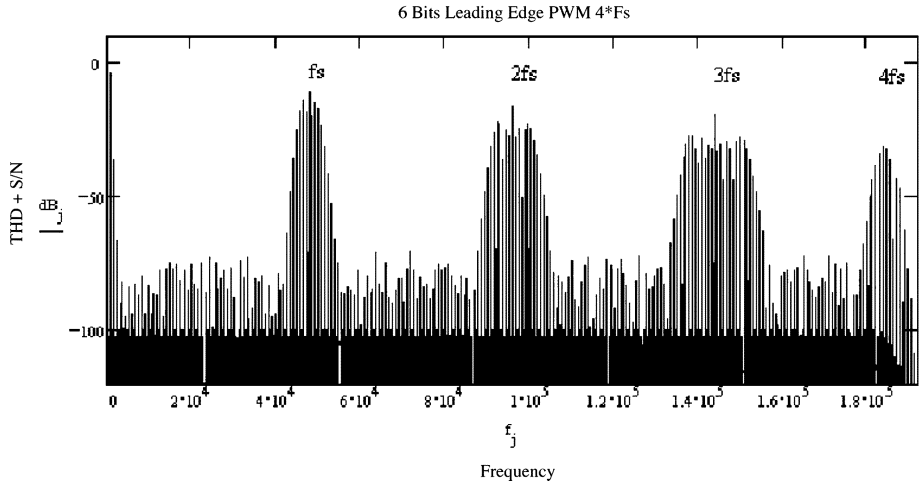

Fig. 3. Typical spectra of uniformly sampled PWM; intermodulation harmonic distortions at each multiples of PWM pulse-repetition frequency 48 kHz and reflected harmonic distortions in baseband, where the input frequency is 750-Hz single tone.

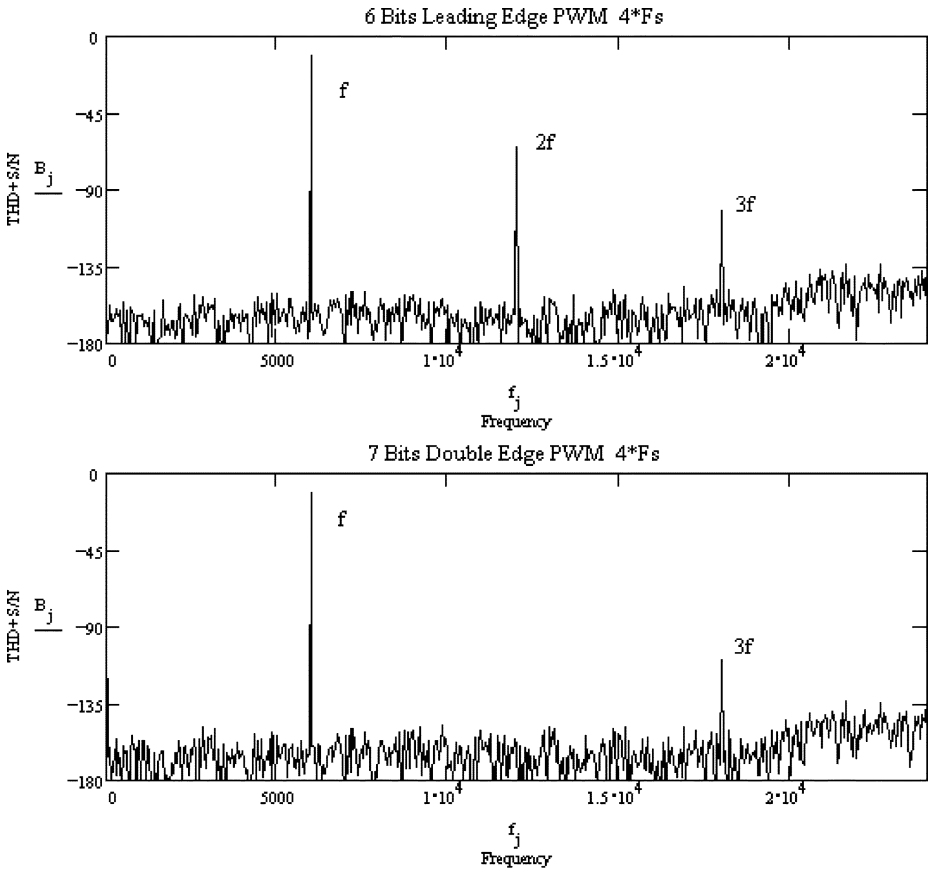

Fig. 4. PWM distortion in audio frequency band. (a) A 6-bit leading-edge sampling. (b) A 7-bit double edge sampling PWM systems at 4 times $f_s = 48$ kHz, input signal is 6 kHz.

reflected distortion components with respect to the 6-kHz input signal. The results confirm that double edge sampling achieves even order harmonic cancellation where for example the component $2f = 12$ kHz is absent, while it remains for leading-edge PWM.

2) *Intermodulation distortion:* The intermodulation results are shown in Fig. 5 where three superimposed input frequencies $f_1 = 0.75$ kHz, $f_2 = 6$ kHz, and $f_3 = 9$ kHz drive a 6-bit $4f_s$ PWM and hence the sampling rate is 192 kHz. The observed intermodulation distortion components are located both sides of the fundamental frequencies f_1, f_2, and f_3 and their multiples.

III. DPM

A. Windowing and Transfer Functions

In the following discussion, only leading-edge sampling digital PWM is presented although DPM can also be implemented for use with double-edge sampling PWM.

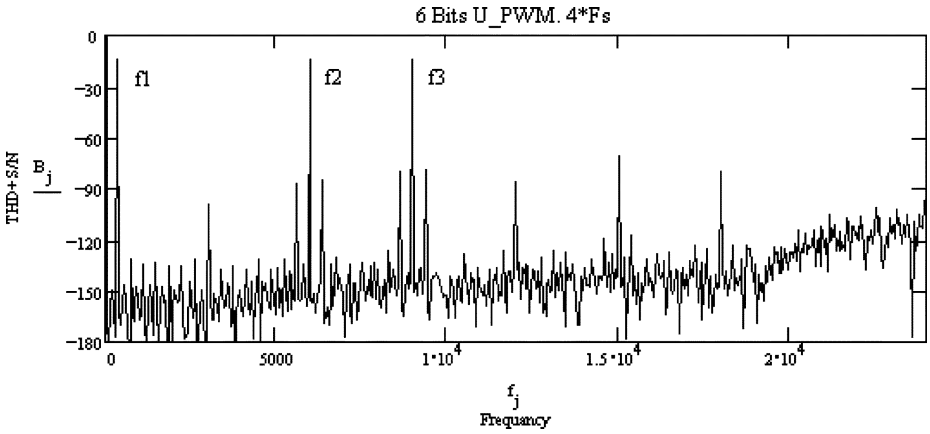

Fig. 5. Intermodulation distortion simulation results, the input frequencies are $f_1 = 0.75$ kHz, $f_2 = 6$ kHz, and $f_3 = 9$ kHz.

DPM is a dynamic switch operation map applied to digital PWM that is composed of a circular structure of 2-level quantizers whose delay length varies with α where, $0 \leq \alpha < D$, consequently, D is the pulse-repetition period. Let a time sequence $\{\cdots, k = D, k+1 = 2D, k+2 = 3D, \cdots\}$ be defined to determine each PWM pulse edge sampling instant where each has the sampled grid $i = 0, 1, 2, \cdots, D-1$ used to upsample in between two consecutive sequences. For notational convenience, in this section, we normalize this time sequence so as D is set at 1, and hence, α is correspondingly fractional.

Based upon this iterative definition, (1) can be rewritten as a difference equation

$$y(\alpha, k+1) = y(\alpha, k) + \sum_{i=0}^{\alpha} \frac{\sin(\pi(k-i))}{\pi(k-i)} + \sum_{i=\alpha+1}^{D-1} \Xi(i) \quad (8)$$

where $\Xi(i) = 0$ or $\Xi(i) = -1$ by the PWM definition in (2). Further, let the impulse function in (8) be defined as

$$h_{\text{pwm}}(\alpha, k) = \sum_{i=0}^{\alpha} \frac{\sin(\pi(k-i))}{\pi(k-i)}. \quad (9)$$

The last term $\sin(\pi(k-\alpha))/\pi(k-\alpha)$ represents the transition edge, where the summation from 0 to α for the pulses defines the method of PWM.

In order to apply a windowing function to (9) by taking $N+1$ consecutive samples in k iterations, samples are denoted as integer $j \in (0, N)$ where they are composed of an odd-N Lagrange interpolation FIR filter on an iterative scale of k. Hence, the property can be applied that impulse responses h_{pwm} for $N - j$ are the same as those for j but placed in reverse order, that is,

$$h_{\text{pwm}}(\alpha, j) = \sum_{i=0}^{\alpha} \frac{\sin(\pi(j-i))}{\pi(j-i)} = (-1)^{N-j} \sum_{i=0}^{\alpha} \frac{\sin(\pi i)}{\pi(j-i)}. \quad (10)$$

In our example where $N = 3$, the sign of $h_{\text{pwm}}(\alpha, j)$ in (10) alternates as $\{-1, 1, -1\}$. Therefore, the PWM pulses that determine the transition edges should shift one repetition period to the right in order to prevent the sign of impulses changing during leading-edge sampling (see the dotted line in Fig. 6).

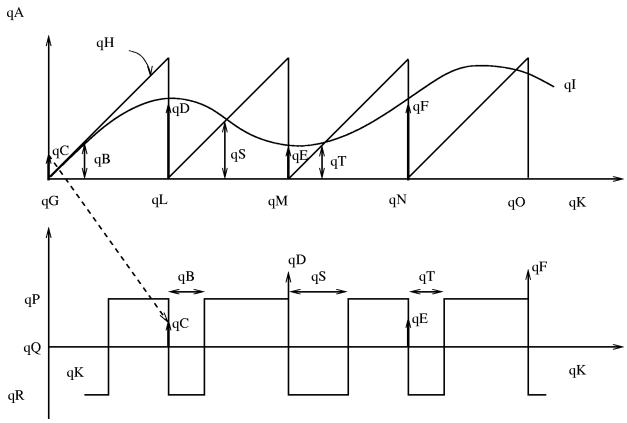

Fig. 6. Mapping is accomplished by an Lagrangian interpolation where the magnitude of modulating signal data α in each frames are linearly converted into time-domain data in leading-edge modulation.

Note that $h(\alpha, j)$ corresponds to the impulse response of DPM defined by the window and the Lagrangian interpolation FIR filter coefficient for Nth order polynomials, which has a classic form

$$h(\alpha, j) = \prod_{k=0,\ k \neq j}^{N} \frac{\alpha - k}{j - k}, \qquad \text{for } j \in \{0, 1, 2, \cdots, N\} \quad (11)$$

where $h(\alpha, j)$ has the Kronecker Delta function property

$$h(\alpha, j) = \begin{cases} 1, & \text{if } j = k \\ 0, & \text{if } j \neq k. \end{cases} \quad (12)$$

Once the Lagrange coefficient polynomial (11) is derived, it is unnecessary to calculate equations simultaneously as the new upsampled data fall on the grid obtained from the summation of products of each coefficient and the output values of the re-quantizer. In order to derive an explicit transfer function expression, take a binomial coefficient for (11) so that it determines the number of ways of choosing sampling time.

For a generic Lagrangian interpolation of (11), one should refer to [7] where several results for the binomial coefficients are introduced. When N is odd, it follows

$$h(\alpha,j)=(-1)^{N-j}\binom{\alpha}{j}\binom{\alpha-j-1}{N-j}$$
$$=(-1)^{N-j}\binom{\alpha}{L}\binom{N}{j}\frac{L}{\alpha-j} \tag{13}$$

since the following relations are satisfied for $N, j \in \mathbb{Z}$ where

$$\binom{\alpha-j-1}{N-j}=\binom{\alpha-j}{N-j}\frac{1}{\alpha-j} \tag{14}$$

and

$$\binom{\alpha}{j}\binom{\alpha-j}{N-j}=\binom{\alpha}{N}\binom{N}{j}. \tag{15}$$

During the upsampling operation that generates the digital PWM clocks, the *sinc* function under the window of length $L=N+1$ for the DPM Lagrangian FIR filter is

$$h(\alpha,j)=(-1)^{N-j}\sum_{i=0}^{\alpha}\left\{\frac{\sin(\pi i)}{\pi(j-i)}\binom{\alpha}{L}\binom{N}{j}\frac{\pi L}{\sin(\pi i)}\right\} \tag{16}$$

in which the two terms, $W_b(j)$ and $C_b(\alpha)$ are defined as

$$W_b(j)=\binom{N}{j} \tag{17}$$

$$C_b(\alpha)=\sum_{i=0}^{\alpha}\left\{\binom{\alpha}{L}\frac{\pi L}{\sin(\pi i)}\right\} \tag{18}$$

is the scaling coefficient and forms an intrinsic equalization function with regard to the digital PWM, which eliminates the intrinsic spectral distortions. This equalization process can be viewed as a pre-processing stage formed by a FIR digital filter whose impulse response compensates for the frequency response of h_{ppm}. Fig. 6(b) depicts frequency-domain magnitude weighting, which can be interpreted as a pre-compensation filter to the digital PWM.

B. Mapping and Implementation

The implementation of (16) for DPM is accomplished using a third-order Lagrangian interpolator. A limit needs to be imposed on the interpolation filter whose normalized gain must not exceed 1 to prevent additional distortion by over modulation resulting from an excessive modulation index. The Farrow structure fractional delay FIR filter (see [8] and [14] for details) is selected for the Lagrangian interpolation filters for DPM in which the coefficients are dynamically adjusted by the reference signal $r(i)$ stored in ROM. Fig. 7 shows the direct mapping principle in which the PWM reference signal $r(i)$ consists of unit-tread staircase $y_1(i)$ is the re-quantized signal at the upsampling instants of the Lagrangian Farrow structure interpolator for which there must be only a single solution to detect the position of the sampling instant for α.

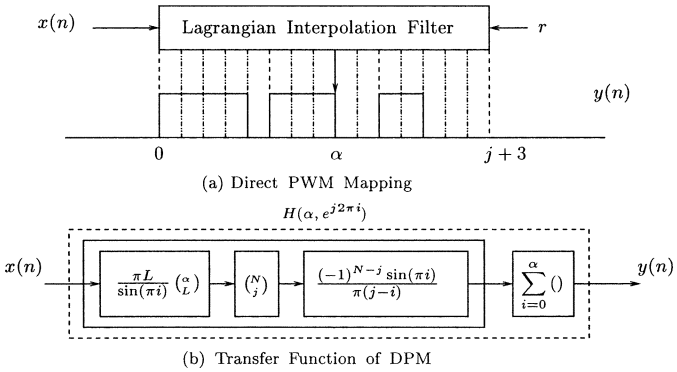

Fig. 7. Direct PWM mapping system represented as a pre-compensation filter and PWM. (a) The Lagrangian interpolation FIR filter consists of the PWM frame where each PPM signal is summed over α. (b) Depicts the transfer function diagram derived from (16).

TABLE I
SAMPLED EXAMPLE OF PWM REFERENCE SIGNAL

t_k	t_{k+1}	t_{k+2}	t_{k+3}
0.4627151	0.6008112	0.7565712	0.8775633

TABLE II
4-BIT DIRECT PWM MAP EXAMPLE BY TABLE I

PWM bit	Interpolation	N.S output	PWM output
16	0.7565712	0.6875	1
15	0.7473108	0.6875	1
14	0.7379273	0.8125	1
13	0.7284337	0.75	1
12	0.7188426	0.8125	1
11	0.7091669	0.625	1
10	0.6994194	0.625	1
9	0.6896129	0.8125	-1, 0
8	0.6797602	0.6875	-1, 0
7	0.6698741	0.5625	-1, 0
6	0.6599674	0.625	-1, 0
5	0.6500529	0.6875	-1, 0
4	0.6401433	0.6875	-1, 0
3	0.6302516	0.6875	-1, 0
2	0.6203905	0.5625	-1, 0
1	0.6105727	0.625	-1, 0

For example, the points at each sample periods before interpolation are shown in Table I, which is taken from a simulation result of the schematic in Fig. 8. α is uniformly sampled and each value provides information on the pulse transition instant of the PWM output signal after one sample delay of the pulse-repetition period. A leading-edge example is illustrated in Fig. 7 where the rising pulse sampling instant is passed to the DPM output signal. Both Tables I and II present examples of 4-bit DPM where t_k, t_{k+1}, t_{k+2}, and t_{k+3} are internal state values of 3-tapped delay line for the Lagrangian Farrow structure FIR filter. In this sequence, the interpolated samples correspond to each digitized 2^4 PWM values. Looking at the period between t_{k+1} and t_{k+2}, the upsampled 16 values can be obtained which are displayed in the Interpolation column in Table II.

The complete digital-to-analog (D/A) conversion system for an audio application is shown in Fig. 8. The pre-compensation FIR filter has a 3-tap delay line and is synchronously controlled

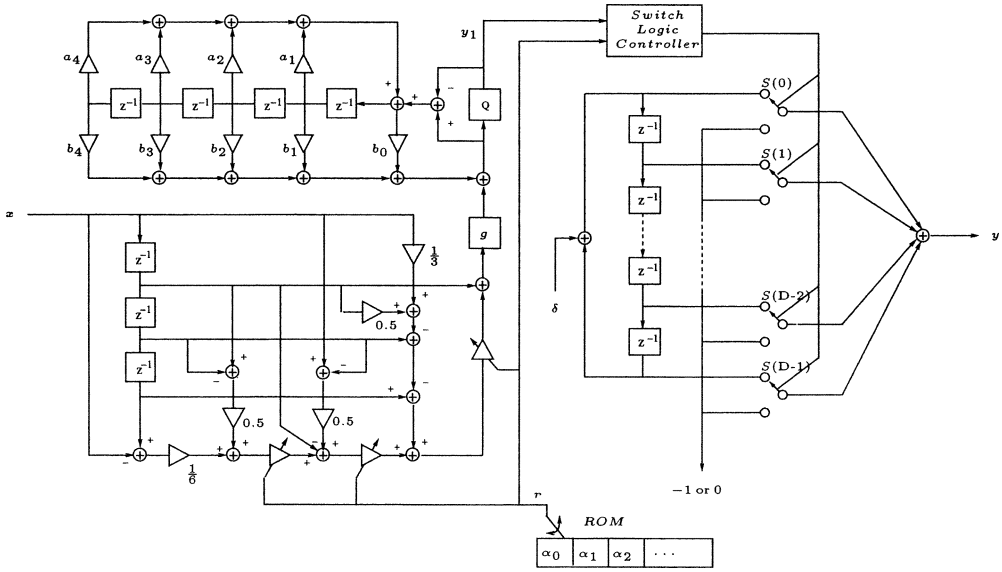

Fig. 8. Direct PWM mapping schematic for $4 \cdot f_s$ input 4-bit PWM D/A converter example.

by r which is stored in the ROM. The output of the Lagrange interpolation filter is scaled by a gain g in order to match the input range of the noise shaping re-quantizer and its output y_1 drives the digital PWM. This re-quantization from the PCM signal, using the *floor* rounding function that returns the greatest integer from the quantizer, has a D-bit range and is given by

$$Q(x) = \frac{\text{floor}(D \cdot x + 0.5)}{D}. \tag{19}$$

The coefficients a_n and b_n in the noise-shaping re-quantization block are set according to the noise shaping system design requirements; a_n should have negative values while b_n positive, etc. Due to the fourth-order noise shaping loop used in this example, which goes unstable unless the overall loop gain is kept to less than 0.5, the coefficient calculation of the noise shaper must be carefully chosen. Although a fourth-order noise shaping re-quantizer is used here, the DPM can take noise-shaping schemes of any type and order. The main idea of using noise-shaping re-quantization is to provide compression of the input PCM signal for the digital PWM. However, the performance of the noise shaping re-quantization has a direct effect on the output signal-to-noise (S/N) ratio.

TABLE III
COMPARISON OF ERROR CORRECTION METHODS OF FOUR PWM DACS

	Linearization Methods	Implementation Methods
PA	Interpolation to approximate analogue PWM - Time Domain	Interpolation and digital signal processing for Newton-Rapson algorithm
MFIR	Frequency moment matching - Frequency Domain	5 tap FIR filter in form of Toeplitz matrix
PNS	Frequency moment matching -Frequency Domain	3 tap FIR filter(ROM) in feedback loop and look-ahead scheme
DPM	Interpolation and windowing -Time and Frequency both	Farrow structure 3 tap FIR filter and digital PWM mapping

TABLE IV
COMPARISON OF SPECIFICATIONS OF FOUR PWM DACS

	PA	MFIR	PNS	DPM	SDM
Sampling Frequency	48kHz	48kHz	48kHz	48kHz	48kHz
PWM Bits	8	10	4	6	1
Oversampling	$8{\cdot}f_s$	$4{\cdot}f_s$	$64{\cdot}f_s$	$4{\cdot}f_s$	$256{\cdot}f_s$
Clock Rate (MHz)	98.304	196.608	49.152	12.288	12.288
THD+S/N	-125dB	-110dB	-160dB	-120dB	-112dB
NS order	5th	(2+2)th	5th	4th	2nd

C. Features and Comparison

The DPM operation can be summarized as D-bit PWM whose 2^D times upsampled values are located within the pulse-repetition period after filtering the input signal by the 3-tap Farrow structure FIR filter. The output of the Farrow structure FIR filter is fed to a noise shaping re-quantizer in order for the input signal to be compressed to D-bit PWM. DPM may be compared with earlier PWM linearization techniques that have been developed previously using time and frequency-domain methods. Time-domain PWM linearization methods have appeared in several studies [2], [4], [5], [12]. These papers demonstrated the typical error found in uniformly sampled PWM and introduced an improved sampling process for digital PWM power amplifiers [5], [12]; to conclude, possible remedies were suggested using upsampling introduced between two consecutive samples to locate the digital PWM edges. However, for finer accuracy, [2], [4] raised the concept of using the polynomial approximation method. On the other hand, the frequency-domain methods are studied in [1], [3], [10] and are based on the concept of moment matching.

In Tables III and IV, outline principles and example results are summarized that correspond to the respective papers, [1]–[3]. However, it should be noted that the clock rates given in Table IV are not related directly to the error correction method and corresponding performance but to the implementation differences. For brevity, the following terms are used; moment matching FIR

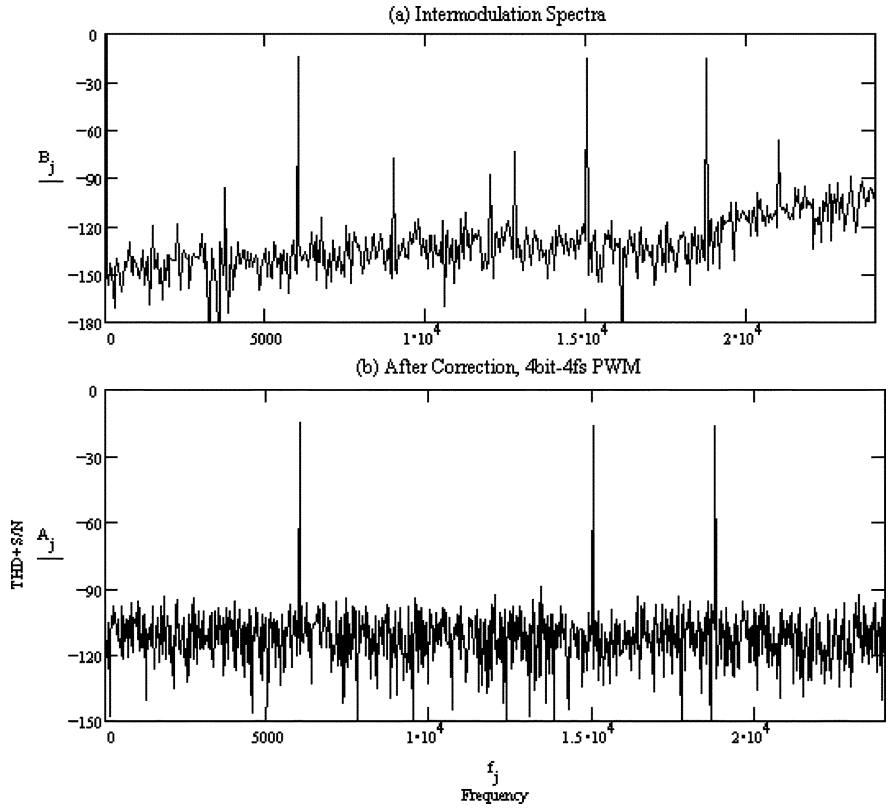

Fig. 9. Simulation results of 4-bit $4f_s$ PWM system (a) uncorrected (b) after correction.

filtering (MFIR) for the paper [1], polynomial approximation (PA) [2], procrastinate noise shaping (PNS) [3], and SDM.

The principal features of the DPM method are as follows.

1) In the time domain, DPM has better computational efficiency since it does not require iterative calculation steps for cross points or roots finding of two polynomials which is used in PA method.
2) In the frequency domain, its implementation is simpler because a 1-tap or 3-tap FIR filter is sufficient for the cascaded pre-compensation FIR filter, compared with MFIR and PNS methods.
3) Unlike SDM adopting 2-level quantization, PWM-based D/A converters (DACs) are known to have a distinctive feature in that the quantization overload problem can be relaxed due to higher bit quantization, [3], this is important in real-time applications although recent developments in Trellis SDM should be observed [17], [18].

The concept behind DPM can possibly be adapted to all forms of PWM's. For example, for double-edge modulation, it should use an even-order (2∼4 tap) Farrow structure Lagrangian interpolation FIR filter. A series of simulations were performed to test the error correction performance of DPM. Taking into account typical DACs; input signals are upsampled by 4 to 8 times.

IV. Simulation Results

In initial investigations, PWM with 4∼8 bit resolution were tested using the processes shown in Fig. 8. Fig. 9(a) shows simulation result of 4-bit, $4f_s$ PWM system with a four times oversampled input signal, where $f_s = 48$ kHz. This uncorrected PWM has an overall system clock rate 3.072 MHz, which is significantly lower than that of the SDM in Table IV. To observe the harmonic and intermodulation distortion in the base-band three superimposed input signals of 6, 15, and 18.75 kHz were used. After DPM operation, Fig. 9(b) reveals that signal purity is preserved more accurately. Following a series of investigations, it was concluded that 3.072 MHz is the minimum system clock frequency required to facilitate appropriate correction for the system; 4-bit PWM fed by $4f_s$ pre-oversampled input signal where $f_s = 48$ kHz.

Next, Fig. 10 presents results where the overall system bit rates are increased to 6.144 and 12.288 MHz, respectively, as the PWM bit resolution is increased from 4 to 5 and 6 bits. With the same superimposed input signal as the earlier example, the PWM intrinsic error is corrected more completely. In Fig. 10 (a), the residual noise and distortion is marked around -120 dB, hence this fact leads us to conclude that the DPM operated at 5-bit $4f_s$ can satisfy the required S/N ratio for high-quality audio applications. The 6-bit $4f_s$ DPM DAC shown in the subfigure (b) has the same system clock rate 12.288 MHz as the commercialized SDM DAC, which is the system proposed in this paper.

Finally, broad-band spectra are considered. Fig. 11 shows two PWM modes 6-bit $4f_s$ and 8-bit $4f_s$, where $f_s = 48$ kHz. The shaped quantization noise and distortion in the high frequency region are chosen so as not to be emphasized significantly where even the highest noise level is lowered to around -100 dB, see the subfigure (b). This is due to one of the distinctive features of the SDM+PWM structure compared to SDM only and can be a desirable characteristic for high resolution DAC applications.

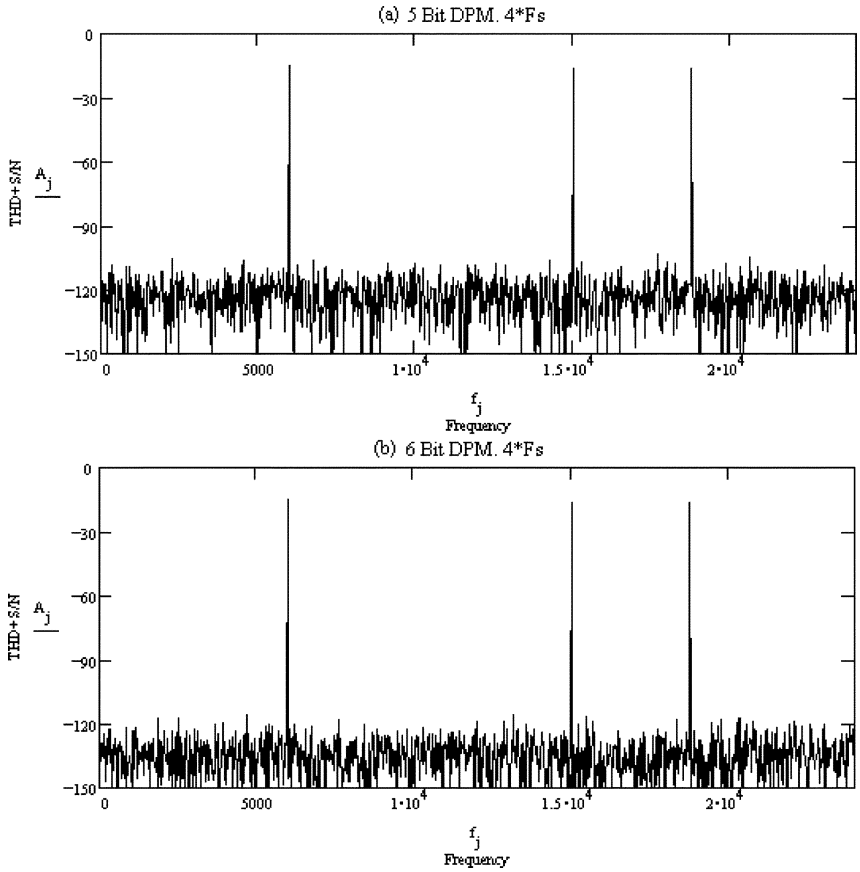

Fig. 10. Simulation results of (a) 5-bit $4f_s$ and (b) 6-bit $4f_s$ PWM systems after error correction by the DPM.

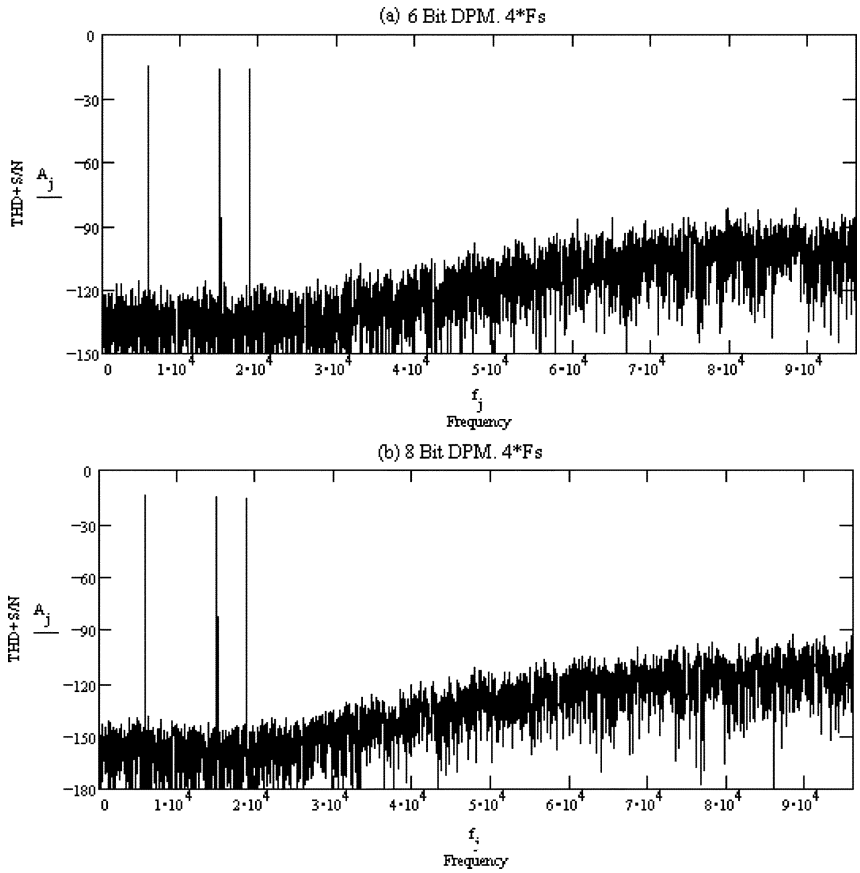

Fig. 11. Simulation results of broad-band spectra of (a) 6-bit $4f_s$ and (b) 8-bit $4f_s$ PWM systems after error correction by the DPM.

V. Summary

A novel error correction scheme for digital PWM has been investigated for use in high-resolution D/A conversion. The main discussion focused on the intrinsic error cancellation achieved using a window function with Lagrangian interpolation in a third-order Farrow structure fractional FIR filter synchronously combined with a digital PWM configured in circular formation. This method is shown to offer advantages against other previously proposed PWM linearization methods.

Although performance estimates are derived from a series of computer simulations, it is shown that relatively high-bit resolution digital PWM with a proper pre-compensation algorithm can outperform SDM; assuming similar system operating environments. Higher resolution D/A conversion can be achieved due not only to the relaxation of the 2-level quantization overload problem but also the significant reduction of noise and distortion generation in high frequency region. In addition, no high-order upsampling digital filter (typically 128 to 256 times) is required compared to SDM, since the third-order Farrow structure fractional FIR filter performs both pre-compensation and upsampling functions in one structure.

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