



### P-Channel JFETs

**J270****J271****SST270****SST271**

#### PRODUCT SUMMARY

Part Number	V <sub>GS(off)</sub> (V)	V <sub>(BR)GSS</sub> Min (V)	g <sub>fs</sub> Min (mS)	I <sub>DSS</sub> Min (mA)
J/SST270	0.5 to 2.0	30	6	–2
J/SST271	1.5 to 4.5	30	8	–6

#### FEATURES

- Low Cutoff Voltage: J270 <2 V
- High Input Impedance
- Very Low Noise
- High Gain

#### BENEFITS

- Full Performance from Low-Voltage Power Supply: Down to 2 V
- Low Signal Loss/System Error
- High System Sensitivity
- High-Quality, Low-Level Signal Amplification

#### APPLICATIONS

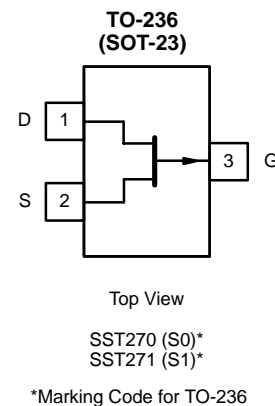
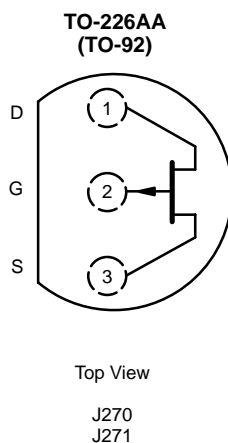
- High-Gain, Low-Noise Amplifiers
- Low-Current, Low-Voltage Battery Amplifiers
- Ultrahigh Input Impedance Pre-Amplifiers
- High-Side Switching

#### DESCRIPTION

The J/SST270 series consists of all-purpose amplifiers for designs requiring p-channel operation.

The TO-226AA (TO-92) plastic package provides a low-cost option, while the TO-236 (SOT-23) package

provides surface-mount capability. Both the J and SST series are available in tape-and-reel for automated assembly (see Packaging Information).



#### ABSOLUTE MAXIMUM RATINGS

Gate-Drain Voltage ..... 30 V  
Gate-Source Voltage ..... 30 V  
Gate Current ..... –50 mA  
Storage Temperature ..... –55 to 150°C  
Operating Junction Temperature ..... –55 to 150°C

Lead Temperature (<sup>1</sup>/<sub>16</sub>" from case for 10 sec.) ..... 300°C  
Power Dissipation<sup>a</sup> ..... 350 mW

#### Notes

a. Derate 2.8 mW/°C above 25°C

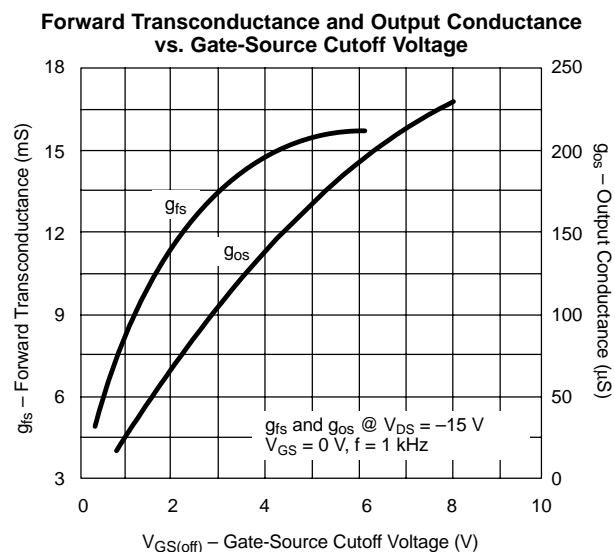
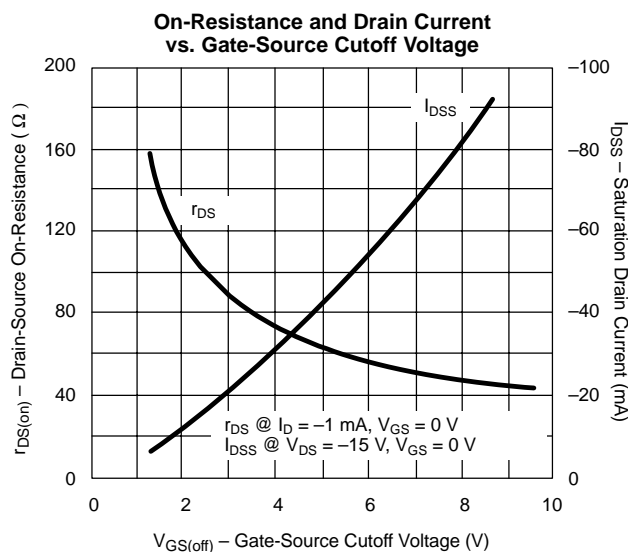
**SPECIFICATIONS ( $T_A = 25^\circ\text{C}$  UNLESS OTHERWISE NOTED)**

Parameter	Symbol	Test Conditions	Typ <sup>a</sup>	Limits				Unit
				J/SST270		J/SST271		
				Min	Max	Min	Max	
Static								
Gate-Source Breakdown Voltage	V <sub>(BR)GSS</sub>	I <sub>G</sub> = 1 μA , V <sub>DS</sub> = 0 V	45	30		30		V
Gate-Source Cutoff Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = −15 V, I <sub>D</sub> = −1 nA		0.5	2.0	1.5	4.5	
Saturation Drain Current <sup>b</sup>	I <sub>DSS</sub>	V <sub>DS</sub> = −15 V, V <sub>GS</sub> = 0 V		−2	−15	−6	−50	mA
Gate Reverse Current	I <sub>GSS</sub>	V <sub>GS</sub> = 20 V, V <sub>DS</sub> = 0 V	10		200		200	pA
		T <sub>A</sub> = 125°C	5					nA
Gate Operating Current	I <sub>G</sub>	V <sub>DG</sub> = −15 V, I <sub>D</sub> = −1 mA	10					pA
Drain Cutoff Current	I <sub>D(off)</sub>	V <sub>DS</sub> = −15 V, V <sub>GS</sub> = 10 V	−10					
Gate-Source Forward Voltage	V <sub>GS(F)</sub>	I <sub>G</sub> = −1 mA , V <sub>DS</sub> = 0 V	−0.7					V
Dynamic								
Common-Source Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> = −15 V, V <sub>GS</sub> = 0 V f = 1 kHz		6	15	8	18	mS
Common-Source Output Conductance	g <sub>os</sub>				200		500	μS
Common-Source Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = −15 V, V <sub>GS</sub> = 0 V f = 1 MHz	20					pF
Common-Source Reverse Transfer Capacitance	C <sub>rss</sub>		4					
Equivalent Input Noise Voltage	$\bar{e}_n$	V <sub>DG</sub> = −10 V, V <sub>GS</sub> = 0 V f = 1 kHz	20					nV/ √Hz

## Notes

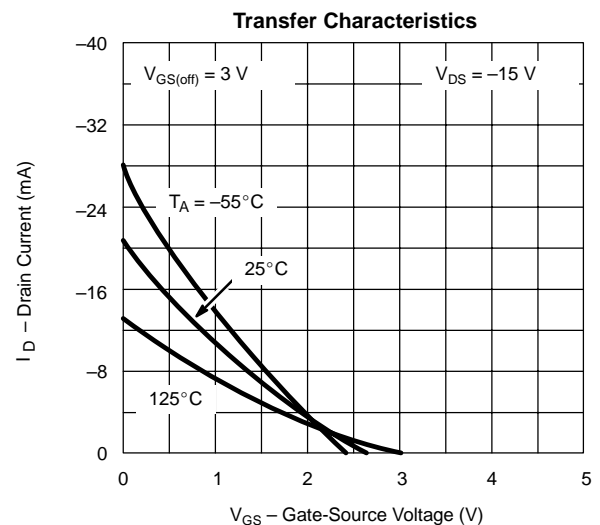
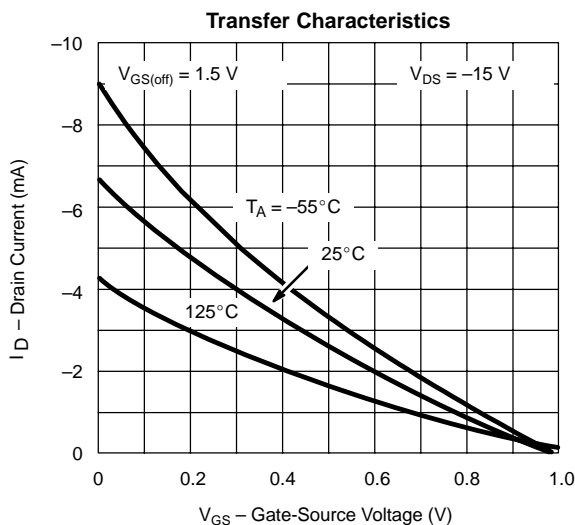
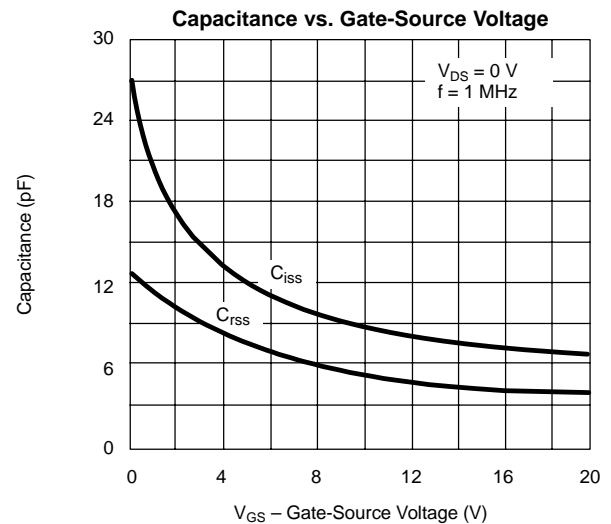
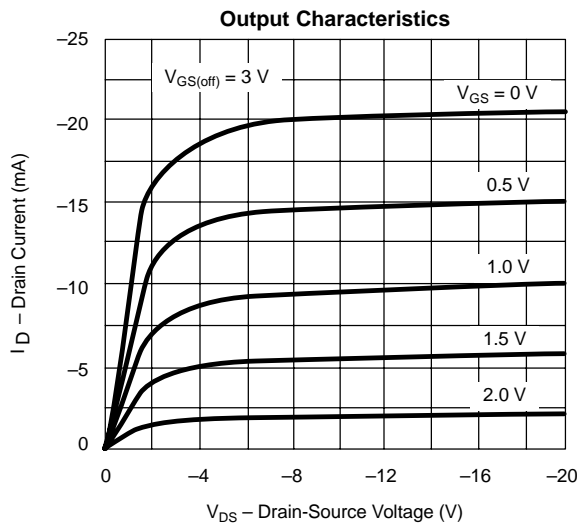
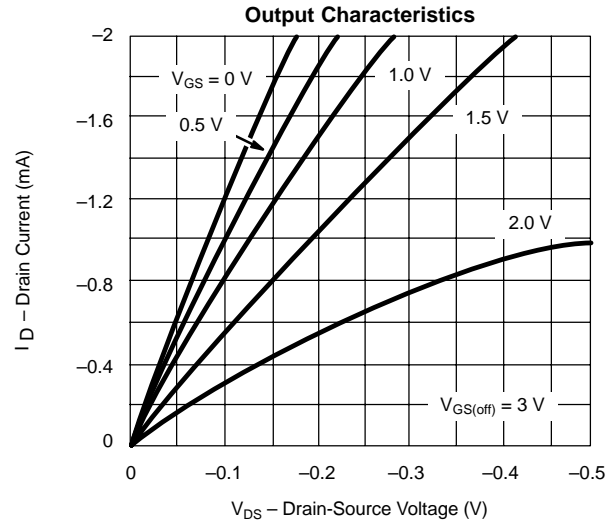
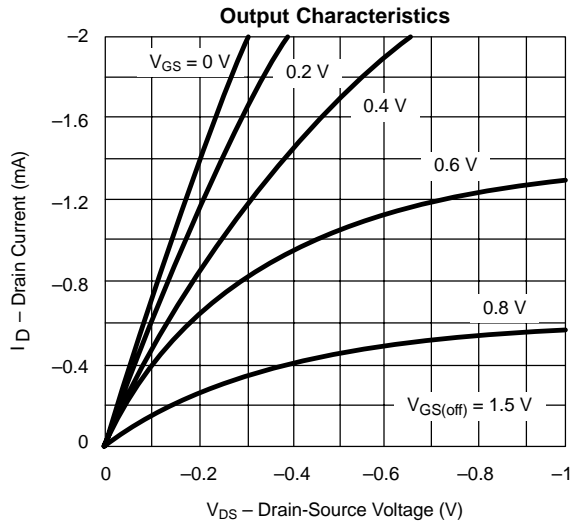
- a. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.  
b. Pulse test:  $PW \leq 300\ \mu\text{s}$  duty cycle  $\leq 3\%$ .

PSCIA

**TYPICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$  UNLESS OTHERWISE NOTED)**



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