

Applications like electronic loads, linear regulators or Class A amplifiers operate in the linear region of the Power MOSFET, which requires high power dissipation capability and extended Forward Bias Safe Operating Area (FBSOA) characteristics. Such mode of operation differs from the usual way of using Power MOSFET, in which it functions like an “on-off switch” in switched-mode applications. In linear mode, the Power MOSFET is subjected to high thermal stress due to the simultaneous occurrence of high drain voltage and current resulting in high power dissipation. When the thermo-electrical stress exceeds some critical limit, thermal hot spots occur in the silicon causing the device to fail [1].

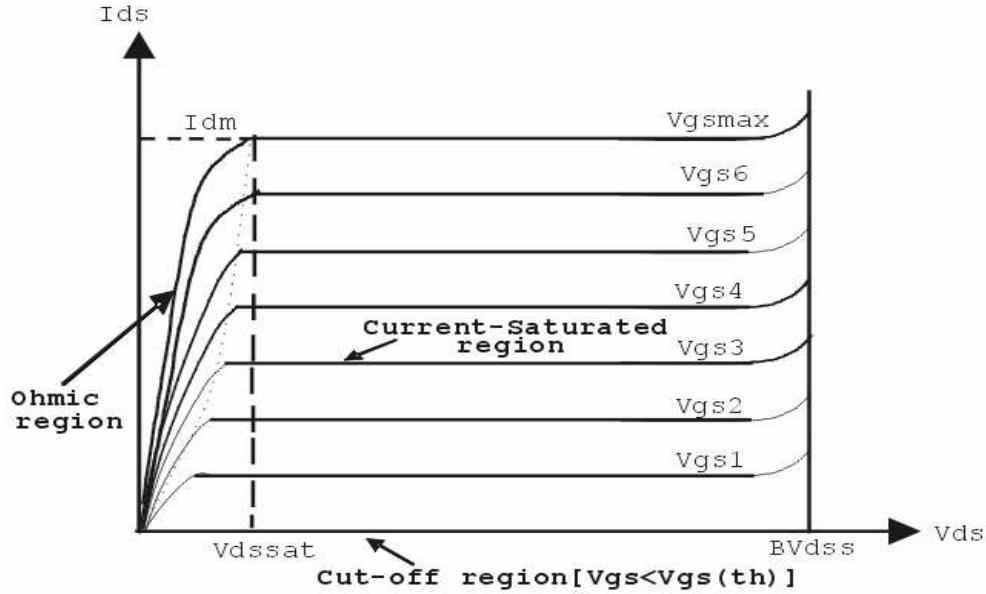


Figure 1: The Output Characteristics of an N-Channel Power MOSFET

Figure 1 shows a typical output characteristic of an N-Channel Power MOSFET in which the different modes of operation are delineated. In the Cut-off region, the gate-source voltage (V_{gs}) is less than the gate-threshold voltage ($V_{gs(th)}$) and the device is an open-circuit or off. In the Ohmic region, the device acts as a resistor with almost a constant on-resistance $R_{DS(on)}$ and is equal to V_{ds}/I_{ds} . In the linear-mode of operation, the device operates in the ‘Current-Saturated’ region where the drain current (I_{ds}) is a function of the gate-source voltage (V_{gs}) and defined by:

$$I_{ds} = K \bullet (V_{gs} - V_{gs(th)})^2 = g_{fs} \bullet (V_{gs} - V_{gs(th)}) \quad \text{Equation (1)}$$

where K is a parameter depending on the temperature and device geometry and g_{fs} is the current gain or transconductance. When the drain voltage (V_{ds}) is increased, the positive drain potential opposes the gate voltage bias and reduces the surface potential in the channel. The channel inversion layer charge decreases with increasing V_{ds} and ultimately, it becomes zero when the drain voltage equals to $(V_{gs} - V_{gs(th)})$. This point is called the “channel pinch-off point” where the drain current becomes saturated [2].

The FBSOA is a datasheet figure of merit that defines the maximum allowed operating points. Figure 2 shows a typical FBSOA characteristic for an N-Channel Power MOSFET. It is bounded by the maximum drain-to-source voltage V_{DSS} , maximum conduction current I_{DM} and constant power dissipation lines for various pulse durations. In this figure, the set of the curves shows a DC line and four single pulse operating lines, 10ms, 1ms, 100 μ s and 25 μ s. The top of each line is truncated to limit the maximum drain current and is bounded by a positive slope line defined by the $R_{ds(on)}$ of the device. The right hand side of each line is terminated at the rated drain-to-source voltage limit (V_{dss}). Each line has a negative slope and is determined by the maximum allowed power dissipation of the device P_d :

$$P_d = [T_{J(max)} - T_C] / Z_{thJC} = V_{DS} I_D \quad \text{Equation (2)}$$

where Z_{thJC} is the junction-to-case transient thermal impedance and $T_{J(max)}$ is the maximum allowed junction temperature of the MOSFET.

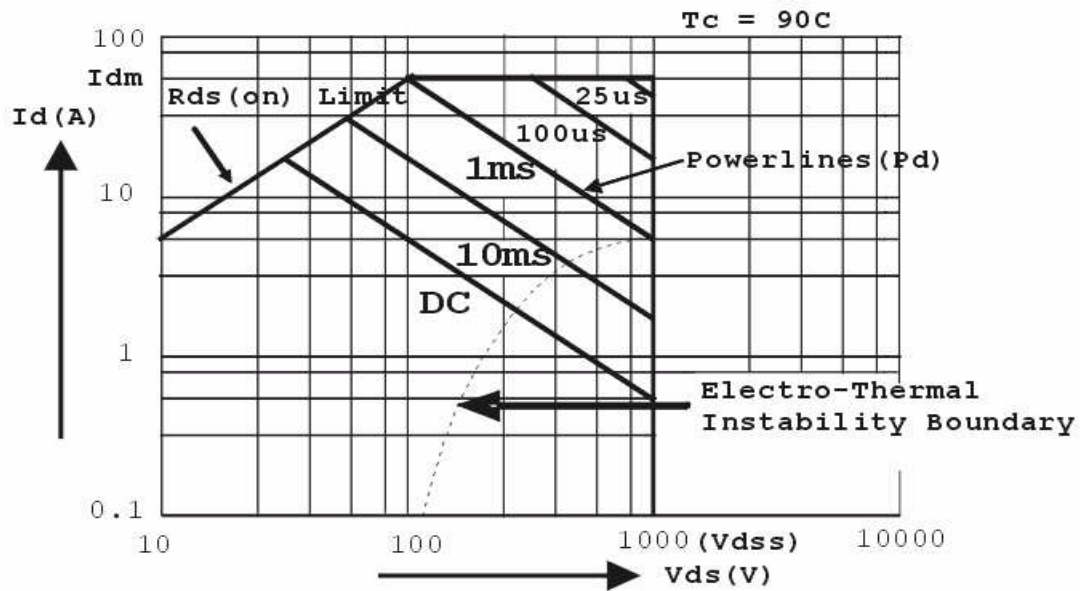


Figure 2: Typical FBSOA graph for an N-Channel Power MOSFET

These theoretical constant power curves are derived from calculation with assumption of essentially uniform junction temperature across the Power MOSFET die. This assumption is not always valid, especially for a large die MOSFETs. Firstly, the edge of a MOSFET die soldered to the mounting tab of a power package has generally lower temperature compared to the center of the die, the result of lateral heat flow. Secondly, material imperfections (die attach voids, thermal grease cavities, etc.) may cause local decrease of thermal conductivity, i.e. increase of local temperature. Thirdly, fluctuations in dopant concentrations and gate oxide thickness and fixed charge will cause fluctuations of local threshold voltage and the current gain (g_{fs}) of MOSFET cells, which will also affect local temperature of the die. Die temperature variations are mostly

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harmless in case of switched mode operation; however, these can trigger catastrophic failure in linear mode operation with pulse duration longer than time required for a heat transfer from the junction to the heat sink. Modern Power MOSFETs optimized for a switch-mode applications were found to have limited capability to operate in the right-side bottom corner of the FBSOA graph, the area to the right of the Electro-Thermal Instability boundary in Figure 2.

Electro-Thermal Instability (ETI) can be understood as a result of positive feedback mechanism on the surface of the Power MOSFET forced into linear mode of operation:

- There is a local increase of junction temperature;
- This causes local decrease of $V_{gs(th)}$ (MOSFET threshold voltage has negative temperature coefficient);
- This causes increase of local current density, $J_{ds} \sim (V_{gs} - V_{gs(th)})^2$;
- Increase of local current density causes increase of local power dissipation and further increase of local temperature.

Depending on the duration of the power pulse, heat transfer conditions and features of the design of MOSFET cells, the ETI may cause a concentration of all the MOSFET current into current filament and formation of a “hot spot”. This normally causes MOSFET cells in that specified areas to loose gate control and turns on the parasitic BJT with consequent destruction of the device.

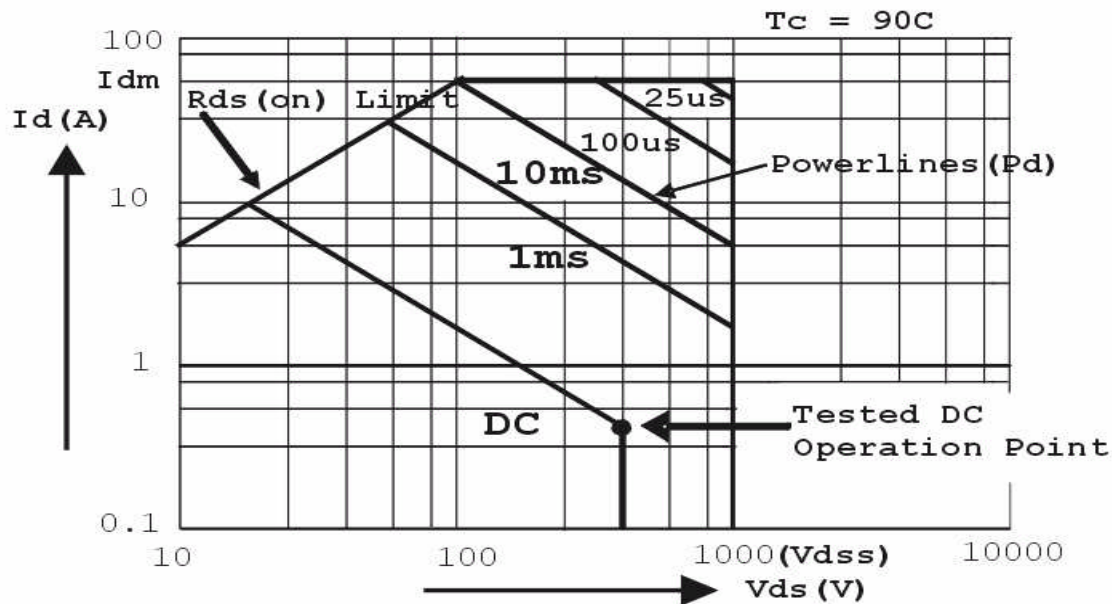


Figure 3: the FBSOA graph for the IXYS Linear Power MOSFET IXTK 22N100L IXYS Corporation has developed a Power MOSFET structure and process that provides an extended FBSOA capability by suppressing the positive feedback of Electro Thermal Instability. The design of these new MOSFETs has a non-uniform distribution of transistor cells, as well as having cells with different threshold voltages [3]. Every transistor cell is designed with a ballast resistor at the source to limit its current [4]. The

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parasitic BJT of each cell is heavily by-passed so that it will not turn-on under extreme electrical stress conditions. In addition, the thermal response of each Power MOSFET is tested to assure no solder voids. As a result, IXYS now offers a family of Power MOSFETs with extended FBSOA suitable for reliable operation in linear mode.

Datasheets of these MOSFETs contain guaranteed FBSOA graphs. For example, Figure 3 shows the FBSOA graph for IXYS linear Power MOSFET IXTK22N100L with its tested DC operation point marked. A list of currently available Power MOSFETs with extended FBSOA capability is shown in Table 1.

Table 1: N-Channel Power MOSFETs with extended FBSOA from IXYS

Part No	V _{dss} (V)	I _d (A)	R _{thJC} °C /W	The SOA Specification Power (W), T _c = 90 °C	Package Type
IXTH24N50L	500	24	0.31	200 @ V _{ds} = 400V, I _d = 0.5A	TO-247
IXTX46N50L	500	46	0.18	240 @ V _{ds} = 400V, I _d = 0.6A	PLUS247
IXTN46N50L	500	46	0.18	240 @ V _{ds} = 400V, I _d = 0.6A	SOT-227B
IXTK46N50L	500	46	0.18	240 @ V _{ds} = 400V, I _d = 0.6A	TO-264
IXTN62N50L	500	62	0.156	300 @ V _{ds} = 400V, I _d = 0.75A	SOT-227B
IXTB62N50L	500	62	0.156	300 @ V _{ds} = 400V, I _d = 0.75A	PLUS264
IXTH12N100L	1000	12	0.31	200 @ V _{ds} = 600V, I _d = 0.25A	TO-247
IXTX22N100L	1000	24	0.18	240 @ V _{ds} = 800V, I _d = 0.3A	PLUS247
IXTN22N100L	1000	24	0.18	240 @ V _{ds} = 800V, I _d = 0.3A,	SOT-227B
IXTK22N100L	1000	24	0.18	240 @ V _{ds} = 800V, I _d = 0.3A	TO-264
IXTN30N100L	1000	30	0.156	300 @ V _{ds} = 600V, I _d = 0.5A	SOT-227B
IXTB30N100L	1000	30	0.156	300 @ V _{ds} = 600V, I _d = 0.5A	PLUS264

Based on equation (2), a single power MOSFET such as IXTK22N100L with voltage rating of 1000V provides a power rating of 700W. This power rating is normally used in the circuit design for switch-mode operation but not for linear applications. For linear operation, IXYS provides a Safe Operating Area (SOA) rating that is obtained under a strict DC operation condition such as 240W at V_{DS} = 800V, I_D = 0.3A and T_C = 90°C for IXTK22N100L.

Application Examples

Active Load:

Consider a 2A/600V regulated power supply that needs to be tested with an active load comprised of multiple Power MOSFETs operating in parallel. In this application, Power MOSFETs should have a rating of 1000V for BV_{DSS} and be capable of dissipating the maximum output power plus a safety margin that includes the over-current protection.

The IXTK22N100L power MOSFET has voltage rating of 1000V and a power dissipation rating of 700W when used for switched mode operation. But this power rating cannot be used when computing its thermal limitations in linear applications. For this case, one must use its SOA rating of 240W at $V_{DS} = 800V$, $I_D = 0.3A$ and $T_C = 90^\circ C$. Assuming a 20% safety margin, this reduces its allowable power dissipation to 192W.

The maximum output power for the power supply is 1200W. Assume another 20% safety margin in the power in order to include over-current protection so that the multiple MOSFETs must be able to dissipate 1440W. As it can be seen, a single MOSFET does not have the capability to dissipate the total power. Thus a load bank with multiple Power MOSFETs connected in parallel is needed to carry the total power. The number of MOSFETs required to connect in parallel for this application is $1440/192 = 8$. A typical arrangement for the load circuit is shown in Figure 4.

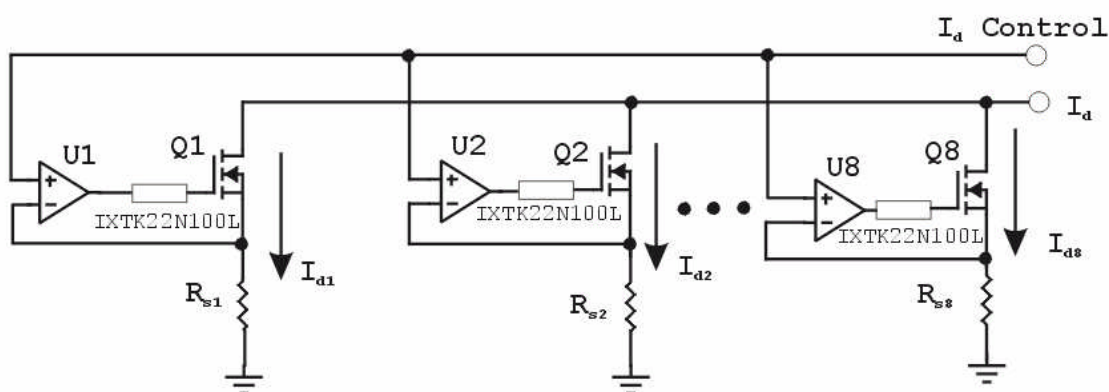


Figure 4: Active load for 2A/600V regulated power supply testing

The source or sense resistance (R_{s1} - R_{s8}) monitors the drain current in each MOSFET. The tolerance of the resistances determines the relative matching between the power MOSFETs. The voltage across the sense resistor is applied to the inverting input of each op amp driving the power MOSFET. The non-inverting input is connected to a control drain current [1].

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Motor Control:

Figure 5 portrays a motor control circuit in which a battery drives a motor in series with two power MOSFETs connected in parallel on the same heatsink.

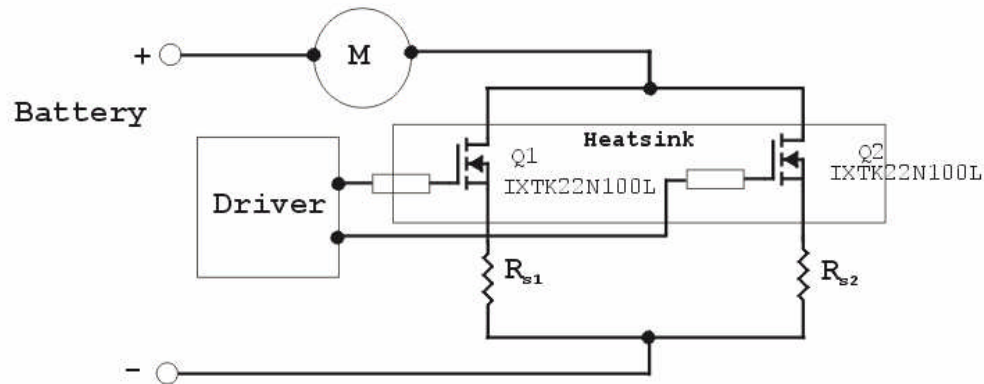


Figure 5: Linear Motor Control Circuit.

The drain current of Power MOSFETs operating in the linear mode is determined by the gate-source voltage. The voltage across the motor terminals is the difference between the battery and the drain-source voltage. The control is achieved through the gate driver, which checks the current flowing in the MOSFETs and establishes the right gate-source voltage.

Linear Regulator:

Figure 6 depicts a basic linear regulator whose output is regulated by controlling the voltage drop across the Pass Transistor. The Pass Transistor is biased in the linear region and acts as a variable resistor. It requires high power dissipation and large FBSOA. The N-Channel Power MOSFETs given in Table 1 can be chosen as Pass Transistor for high power requirements.

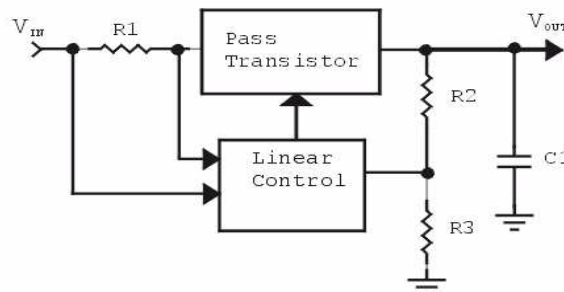


Figure 6: Basic Circuit Elements of a Linear Regulator

References:

- [1] Richard Frey, Denis Grafham, Tom Mackewich, “New 500V Linear MOSFETs for a 120 kW Active Load” Application Note, Advanced Power Technology (APT), 2000.
- [2] B. Jayant Baliga, “Power Semiconductor Devices” PWS Publishing Company, 1996.

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- [3] Nathan Zommer, Vladimir Tsukanov, "Non-Uniform Power Semiconductor Device" United States Patent # US 6710405B2, March 2004.
- [4] Nathan Zommer, "Monolithic Semiconductor Device and Method of Manufacturing Same" United States Patent # US 4860072, August 1989.