

Application Note AN-1144

IRS20957S Functional Description

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IRS20957S General Description

Note: The IRS20957S is an improved version of the IRS20955S. The IRS20955S is no longer recommended for new designs. For details, refer to application note AN-1141, IRS20955S and IRS20957S Comparison.

The IRS20957 is a high voltage, high speed MOSFET driver with a floating PWM input designed for Class D audio amplifier applications. Bi-directional current sensing detects over current conditions during positive and negative load currents without any external shunt resistors. A built-in protection control block provides a secure protection sequence against over-current conditions and a programmable reset timer. The internal dead-time generation block enables accurate gate switching and optimum dead-time setting for better audio performance, such as lower THD and lower audio noise floor.

For the convenience of half bridge configuration, the PWM input and protection logic are constructed on a floating well.

Typical Implementation

The following explanations are based on a typical application circuit with self-oscillating PWM topology shown in Figure 1. For further information, refer to the IRAUDAMP4 reference design.

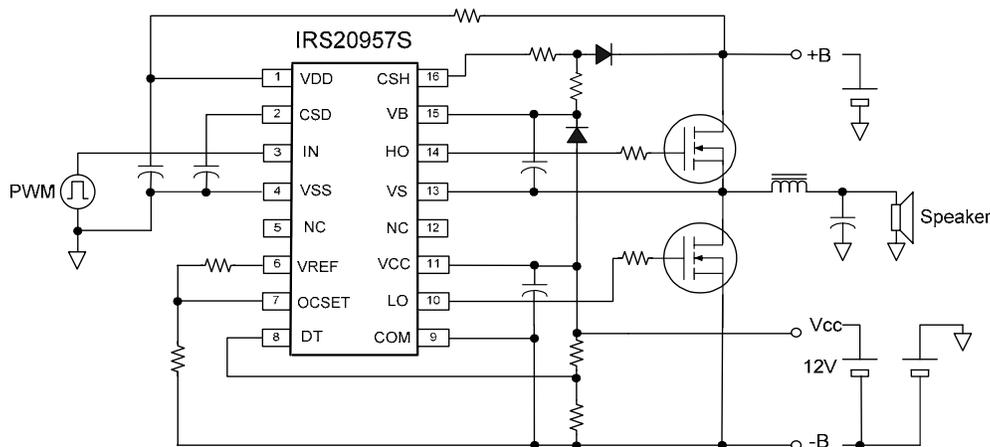


Figure 1. IRS20957 Typical Application Circuit

Floating PWM Input

The [IRS20957](#) accepts floating inputs, enabling easy half-bridge implementation. V_{DD} , CSD and IN refer to V_{SS} . As a result, the PWM input signal can directly feed into IN while referencing V_{SS} , which is typically the midpoint between the positive and negative DC bus voltages in a half-bridge configuration. The IRS20957 also accepts a non-floating input when V_{SS} is tied to COM.

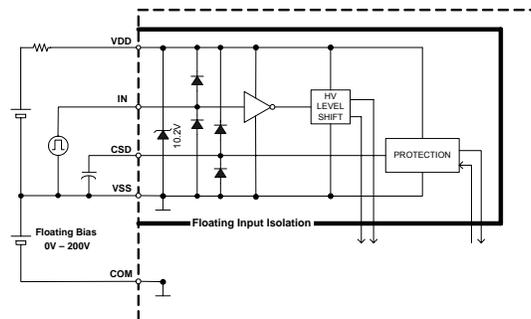


Figure 2. Floating PWM Input Structure

Over-Current Protection (OCP)

The IRS20957 features over-current protection to protect the power MOSFETs during abnormal load conditions. The IRS20957 starts a sequence of events when it detects an over-current condition during either high-side or low-side turn on of a pulse.

As soon as either the high-side or low-side current sensing block detects over-current:

1. The OC Latch (OCL) flips logic states and shutdowns the outputs LO and HO.
2. The CSD pin starts discharging the external capacitor C_t .
3. When V_{CSD} , the voltage across C_t , falls below the lower threshold V_{th2} , an output signal from COMP2 resets OCL.
4. The CSD pin starts charging the external capacitor C_t .
5. When V_{CSD} goes above the upper threshold V_{th1} , the logic on COMP1 flips and the IC resumes operation.

As long as the over-current condition exists, the IC will repeat the over-current protection sequence at a repetition rate dependent upon capacitance in CSD pin.

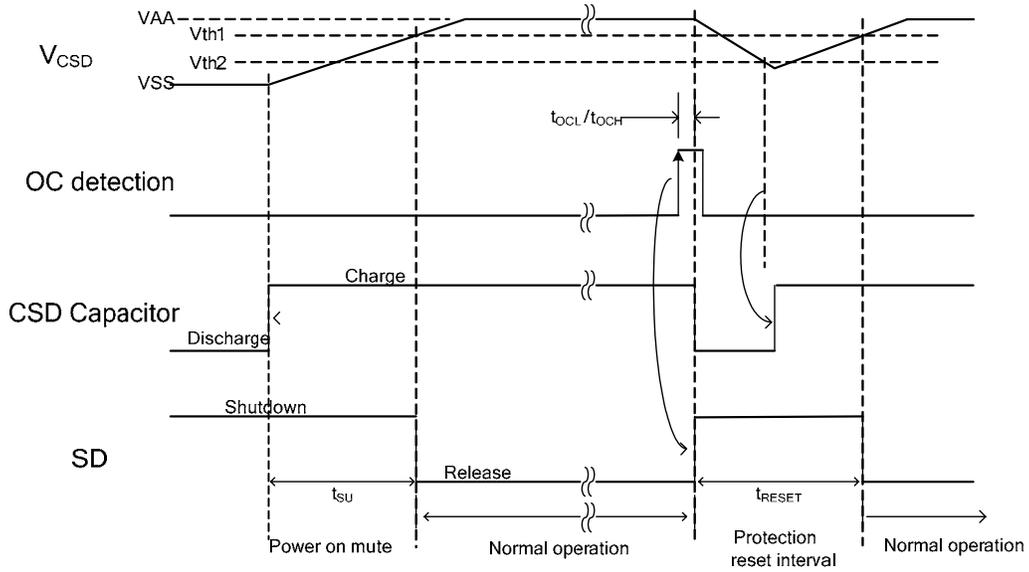


Figure 3. Over-Current Protection Timing Chart

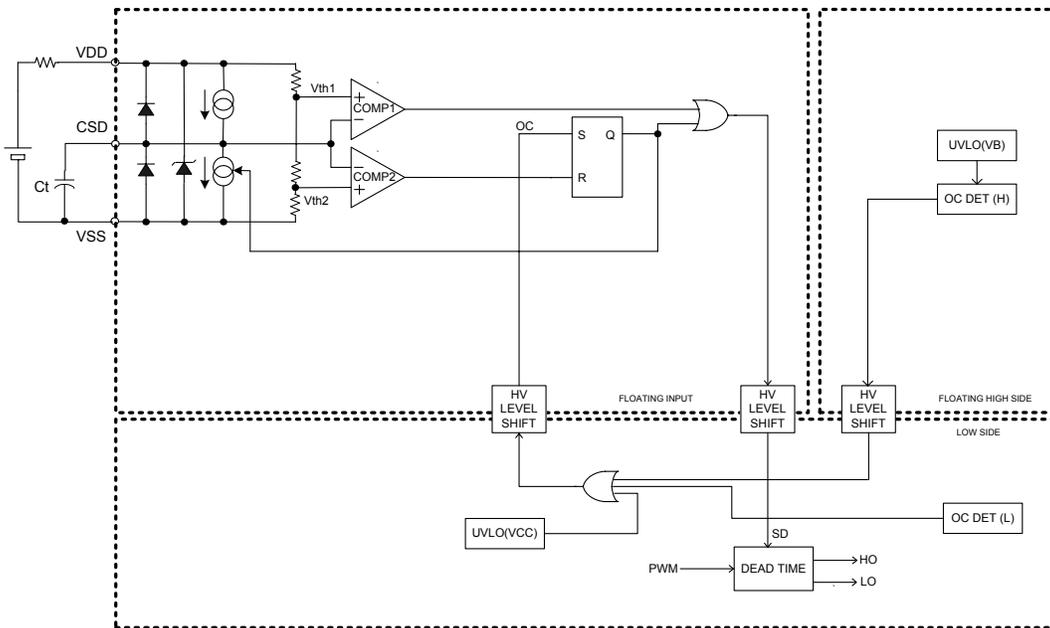


Figure 4. Shutdown Functional Block Diagram

Protection Control

The internal protection control block dictates the operational mode, normal, or shutdown, using the input of the CSD pin. In shutdown mode, the IC forces LO and HO to output 0V with respect to COM and VS respectively to turn off the power MOSFETs.

The CSD pin provides five functions.

1. Power up delay timer
2. Self-reset timer
3. Shutdown input
4. Latched protection configuration
5. Shutdown status output (host I/F)

Self Reset Protection

By putting a capacitor between CSD and VSS, the IRS20957 resets itself after entering the shutdown mode.

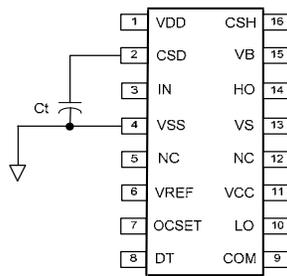


Figure 5. Self Reset Protection Configuration

Designing C_t

The timing capacitor, C_t , is used to program t_{RESET} and t_{SU} .

- t_{RESET} is the amount of time that elapses from when the IC enters the shutdown mode to the time when the IC resumes operation. t_{RESET} should be long enough to avoid over heating the MOSFET from the repetitive sequence of shutting down and resuming operation during over-current conditions. In most applications, the minimum recommended time for t_{RESET} is 0.1 second.
- t_{SU} is the amount of time between powering up the IC in the shutdown mode to the moment the IC releases shutdown to begin normal operation.

The values chosen for t_{RESET} and t_{SU} will determine the capacitance of C_t using the given equations:

The C_t determines t_{RESET} and t_{SU} as following equations:

$$t_{RESET} = \frac{C_t \cdot V_{DD}}{1.1 \cdot I_{CSD}} \quad [s]$$

$$t_{SU} = \frac{C_t \cdot V_{DD}}{0.7 \cdot I_{CSD}} \quad [s]$$

where I_{CSD} = the charge/discharge current at the CSD pin

V_{DD} = the floating input supply voltage with respect to V_{SS} .

Shutdown Input

The IRS20957 can be shut down by an external shutdown signal SD. Figure 6 shows how to add an external discharging path to shutdown the PWM.

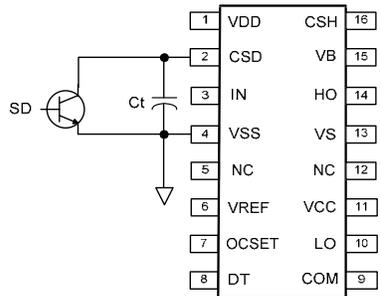


Figure 6. Shutdown Input

Latched Protection

Connecting CSD to V_{DD} through a $10k\ \Omega$ or less resistor configures the over-current protection latch. The latch locks the IC in shutdown mode after over-current is detected. An external reset switch can be used to bring CSD below the lower threshold V_{th2} for a minimum of 200 ns to properly reset the latch. After the power up sequence, a reset signal to the CSD pin is required to release the IC from the latched shutdown mode.

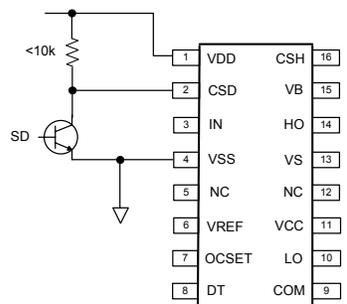


Figure 7. Latched Protection Configuration

Interfacing with System Controller

The IRS20957 can communicate with an external system controller through a simple interfacing circuit shown in Figure 8. A generic PNP transistor U1 detects the sink current at the CSD pin during an OCP event and outputs a shutdown signal to an external system controller. Another generic NPN transistor U2 can then reset the internal protection logic by pulling the CSD voltage below the lower threshold V_{th2} for a minimum of 200 ns. Note that the CSD pin is configured to operate in latched OCP. After the power up sequence, a reset signal to the CSD pin is required to release the IC from the shutdown mode.

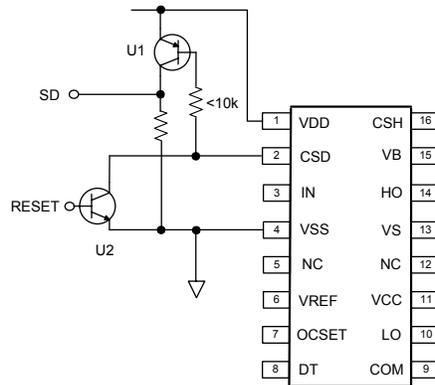


Figure 8. Interfacing with Host Controller

Programming OCP Trip Level

In a Class D audio amplifier, the direction of the load current alternates with the audio input signal. An over-current condition can therefore occur during either a positive current cycle or a negative current cycle. The IRS20957 uses the $R_{DS(ON)}$ of the output MOSFETs as current sensing resistors. Due to the structural constraints of high voltage ICs, current sensing is implemented differently for high side and low side. If the measured current exceeds a predetermined threshold, the OCP block outputs a signal to the protection block, forcing HO and LO low and protecting the MOSFETs.

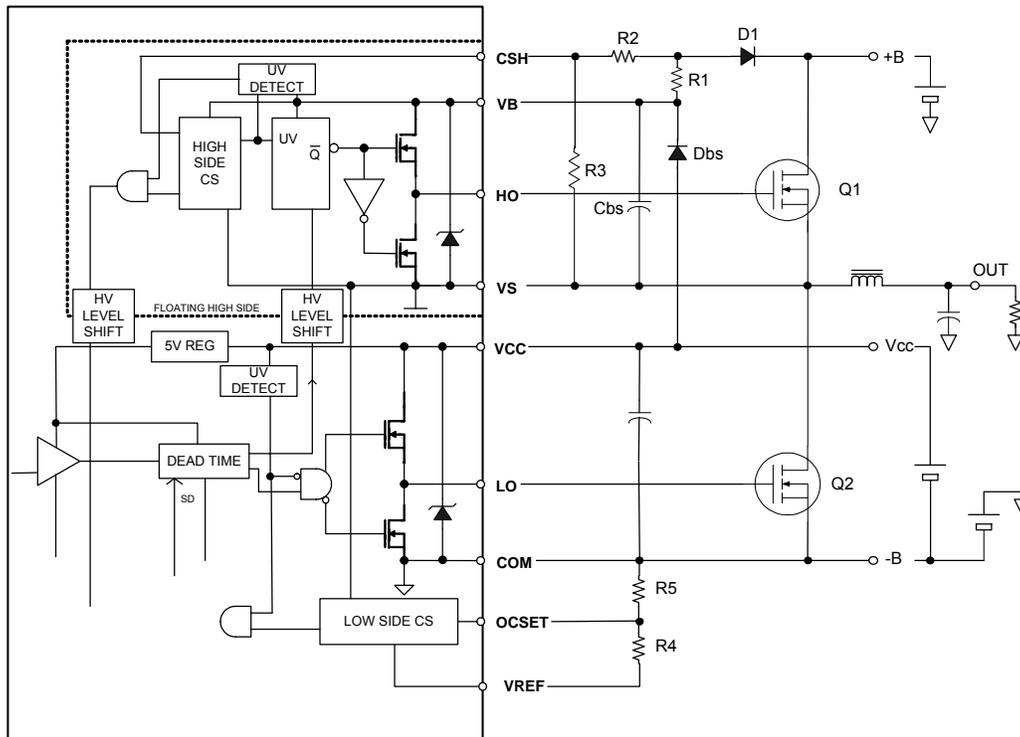


Figure 9. Bi-Directional Over-Current Protection

Low-side Over-Current Sensing

For negative load currents, low-side over-current sensing monitors the load condition and shuts down switching operation if the load current exceeds the preset trip level.

Low-side current sensing is based on the measurement of V_{DS} across the low side MOSFET during low-side turn on. In order to avoid triggering OCP from overshoot, a blanking interval inserted after LO turn on disables over-current detection for 450 ns.

The OCSET pin is used to program the threshold for low-side over-current sensing. When the V_{DS} measured across the low-side MOSFET exceeds the voltage at the OCSET pin with respect to COM, the IRS20957 begins the OCP sequence described earlier.

Note that programmable OCSET range is 0.5V to 5.0V. To disable low side OCP, connect OCSET to VCC directly.

To program the trip level for over current, the voltage at OCSET can be calculated using the equation below.

$$V_{OCSET} = V_{DS(Low\ Side)} = I_{TRIP+} \times R_{DS(ON)}$$

In order to minimize the effect of the input bias current at the OCSET pin, select resistor values for R4 and R5 such that the current through the voltage divider is 0.5 mA or more.

* Note: Using V_{REF} to generate an input to OCSET through a resistive divider provides improved immunity from fluctuations in V_{CC} .

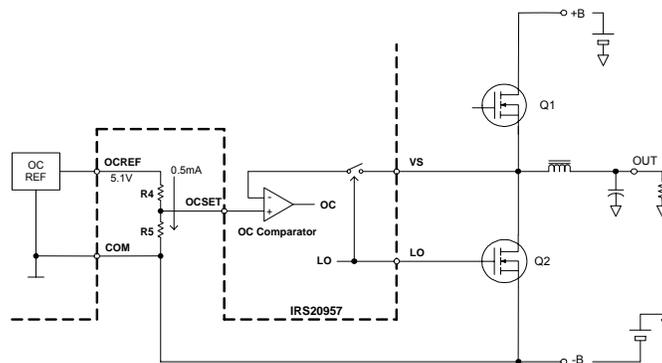


Figure 10. Low-Side Over-Current Sensing

Low-Side Over-Current Setting

Assume that the low side MOSFET has $R_{DS(on)}$ of 100m Ω . V_{OCSET} to set the current trip level at 30A is given by:

$$V_{OCSET} = I_{TRIP+} \times R_{DS(ON)} = 30\text{ A} \times 100\text{ m}\Omega = 3.0\text{ V}$$

Choose $R4+R5=10\text{ k}\Omega$ to properly load the VREF pin.

$$\begin{aligned} R_5 &= \frac{V_{OCSET}}{V_{REF}} \cdot 10\text{ k}\Omega \\ &= \frac{3.0\text{ V}}{5.1\text{ V}} \cdot 10\text{ k}\Omega \\ &= 5.8\text{ k}\Omega \end{aligned}$$

where $V_{REF} = 5.1\text{ V}$

Based on the E-12 series of resistor values, choose R5 to be 5.6 k Ω and R4 to be 3.9 k Ω to complete the design.

In general, $R_{DS(ON)}$ has a positive temperature coefficient that needs to be considered when setting the threshold level. Also, variations in $R_{DS(ON)}$ will affect the selection of external or internal component values.

High-Side Over-Current Sensing

For positive load currents, high-side over-current sensing also monitors the load condition and shuts down the switching operation if the load current exceeds the preset trip level.

High-side current sensing is based on the measurement of V_{DS} across the high-side MOSFET during high-side turn on through pins CSH and VS. In order to avoid triggering OCP from overshoot, a blanking interval inserted after HO turn on disables over-current detection for 450 ns.

In contrast to low-side current sensing, the threshold at which the CSH pin engages OC protection is internally fixed at 1.2V. An external resistive divider R2 and R3 can be used to program a higher threshold.

An external reverse blocking diode, D1, is required to block high voltages from feeding into the CSH pin while the high-side is off. Due to a forward voltage drop of 0.6V across D1, the minimum threshold required for high-side over-current protection is 0.6V.

$$V_{CSH} = \frac{R3}{R2 + R3} \cdot (V_{DS(HIGH\ SIDE)} + V_{F(D1)})$$

where $V_{DS(HIGH\ SIDE)}$ = the drain to source voltage of the high-side MOSFET during high-side turn on
 $V_{F(D1)}$ = the forward drop voltage of D1

Since $V_{DS(HIGH\ SIDE)}$ is determined by the product of drain current I_D and $R_{DS(ON)}$ of the high-side MOSFET. V_{CSH} can be rewritten as:

$$V_{CSH} = \frac{R3}{R2 + R3} \cdot (R_{DS(ON)} \cdot I_D + V_{F(D1)})$$

The reverse blocking diode D1 is forward biased by a 10 kΩ resistor R1.

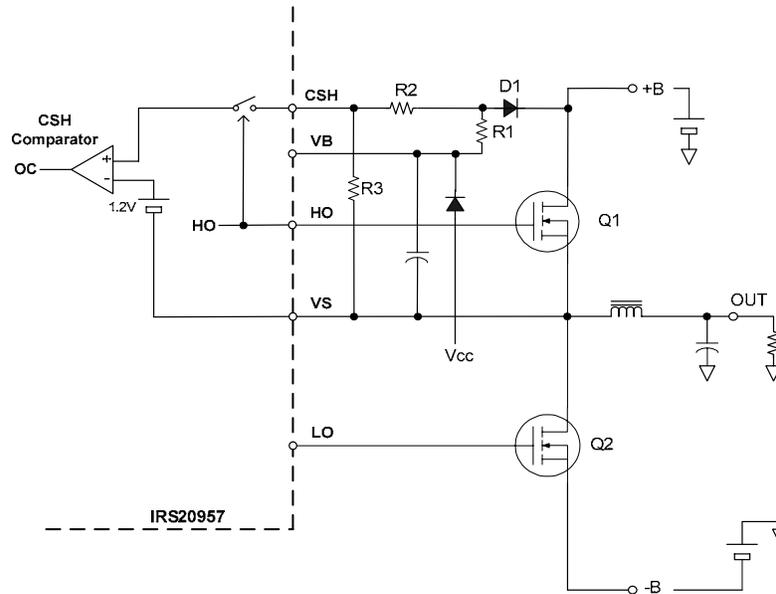


Figure 1. Programming High-Side Over-Current Threshold

High-Side Over-Current Setting

Figure 11 demonstrates the typical circuitry used for high-side current sensing. In the following example, the over-current protection level is set to trip at 30A using a MOSFET with an $R_{DS(ON)}$ of 100 m Ω . The component values of R2 and R3 can be calculated using the following formula:

Let $R_2 + R_3 = 10 \text{ k}\Omega$.

$$R_3 = 10 \text{ k}\Omega \cdot \frac{V_{th_{OCH}}}{V_{DS} + V_F}$$

where $V_{th_{OCL}} = 1.2\text{V}$

V_F = the forward voltage of reverse blocking diode D1 = 0.6V.

$V_{DS@ID=30A}$ = the voltage drop across the high-side MOSFET when the MOSFET current is 30 A.

Therefore, $V_{DS@ID=30A} = I_D \times R_{DS(ON)} = 30\text{A} \times 100 \text{ m}\Omega = 3\text{V}$

Based on the formulas above, $R_2 = 6.8 \text{ k}\Omega$ and $R_3 = 3.3 \text{ k}\Omega$.

Choosing the Right Reverse Blocking Diode

The selection of the appropriate reverse blocking diode D1 depends on its voltage rating and speed. To effectively block bus voltages, the reverse voltage must be higher than the voltage difference between +B and -B and the reverse recovery time must be as fast as the bootstrap charging diode. A diode such as the NXP BAV21 W, a 200V, 50 ns high-speed switching diode, is more than sufficient.

Deadtime Generator

Deadtime is the blanking period inserted between either high-side Turn-OFF and low-side Turn-ON, or low-side Turn-OFF and high-side Turn-ON. Its purpose is to prevent shoot through, or a rush of current through both MOSFETs. In the IRS20924(S), an internal deadtime generation block allows the user to select the optimum deadtime from a range of preset values. Selecting a preset deadtime through the DT pin voltage can easily be done through an external voltage divider. This way of setting deadtime prevents outside noise from modulating the switching timing, which is critical to the audio performance.

How to Determine Optimal Deadtime

The effective deadtime in an actual application differs from the deadtime specified in this datasheet due to the switching fall time, t_f . The deadtime value in this datasheet is defined as the time period between the beginning of turn-off on one side of the switching stage and the beginning of turn-on on the other side as shown in Figure 12. The fall time of the MOSFET gate voltage must be subtracted from the deadtime value in the datasheet to determine the effective deadtime of a Class D audio amplifier.

$$(\text{Effective deadtime}) = (\text{Deadtime in datasheet}) - t_f$$

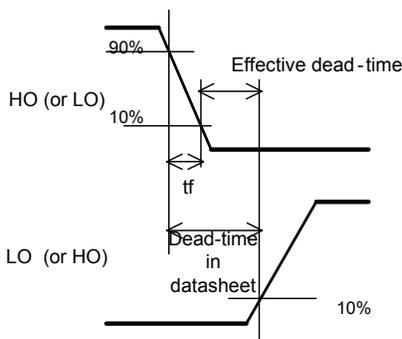


Figure 12. Effective Deadtime

A longer deadtime period is required for a MOSFET with a larger gate charge value because of the longer t_f . Although a shorter effective deadtime setting is beneficial to achieving better linearity in Class D amplifiers, the likelihood of shoot-through current increases with narrower dead-time settings. Negative values of effective dead-time may cause excessive heat dissipation in the MOSFETs, leading to potentially serious damage.

To calculate the optimal deadtime in a given application, the fall time t_f for both HO and LO in the actual circuit needs to be taken into account. In addition, variations in temperature and device parameters could also affect the effective deadtime in the actual circuit. Therefore, a minimum effective deadtime of 10 ns is recommended to avoid shoot-through current over the range of operating temperatures and supply voltages.

Programming Deadtime

The IRS20957 selects the deadtime from a range of preset deadtime values based on the voltage applied at the DT pin. An internal comparator translates the DT input to a predetermined deadtime by comparing the input with internal reference voltages. These internal reference voltages are set in the IC through a resistive voltage divider using V_{CC} . The relationship between the operation mode and the voltage at DT pin is illustrated in the Figure13 below.

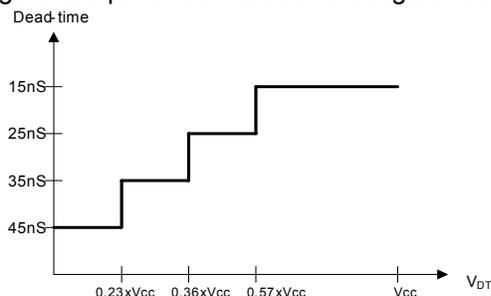


Figure 2. Deadtime vs. V_{DT}

Table 1 suggests pairs of resistor values used in the voltage divider for selecting deadtime. Resistors with up to 5% tolerance are acceptable when using these values.

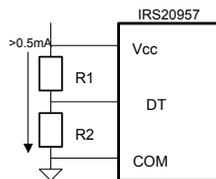


Figure 3. External Voltage Divider

Table 1 Recommended Resistor Values for Deadtime Selection

Deadtime Mode	R1	R2	DT Voltage
DT1	<10 k Ω	Open	V_{CC}
DT2	5.6 k Ω	4.7 k Ω	$0.46(V_{CC})$
DT3	8.2 k Ω	3.3 k Ω	$0.29(V_{CC})$
DT4	Open	<10 k Ω	COM

Supplying V_{DD}

V_{DD} is designed to be supplied with an internal Zener diode clamp. I_{DD} , the supply current for V_{DD} , can be estimated by:

$$I_{DD} \approx 1.5 \text{ mA} \times 300 \times 10^{-9} \times \text{switching frequency} + 0.5 \text{ mA} + 0.5 \text{ mA}$$

(Dynamic power consumption) (Static) (Zener bias)

The value of R_{DD} used to supply I_{DD} should meet the following requirement:

$$R_{DD} \leq \frac{V_{+B} - 10.2 V}{I_{DD}} \quad [\Omega]$$

Example: In the case where the average PWM switching frequency is 400kHz, the required I_{DD} is 1.18 mA. Based on this calculation, a 50V power supply voltage would require R_{DD} to be 33 k Ω or less.

Furthermore, make sure I_{DD} is below the maximum Zener diode bias current, I_{DDZ} , during static state conditions.

$$I_{DDZ} \geq \frac{V_{+B} - 10.2 V}{R_{DD}} - 0.5 mA$$

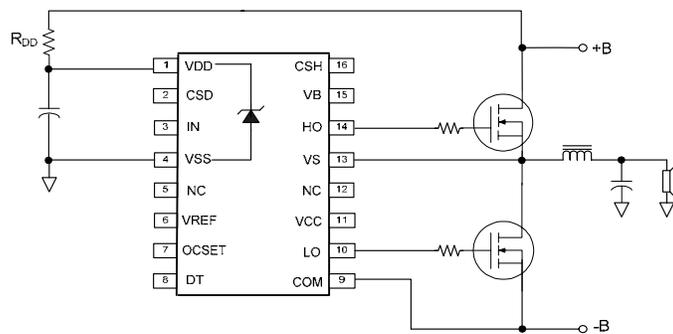


Figure 4. Supplying V_{DD}

Charging V_{BS} Prior to Start

The high-side bootstrap capacitor can be charged through a resistor from the positive supply bus to the V_B pin by utilizing an internal 15.3V Zener diode between V_B and V_S . This scheme provides proper PWM start-up with self-oscillating topologies.

The value of this charging resistor is subject to several constraints:

- The minimum value of R_{CHARGE} is limited by the leakage current of the bootstrap voltage supply through R_{CHARGE} , which would limit the maximum PWM modulation index of the system.
- The maximum value of R_{CHARGE} is limited by the current charge capability of the resistor during startup:

$$I_{CHARGE} > I_{QBS}$$

where I_{CHARGE} = the current through R_{CHARGE}
 I_{QBS} = the high side quiescent current.

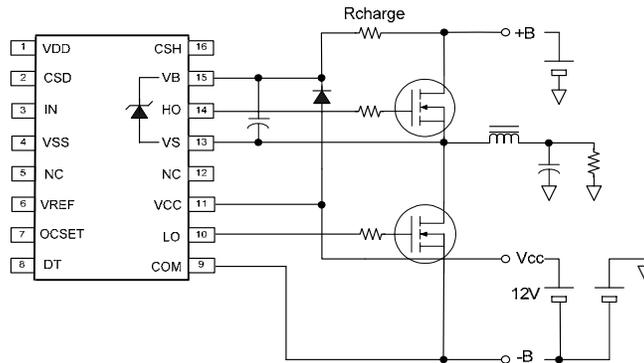


Figure 16. Boot Strap Supply Pre-charging

Start-up Sequence (UVLO)

The protection control block in the IRS20957 monitors the status of V_{DD} and V_{CC} to ensure that both voltage supplies are above the UVLO (under-voltage lockout) threshold before beginning normal operation. If either V_{DD} or V_{CC} is below the under voltage threshold, LO and HO are disabled in shutdown mode until both V_{DD} and V_{CC} rise above the voltage threshold.

Power-down Sequence

As soon as V_{DD} or V_{CC} falls below the UVLO threshold, protection logic in the IRS20957 turns off LO and HO, shutting off the power MOSFETs.

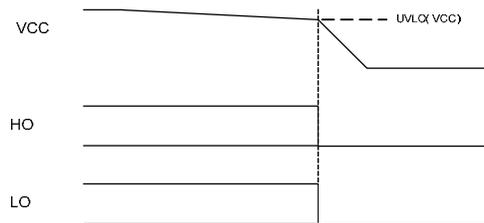


Figure 5. IRS20957 UVLO Timing Chart

Power Supply Decoupling

Ceramic capacitors of 0.1 μF or more should be placed close to the power supply pins of the IC on the board. Please refer to the application note [AN-978](#) for general design considerations of a high voltage gate driver IC.

V_{SS} Negative Bias Clamping

V_{SS} can go below COM when a negative supply is missing in a dual supply configuration. In this case, excessive negative V_{SS} voltage with respect to COM could damage the IRS20957. Having

a diode to clamp potential negative biases to V_{SS} is recommended to protect the IC. A standard recovery diode with a current rating of 1A such as the 1N4002 is sufficient for this purpose.

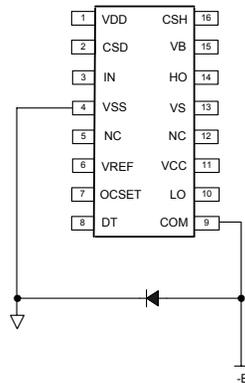


Figure 6. Negative V_{SS} Clamping

Junction Temperature Estimation

The power dissipation in the IRS20957 is dominated by the following items:

- P_{MID} : Power dissipation of the floating input logic and protection circuitry
- P_{LSM} : Power dissipation of the input level shifter
- P_{LOW} : Power dissipation in low-side
- P_{LSH} : Power dissipation of the high-side level shifter
- P_{HIGH} : Power dissipation in high-side

1. P_{MID} : Power Dissipation of the Floating Input Logic and Protection Circuitry

The power dissipation of the floating input section is given by:

$$P_{MID} = P_{ZDD} + P_{LDD} \approx \frac{V_{+BUS} - V_{DD}}{R_{DD}} \cdot V_{DD}$$

where

P_{ZDD} = the power dissipation from the internal Zener diode clamping V_{DD}

P_{LDD} = the power dissipation from the internal logic circuitry

V_{+BUS} = the positive bus voltage feeding V_{DD}

R_{DD} = the resistor feeding V_{DD} from V_{+BUS}

*For obtaining the value of R_{DD} , refer to the section "Supplying V_{DD} ."

2. P_{LSM} : Power Dissipation of the Input Level Shifter

$$P_{LSM} = 2 nC \times f_{sw} \times V_{SS, BIAS}$$

where

f_{SW} = the PWM switching frequency

$V_{SS,BIAS}$ = the bias voltage of V_{SS} with respect to COM

3. P_{LOW} : Power Dissipation in Low-Side

The power dissipation in low-side comes from the losses of the logic circuitry and the losses of driving LO.

$$P_{LOW} = P_{LDD} + P_{LO}$$

$$= (I_{QCC} \cdot V_{CC}) + \left(V_{CC} \cdot Q_g \cdot f_{SW} \cdot \frac{R_O}{R_O + R_g + R_{g(int)}} \right)$$

where

P_{LDD} = the power dissipation from the internal logic circuitry

P_{LO} = the power dissipation from the gate drive stage to LO

R_O = the output impedance of LO, typically 10 Ω for the IRS20957

$R_{g(int)}$ = the internal gate resistance of the low side MOSFET driver, typically 10 Ω for the IRS20957

R_g = the external gate resistance of the low side MOSFET

Q_g = total gate charge of the low side MOSFET

4. P_{LSH} : Power Dissipation of the High-Side Level Shifter

$$P_{LSH} = 0.4 \text{ nC} \times f_{SW} \times V_{BUS}$$

where

f_{SW} = the PWM switching frequency

V_{BUS} = the difference between the positive bus voltage and negative bus voltage

5. P_{HIGH} : Power Dissipation in High-side

The power dissipation in high-side comes from the losses of the logic circuitry and the losses of driving LO.

$$P_{HIGH} = P_{LDD} + P_{HO}$$

$$= (I_{QBS} \cdot V_{BS}) + \left(V_{BS} \cdot Q_g \cdot f_{SW} \cdot \frac{R_O}{R_O + R_g + R_{g(int)}} \right)$$

where

P_{LDD} = the power dissipation from the internal logic circuitry

P_{LO} = the power dissipation from the gate drive stage to HO

R_O = equivalent output impedance of HO, typically 10 Ω for the IRS20957

$R_{g(int)}$ = the internal gate resistance of the high-side MOSFET driver, typically 10 Ω for the IRS20957

R_g = external gate resistance of the high-side MOSFET

Q_g = total gate charge of the high- side MOSFET

Total power dissipation, P_d , is given by

$$P_d = P_{MID} + P_{LSM} + P_{LOW} + P_{HSM} + P_{HIGH} \cdot$$

Tj: Junction Temperature

Given $R_{th,JA}$, the thermal resistance between the ambient and junction temperature, T_J , the junction temperature, can be calculated from the formula provided below.

$$T_J = R_{th,JA} \cdot P_d + T_A < 150 \text{ } ^\circ\text{C}$$

Revision History

Date	Change
Xx/xx/2007	Initial online release
September 16 th , 2008	Updated for IRS20957S . IRS20955S is not recommended for new design. Charging VBS Prior to Start: Vbs Zener diode clamping voltage from 20.4V to 15.3V. Other minor language corrections.