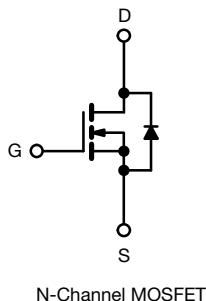
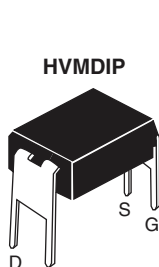


## Power MOSFET



### FEATURES

- Dynamic dV/dt rating
- Repetitive avalanche rated
- For automatic insertion
- End stackable
- Fast switching
- Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



### PRODUCT SUMMARY

V <sub>DS</sub> (V)	200	
R <sub>DS(on)</sub> (Ω)	V <sub>GS</sub> = 10 V	1.5
Q <sub>g</sub> (Max.) (nC)	8.2	
Q <sub>gs</sub> (nC)	1.8	
Q <sub>gd</sub> (nC)	4.5	
Configuration	Single	

### DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The 4 pin DIP package is a low cost machine-insertable case style which can be stacked in multiple combinations on standard 0.1" pin centers. The dual drain serves as a thermal link to the mounting surface for power dissipation levels up to 1 W.

### ORDERING INFORMATION

Package	HVMDIP
Lead (Pb)-free	IRFD210PbF

### ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25 °C, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-source voltage			V <sub>DS</sub>	200	V
Gate-source voltage			V <sub>GS</sub>	± 20	
Continuous drain current	V <sub>GS</sub> at 10 V	T <sub>A</sub> = 25 °C	I <sub>D</sub>	0.60	A
		T <sub>A</sub> = 100 °C		0.38	
Pulsed drain current <sup>a</sup>			I <sub>DM</sub>	4.8	
Linear derating factor				0.0083	W/°C
Single pulse avalanche energy <sup>b</sup>			E <sub>AS</sub>	79	mJ
Repetitive avalanche current <sup>a</sup>			I <sub>AR</sub>	0.60	A
Repetitive avalanche energy <sup>a</sup>			E <sub>AR</sub>	0.10	mJ
Maximum power dissipation	T <sub>A</sub> = 25 °C		P <sub>D</sub>	1.0	W
Peak diode recovery dV/dt <sup>c</sup>			dV/dt	5.0	V/ns
Operating junction and storage temperature range			T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C
Soldering recommendations (peak temperature)	For 10 s			300 <sup>d</sup>	

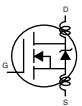

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- V<sub>DD</sub> = 50 V, starting T<sub>J</sub> = 25 °C, L = 82 mH, R<sub>g</sub> = 25 Ω, I<sub>AS</sub> = 1.2 A (see fig. 12)
- I<sub>SD</sub> ≤ 3.3 A, dI/dt ≤ 70 A/μs, V<sub>DD</sub> ≤ V<sub>DS</sub>, T<sub>J</sub> ≤ 150 °C
- 1.6 mm from case

**THERMAL RESISTANCE RATINGS**

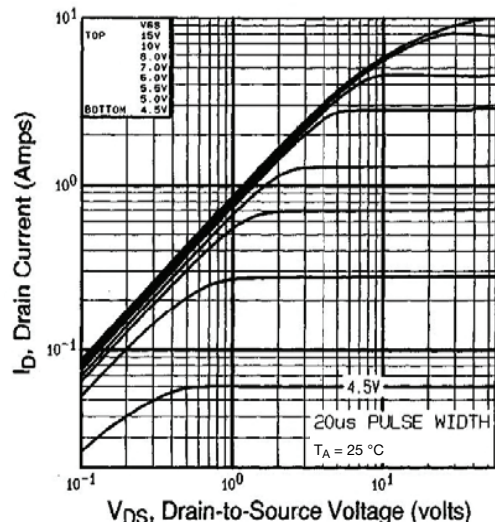
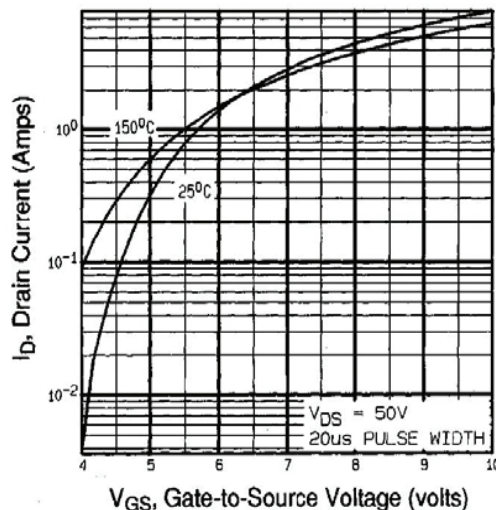
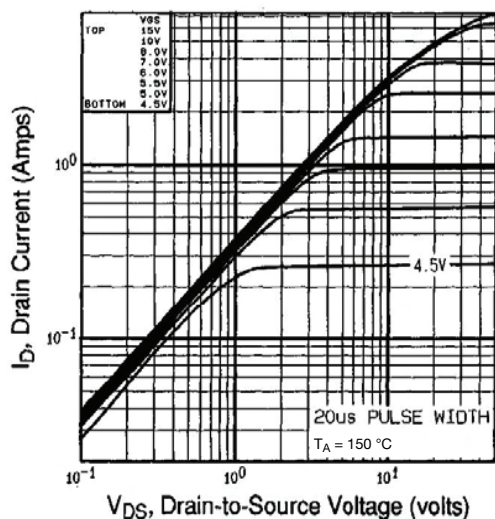
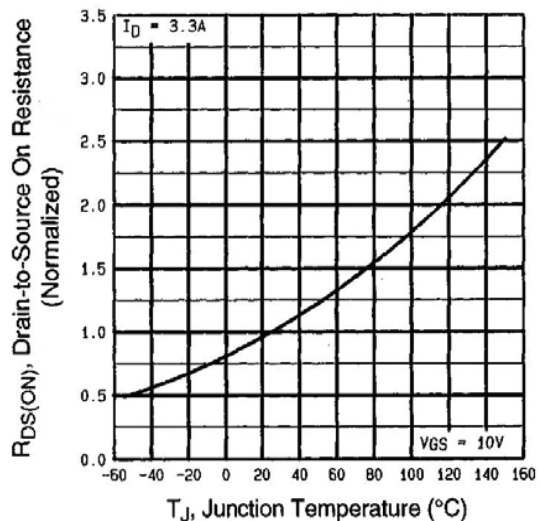
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	120	°C/W

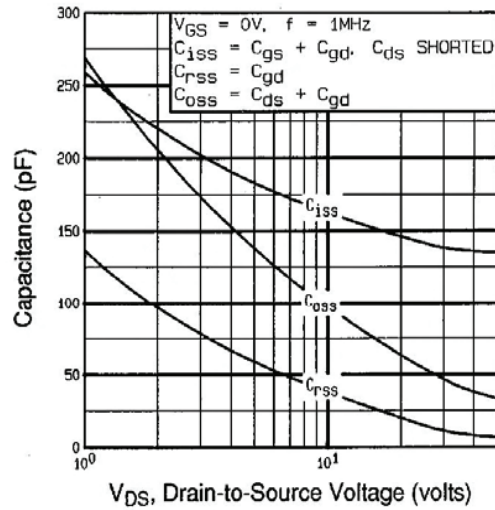
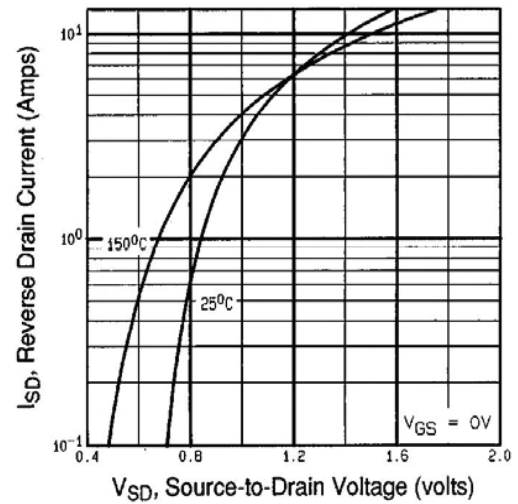
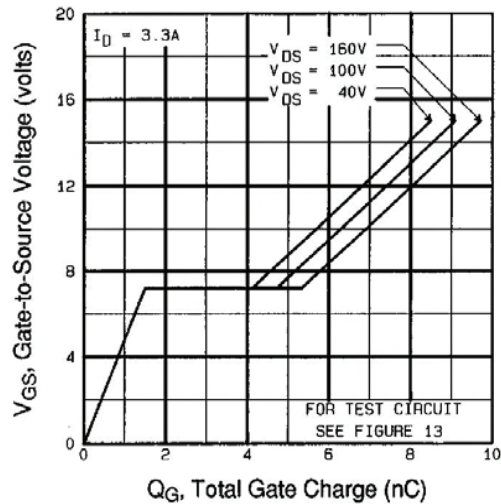
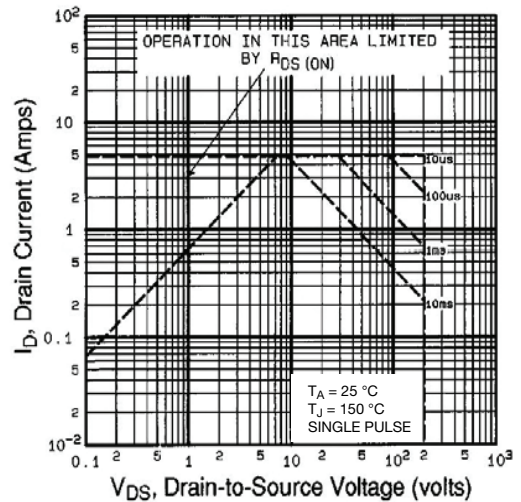
**SPECIFICATIONS** ( $T_J = 25\text{ °C}$ , unless otherwise noted)

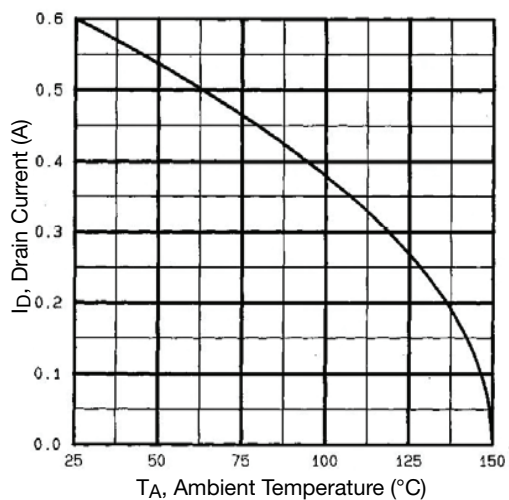
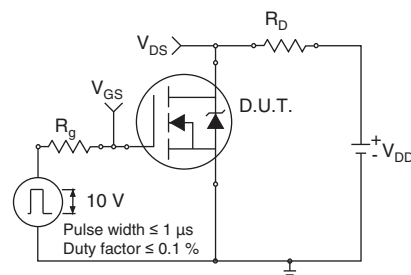
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA		200	-	-	V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	Reference to 25 °C, I <sub>D</sub> = 1 mA		-	0.30	-	V/°C
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		2.0	-	4.0	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 200 V, V <sub>GS</sub> = 0 V		-	-	25	μA
		V <sub>DS</sub> = 160 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C		-	-	250	
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 0.36 A <sup>b</sup>	-	-	1.5	Ω
Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 50 V, I <sub>D</sub> = 0.36 A <sup>b</sup>		0.10	-	-	S
Dynamic							
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V V <sub>DS</sub> = 25 V f = 1.0 MHz, see fig. 5		-	140	-	pF
Output Capacitance	C <sub>oss</sub>			-	53	-	
Reverse Transfer Capacitance	C <sub>rss</sub>			-	15	-	
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 3.3 A, V <sub>DS</sub> = 160 V see fig. 6 and 13 <sup>b</sup>	-	-	8.2	nC
Gate-Source Charge	Q <sub>gs</sub>			-	-	1.8	
Gate-Drain Charge	Q <sub>gd</sub>			-	-	4.5	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 100 V, I <sub>D</sub> = 3.3 A R <sub>g</sub> = 24 Ω, R <sub>D</sub> = 30 Ω, see fig. 10 <sup>b</sup>		-	8.2	-	ns
Rise Time	t <sub>r</sub>			-	17	-	
Turn-Off Delay Time	t <sub>d(off)</sub>			-	14	-	
Fall Time	t <sub>f</sub>			-	8.9	-	
Internal Drain Inductance	L <sub>D</sub>	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.0	-	nH
Internal Source Inductance	L <sub>S</sub>			-	6.0	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	0.60	A
Pulsed Diode Forward Current <sup>a</sup>	I <sub>SM</sub>			-	-	4.8	
Body Diode Voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 0.60 A, V <sub>GS</sub> = 0 V <sup>b</sup>		-	-	2.0	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = 3.3 A, dI/dt = 100 A/μs <sup>b</sup>		-	150	310	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			-	0.60	1.4	μC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> and L <sub>D</sub> )					

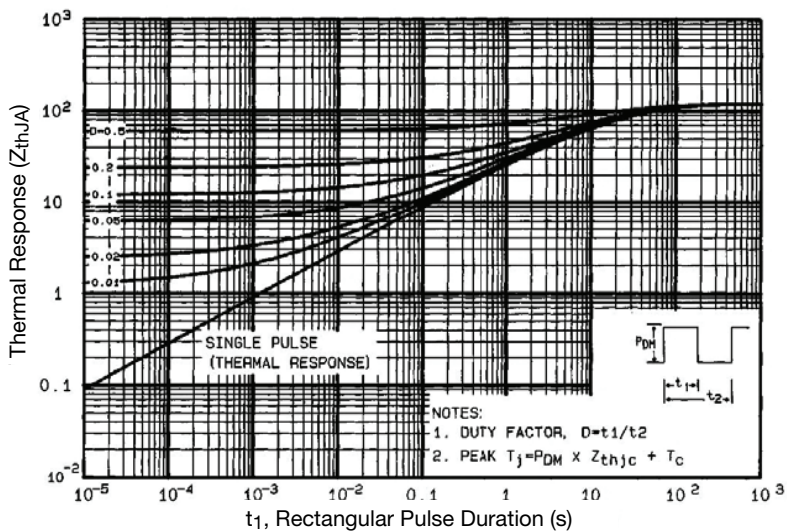
**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)  
b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Fig. 1 - Typical Output Characteristics,  $T_A = 25\text{ }^{\circ}\text{C}$** 

**Fig. 3 - Typical Transfer Characteristics**

**Fig. 2 - Typical Output Characteristics,  $T_A = 150\text{ }^{\circ}\text{C}$** 

**Fig. 4 - Normalized On-Resistance vs. Temperature**


**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**

**Fig. 7 - Typical Source-Drain Diode Forward Voltage**

**Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage**

**Fig. 8 - Maximum Safe Operating Area**


**Fig. 9 - Maximum Drain Current vs. Ambient Temperature**

**Fig. 10a - Switching Time Test Circuit**

**Fig. 10b - Switching Time Waveforms**

**Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Ambient**

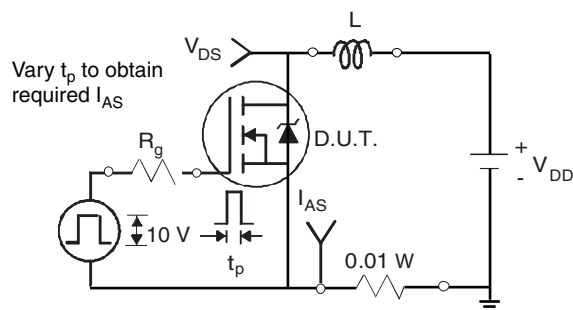


Fig. 12a - Unclamped Inductive Test Circuit

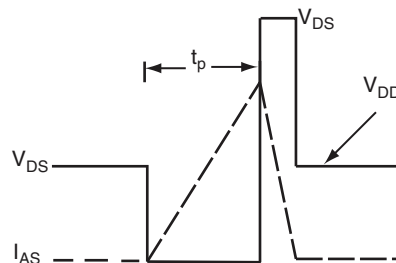


Fig. 12b - Unclamped Inductive Waveforms

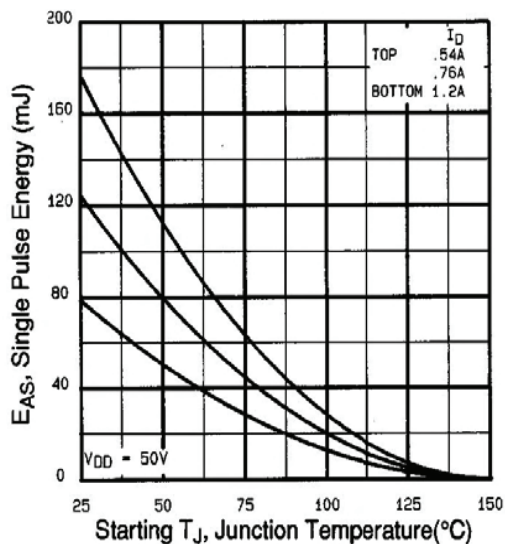


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

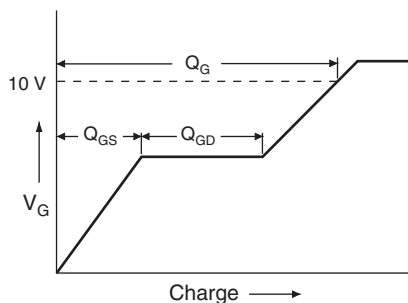


Fig. 13a - Basic Gate Charge Waveform

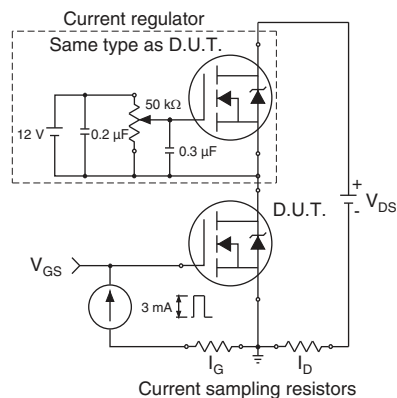
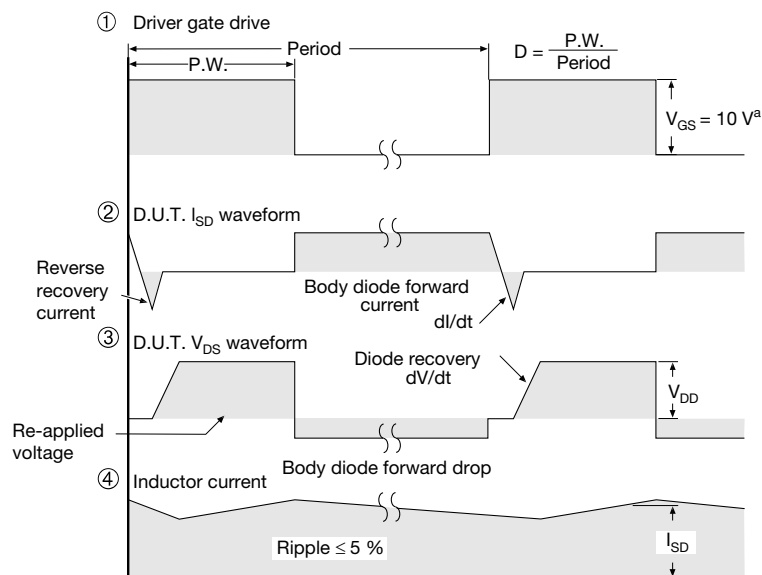
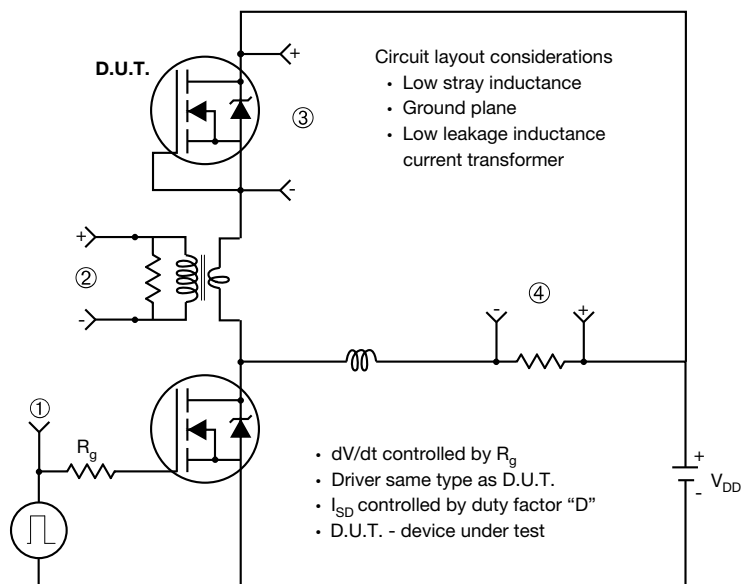


Fig. 13b - Gate Charge Test Circuit



## Peak Diode Recovery dV/dt Test Circuit



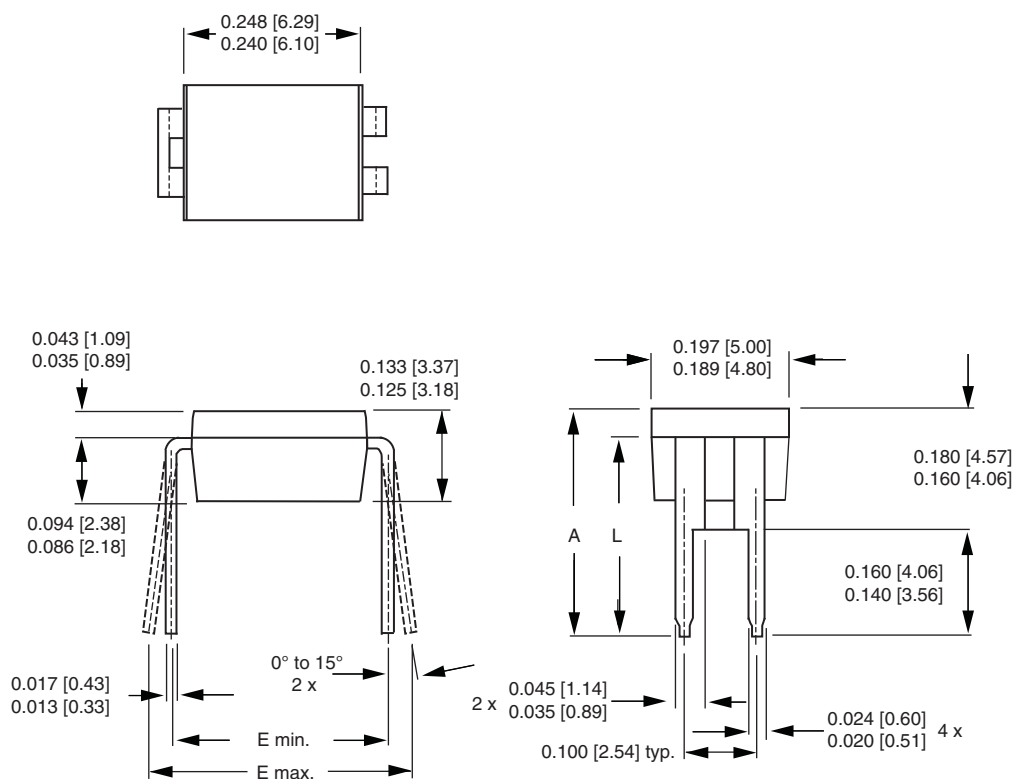
### Note

a.  $V_{GS} = 5\text{ V}$  for logic level devices

**Fig. 14 - For N-Channel**

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## HVM DIP (High voltage)



DIM.	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.310	0.330	7.87	8.38
E	0.300	0.425	7.62	10.79
L	0.270	0.290	6.86	7.36

ECN: X10-0386-Rev. B, 06-Sep-10  
DWG: 5974

### Note

- Package length does not include mold flash, protrusions or gate burrs. Package width does not include interlead flash or protrusions.





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