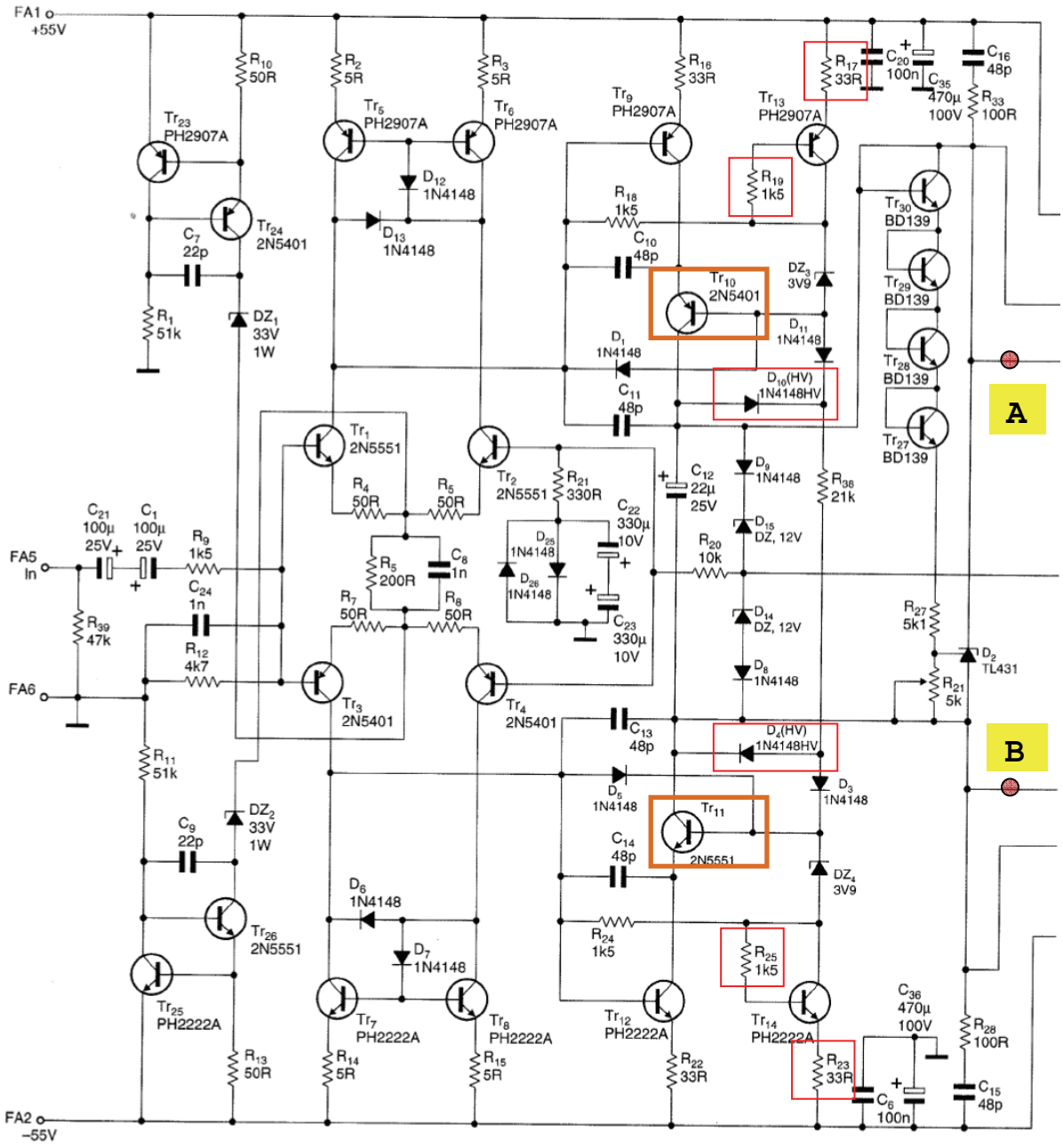
Improving the robustness of the Ultra-fast Audio Power Amplifier



case V_{os} is limited to few hundred millivolt. This represents an acceptable level of output offset.

Filtering added. Another change made to increase flexibility is to allow the possibility of incorporating an input pass-band filter, via components C_1 and C_{21}, together with R_{12} for the high-pass section and R_9+C_{24} for the low-pass section.

In the following analysis, C_1 and C_{21} are considered equal to $2C_H$. With component value shown, the –3 dB bandwidth is 1Hz to 120kHz. Assuming that the signal source resistance, which is usually lower than 300Ω, has no influence, high-pass and low-pass frequency corners are given by

$$f_H = \frac{1}{2\pi R_H C_H}$$

and

$$f_L = \frac{1}{2\pi R_L C_{24}}$$

respectively, where R_H is the sum R_{12}+R_9, and R_L is the parallel R_{12}//R_9. They are easily adapted, and the low-pass section can be bypassed by omitting C_{24} and shorting R_9.

Improved temperature sensing. The temperature-sensing network *TS* incorporates an additional transistor. This adds

Fig. 1. Detailed circuit diagram of the chosen practical implementation of the 100W/8Ω audio-power amplifier, featuring a speed higher than 300V/µs and rated power thd figures of 0.002% and 0.018% at 1kHz and 20 kHz, respectively. All diodes are 1N4448 Diodes D_4 and D_{10} marked 1N4448HV are still 1N4448, but selected for a reverse voltage higher than 120V. This selection is made by applying a reverse voltage of 130V via a resistor of 10kΩ and measuring the current, which has to be less than 10mA. The yield is normally higher than 50%.

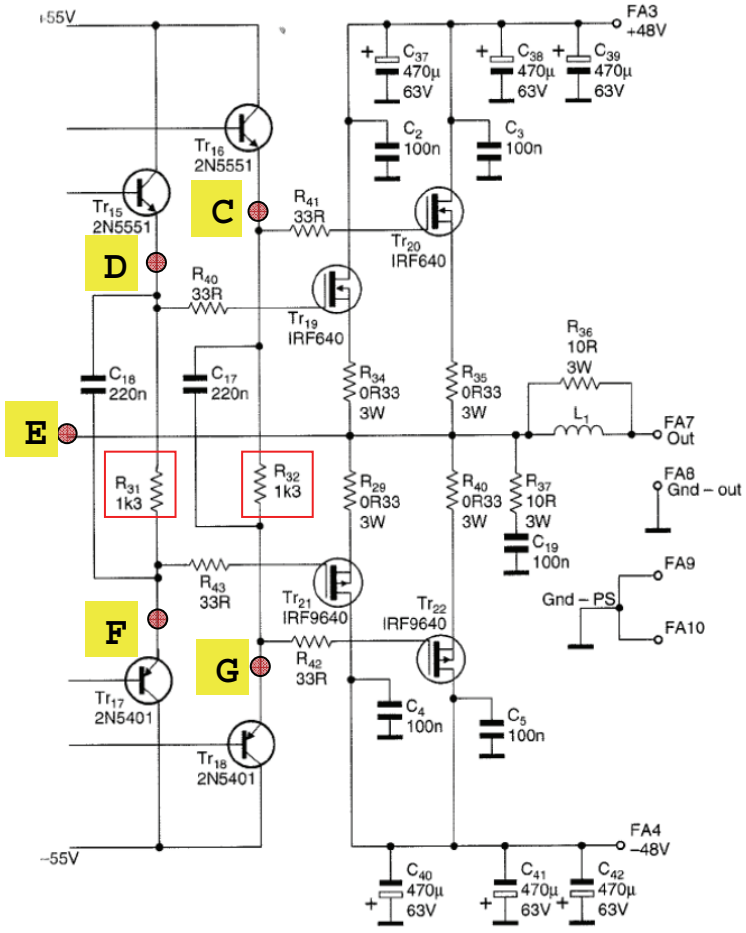


Table 2. Slewing performance of the audio power amplifier for a source resistance of 50Ω and an 8Ω load. Pulse input was 6V peak, as in Fig. 4 of my previous article.[1]

Characteristic results	Measurement
Positive slew-rate	+320V/µs
Negative slew-rate	–300V/µs

Table 3 . Total harmonic distortion figures of the final 100W/8Ω audio power amplifier for a source resistance of 50Ω and an 8Ω load. Quiescent current was 150mA and bandwidth 80kHz.

V_{out}, pk-pk	1kHz	20kHz
5	0.0030%	0.0043%
10	0.0028%	0.0047%
20	0.0023%	0.0061%
40	0.0028%	0.0110%
80	0.0026%	0.0170%

Note: Total harmonic distortion remains virtually constant when source impedance R_s varies in the range 50Ω to 5kΩ. The instrumentation limit, thd+noise, was 0.002% at 1kHz; 0.003% at 20kHz.

extra flexibility to the mounting mode of the temperature-sensing network relative to the power output devices Tr_{19-22}.

In my original prototype, the three sensing transistors were mounted very close to output power mosfets. A total $\Delta V_{TS}/\Delta T$ of –6mV/°C was adequate.

However, when a more practical scheme for mounting the temperature-sensing network on the heat sink is needed, like the one presented here, you have to allow a looser thermal coupling with power devices. Because of this, $\Delta V_{TS}/\Delta T$ will be higher and it may turn out that a greater number of temperature sensing transistors will be needed.

In the layout scheme proposed, four transistors providing a $\Delta V_{TS}/\Delta T$ of –8mV/°C were x found adequate to provide a fairly stable – within 20% – output power mosfets bias setting under a wide range of operating conditions.

The quiescent current of output devices has been set to 150mA, which further contributes to the thermal stability of the operating point of the output mosfets. The

Table 1. Main characteristics of the fast audio power amplifier for 150mA quiescent current and 80kHz bandwidth.

Characteristic	Measurement results
Measured output offset voltage	+32mV
DC open-loop gain	110dB
Low-frequency closed loop gain	32dB
Small-signal bandwidth before the output filter (–3dB)	20Hz (–0.1dB), 1.3MHz
Unity gain frequency before the output filter	22MHz
Open-loop gain at 20kHz	66dB
Closed-loop amplifier phase margin before the output filter	+76°
Output noise (BW=80kHz, input terminated with 50Ω)	42µV rms
Slew rate	See Table 2
Total harmonic distortion (thd)	See Table 3

Background: the original design and the reasons for some circuit changes

The final schematic of the Ultra-fast amplifier was published in August 1998 in EW+WW (Electronics World + Wireless World) and is reported in the above pages. It is aligned with to the pcb provided to EW+WW readers.

Main characteristics and criticalities are as follows:

1- Input stage (Tr1 to Tr4): idle current of each transistor is about 2mA; the peak current for a (nominal) differential input peak-to-peak voltage of $\pm 3V_{p\text{-}p}$ ranges from a static 6mA (limited mainly by R_5) up to a dynamic (short time) 18mA (limited by R_4,R_5, R_7 and R_8; time duration defined by C8). They correspond to about 300mW of continuous power and 1.2W of instantaneous power dissipated by the transistors, respectively.

2-Intermediate stage (IS) BJT's (Tr9, Tr10, …): nominal idle current is about 7mA (and 350mW), but due to temperature variations, component tolerance and device mismatches can exceed 10mA. The peak current is limited to about 110mA. So idle dissipated power of Tr9 and Tr10 can exceed 500mW while the instantaneous power (say <1uS in normal operation) can exceed 5W, which can seriously stress both transistors if the frequency of input transients is excessive (especially in the test phases).

3- Output stage driver (Tr16 to Tr18): idle current is a stable 6mA (300mW at Vce=50V) which is enough to drive the output MOSFET's to a full $80V_{P\text{-}P}$ output swing in class-A up to 200kHz. However no limit is set for the peak collector current (for sonic reasons), and therefore these transistors could experience level of stress rather high in critical operating conditions, e.g. power on/off, signal overload and high ambient temperatures. Simulations show that the instantaneous dissipated power during fast rated input transients (<200ns) is about 5W, yet within the safe operating area (SOA) of the devices.

4- double dual power supply voltages ($\pm$55V and $\pm$48V) was suggested in order to increase the overall amplifier efficiency

Considerations:
1- the amplifier was designed to be robust enough to manage the reproduction of audio programs (even the most demanding in terms of speed) with **occasional very-fast transients**, where all stages can provide for a short time the **extremely high currents needed to sustain its high speed**.

2- However there are some potentially critical situations where some transistors (Tr10, Tr11 and Tr16 to Tr18) could be stressed beyond their safe operation limits, e.g.:
- **power on/off** especially with double separated supply voltages;
- too **high a frequency of occurrence** of very fast transients;
- **severe input/output overload**, again .. especially with double separated supply voltages;
- **the test phase**, which in my opinion, if not well managed, can potentially be the most critical.

3- I propose a simple solution here to limit the stress of critical BJT's in all the above critical situations above mentioned, and to substantially reduce the risk of failure in ultra-fast amplifiers. More specifically this solution mainly addresses those amplifiers built on the PCB designed for EW+WW with the goal of avoiding the need to cut any trace!

4- a revised and upgraded design solution (the **Ultra-fast Amplifier 2.0** ?) is by now under development and will be soon assembled and tested (and hopefully published) in a near future.

Details of the recommended solution

1- Recommendation #1: use a single dual (unregulated) supply voltage of nominal +55V and -55V both for all stages of the amplifier, adding, if appropriate, an extra decoupling filter for the input and the intermediate stages

2- Recommendation #2: incorporate/add the circuit in Fig.1 below to improve the robustness and operational capabilities of the driver of power MOSFET's, which will become (as shown in Fig.2) more robust in all operating conditions and capable to extend its operation to class-B when requested. I suggest a hard accommodation of all additional components on the soldering side of the existing PCB. There is no need to cut any trace!

3- Recommendation #3: replace in a sequence (and in accordance to actual needs) the values of some components as shown in the table 1 here below

Table 1

step	component	current value	replace with	desired effect/comments
1	R_{17}, R_{23}	33Ω	5Ω	reduce Tr_{10}-Tr_{11} idle current I_Q(IS) to about 6-7mA (if needed)
2	R_{19}, R_{25}	1.5kΩ	5Ω	to be done only if step 1 is not enough: I_Q(IS) about 6-7mA
3	Tr_{10}	2N5401	2 x 2N5401 (*)	**optional step** in order to increase robustness of intermediate stage (penalty: slew-rate slightly reduced)
4	Tr_{11}	2N5551	2 x 2N5551 (*)	
5	R_{31}, R_{32}	1.3kΩ	2.4kΩ	Tr_{15},Tr_{17}, Tr_{18},Tr_{19} idle current (power!) reduced to 3-4mA
6	D_4-D_{10}(HV)	1N4148(HV)	BAV21	avoid selection of 1N4148 (BAV21 is a 200V fast diode)

(*) **transistor matched within ΔVbe ≦ 10mV @ Ic=5mA**

Fig.1-The additional circuitry to be integrated into the ultra-fast amplifier schematic

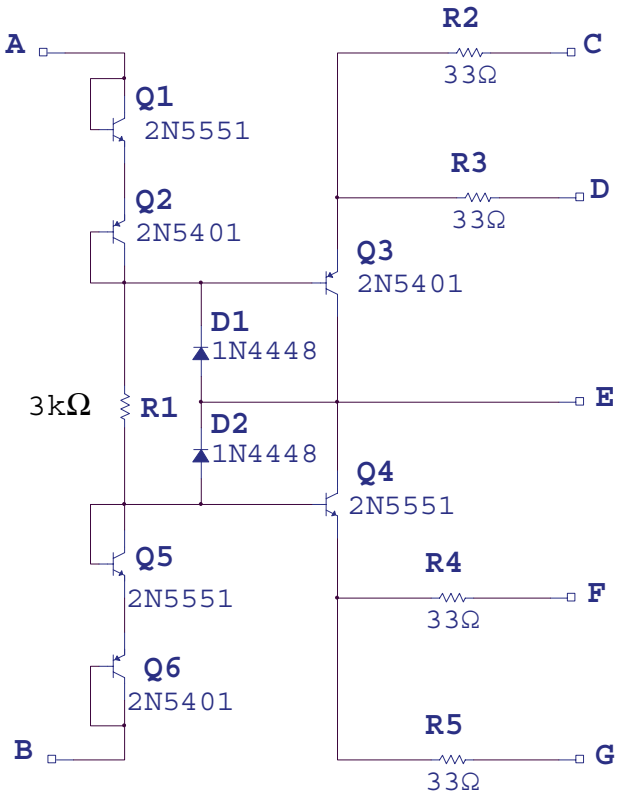


Fig. 2-Overall view of the complete driver circuit