I2S FIFO II KIT user guide

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Introduction

The digital audio stream consists of two parts: the data and the clock. Usually we don't have any problems with data. However, the clock is not perfect (there are no ideal clocks in the real world); it comes with jitter (or phase noise). Jitter is the main reason why different digital audio sources sound different even when they are played from the same audio stream.

An asynchronous I2S FIFO is a kind of logic device which can buffer the digital audio stream, allowing the audio data to pass through while isolating the original clock and replacing it with a new secondary clock. If the new clock has less phase noise than the old one, the digital audio stream after the FIFO will have less jitter and that will make the DAC or other digital audio device playing the stream sound better. Moreover, the sound quality of the playback will be independent from the digital audio source. So, together with clock technology, the I2S FIFO is firmly believed to be one of the most effective solutions to deal with jitter.

This I2S FIFO II KIT is upgraded from audiophile well-reputed FIFO I with the most up to date technology. It's a very flexible and expandable design with stacking possibility when integrating with other boards.

I2S FIFO II Board features and specifications

▪ Two I2S inputs

- LVTTL (3.3V) logic input level with 5V TTL tolerant.
- 44.1 KHz, 48 KHz, 88.2 KHz, 96 KHz, 176.4 KHz, 192 KHz, 352.8KHz, 384KHz - 16bit, 24bit or 32bit.

▪ I2S input selection

- I2S input ports can be selected by a jumper or a on/off switch on front panel.

- Switching between two I2S sources is a glitch-free design. At the moment of switching, FIFO II output will keep streaming with no stops on any of the clock signals, such as MCLK, SCK/BCK and WS/LR, but SD/DATA will become zero to keep digital silence until new I2S signal is locked.

▪ I2S output

- LVTTL (3.3V) logic output level.
- 44.1 KHz, 48 KHz, 88.2 KHz, 96 KHz, 176.4 KHz, 192 KHz, 352.8KHz, 384KHz - 16bit, 24bit or 32bit.

▪ FIFO Memory

- 4Mb SRAM.
- Speed 10ns.

▪ FIFO initial delay time

Fs	44.1KHz	48KHz	88.2KHz	96KHz	176.4KH	192KHz	352.8KH	384KHz
Delay(s)	0.74	0.68	0.37	0.34	0.18	0.17	0.09	0.085

▪ Clock boards integration

- Can be integrated with various clock boards such as Dual XO Clock Board I/ II and Si570 clock board.

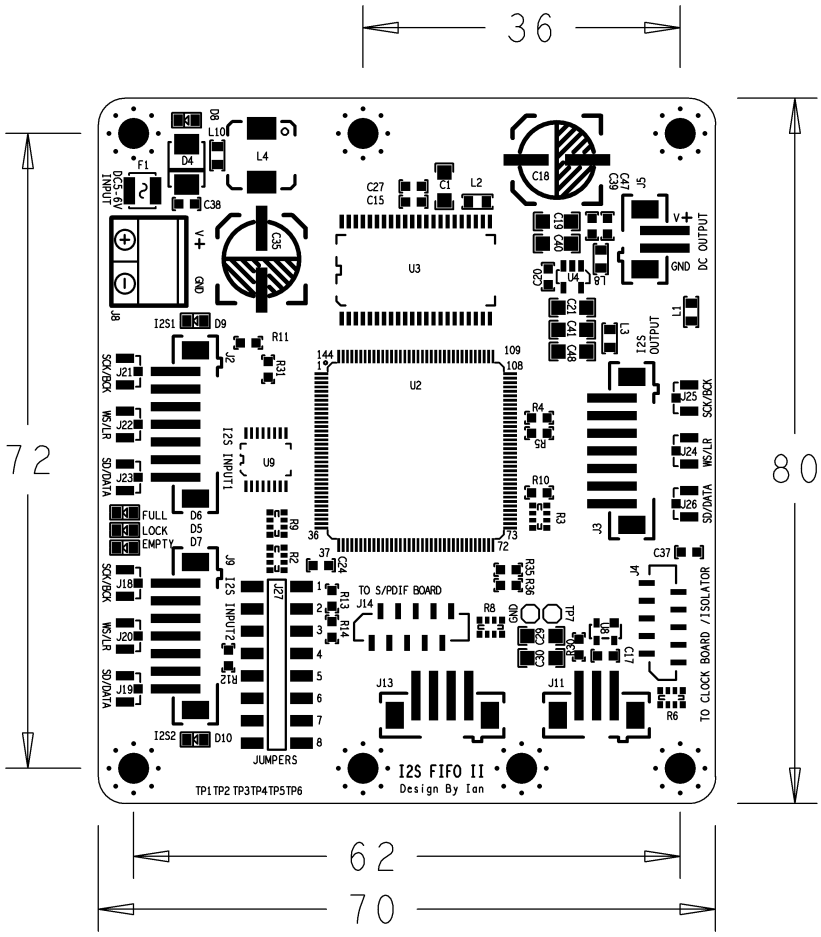
▪ S/PDIF Interface Board integration

- Can be set up as an S/PDIF FIFO when integrated with S/PDIF board.

KIT includes

- An assembled and tested I2S FIFO II PCB with attached frame and Single XO Clock Board
- Two 8" single-ended PH 2.0mm 7-pin I2S cables
- One 2.5" double-ended PH 2.0 mm 7-pin I2S bridge cable (already connected on the board)
- One 2.5" 10-pin FPC/FFC cable (already be connected on the board)
- Five shunt jumpers

Layout and dimensions (in mm)



Connectors

- DC Power input: J8, 2-pin 5.0mm terminal block DC 5V-6V

FIFO II itself consumes around 70mA average current when running at 98.3040MHz. Current consumption of clock board needs to be taken into account additional if it is powered by FIFO II.

- Two I2S inputs:

J2 (INPUT1) and J9 (INPUT2), two PH 2.0mm 7-pin connectors, configured as:

1	2	3	4	5	6	7
GND	SCK/BCK	GND	WS/LR	GND	SD/DADA	GND

or, six U.FL coaxial cable connectors, configured as:

INPUT1	J21	J22	J23
INPUT2	J18	J20	J19
I2S signals	SCK/BCK	WS/LR	SD/DADA

- I2S output:

J3, a PH 2.0mm 7-pin connector, configured as:

1	2	3	4	5	6	7
GND	SCK/BCK	GND	WS/LR	GND	SD/DADA	GND

or, three U.FL coaxial cable connectors, configured as:

J25	J24	J26
SCK/BCK	WS/LR	SD

- Clock board interface: J4, FPC/FFC 1.0mm 10-pin connector, double-sided contacts

- S/PDIF board interface: J14, FPC/FFC 1.0mm 10-pin connector, double-sided contacts

- Optional control signals output port: J13, PH 2.0mm 4-pin connector (This is not used in most applications. It is used with some DACs, or other devices, that need these signals). The configuration is:

1	2	3	4
SILENCE	128Fs	512Fs	GND

SILENCE	Function
1	To silence the DAC
0	Normal operating

512Fs	128Fs	MCLK VS. output I2S Fs
1	1	256 * Fs
1	0	512 * Fs
0	1	128 * Fs
0	0	Reserve

- Optional MCLK input: J1, U.FL coaxial cable connector at bottom side of PCB, please keep it unpopulated except feeding MCLK from an external oscillator other than a clock board.

- Connectors reserved for future applications: J5 and J11 , please keep them un-connected

LED indicators

- Power supply indicator: D8 (GREEN) indicating DC power supply is good when lit.

- I2S input port indicators:

D9: I2S1 (GREED)	Indicating I2S1 (J2) is selected when lit
D10: I2S2 (GREED)	Indicating I2S2 (J9) is selected when lit

- FIFO status indicators:

D5 : LOCK (GREEN)	Indicating FIFO is locked with input I2S signal when lit
D6: FULL (RED)	Indicating FIFO buffer is full when lit or flashing
D7: EMPTY (RED)	Indicating FIFO buffer is empty when lit or flashing

Jumpers

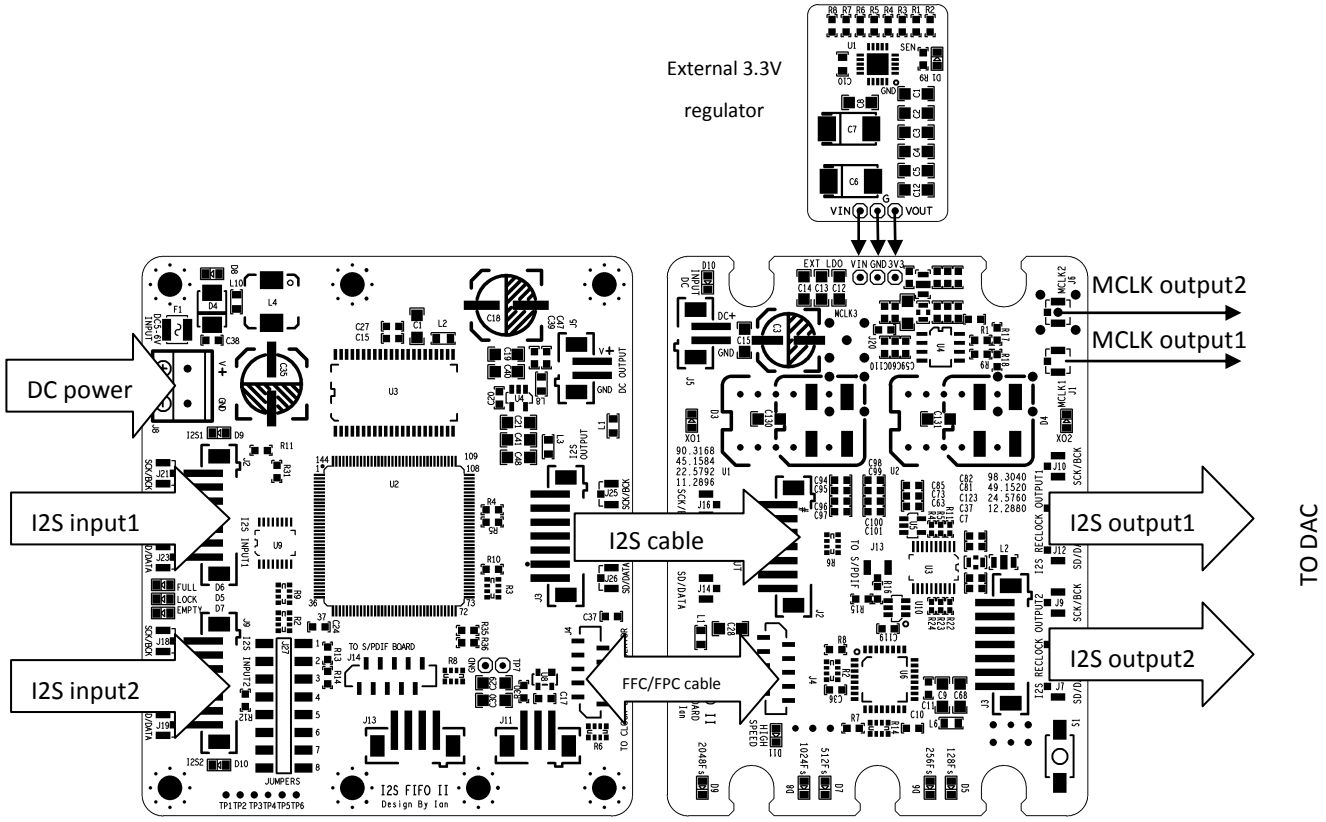
* Factory default: all jumpers are open

* Jumper settings can only be changed when power is off, except jumper1, I2S input selection.

Jumper numbers	Left PIN	Right PIN	Descriptions	Notes
1	GND	I2S input selection	Open: I2S INPUT1(J2) is selected Short: I2S INPUT2(J9) is selected	Can be connected to front panel
2	GND	I2S1 LED +	3.3V (with 200 ohm internal serial resistor) when INPUT1(J2) is selected	
3	GND	I2S2 LED +	3.3V (with 200 ohm internal serial resistor) when INPUT2(J9) is selected	
4	GND	Input format s1	S1 open, S2 open: I2S, 16 to 32bit S1 short, S2 open: Left justified, 16 to 32bit S1 open, S2 short: Right justified 16bit S1 short, S2 short: Right justified 24bit	To select of input format
5	GND	Input format s2		
6	GND	Output format	Open: I2S, 32bit Short: Left justified, 32bit	To select output format
7	GND	Default MCLK *Fs	Open: MCLK=256*Fs Short: MCLK=512*Fs	To change only when work with external oscillator if it is without a clock board
8	GND	NA	Reserved for future application	Keep un-connected

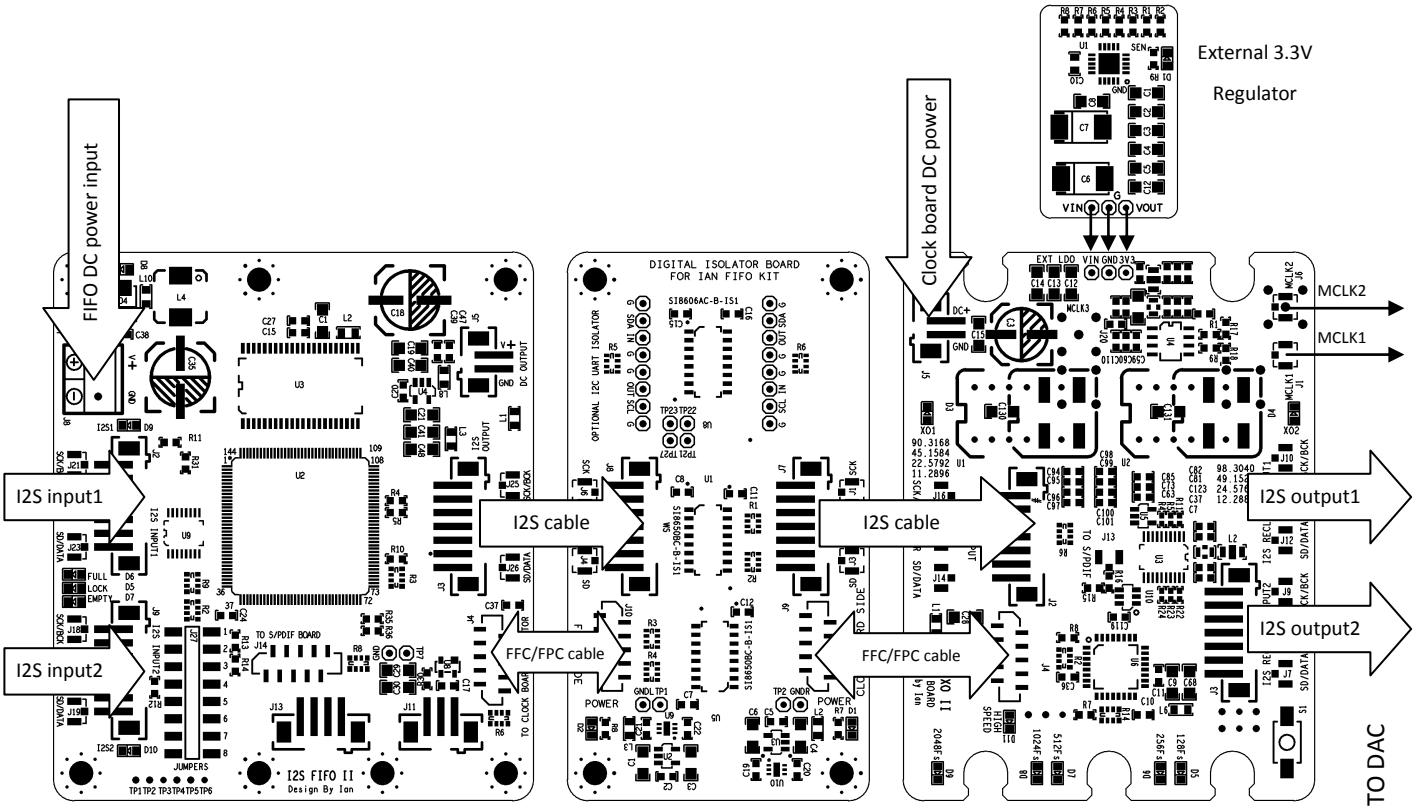
Working with a clock board

This is the most common way to run the FIFO II KIT.



Working with an isolator and a clock board

This is the recommended, “full feature” configuration.

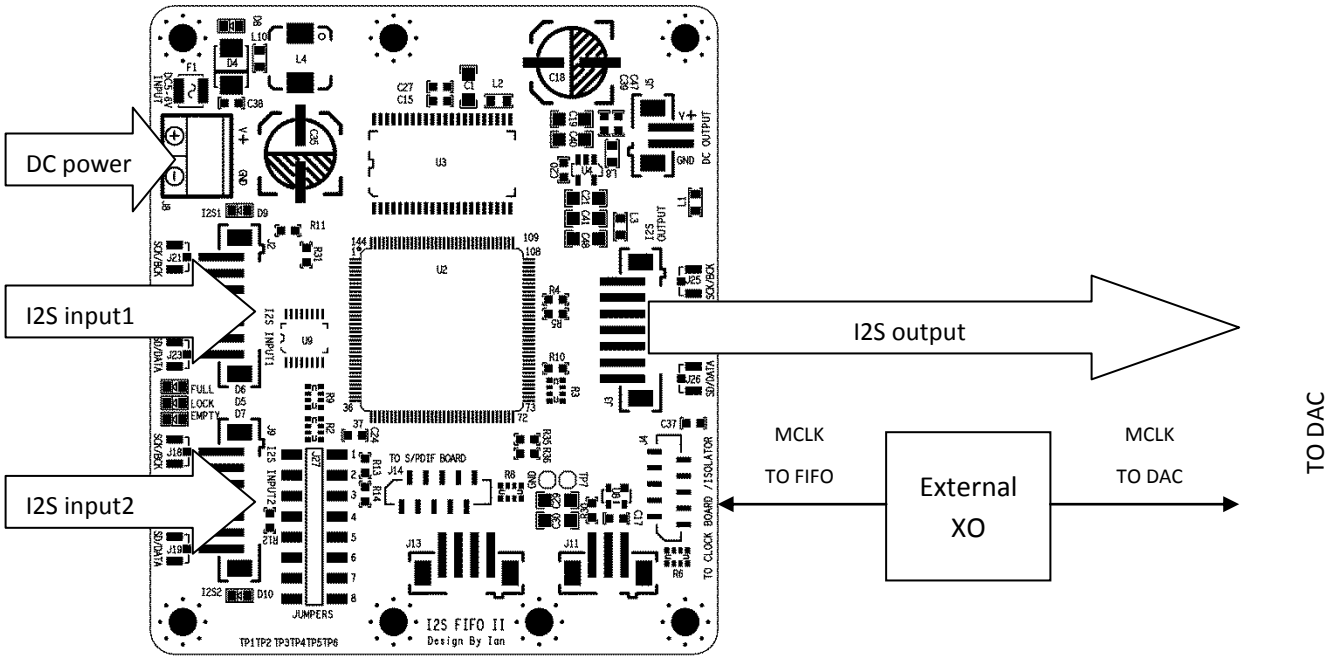


Working with external clock source

This configuration is not recommended for normal applications. It can be used to evaluate external XO in fully manual mode without a clock board involved. Automatic Fs switching feature will be disabled in this mode. Jumper7 has to be set according to digital music signal Fs and the frequency of external XO. For example, if you want to play a 88.2KHz music with a 45.1584MHz XO, you need short jumper7 to get 256*Fs as default setting.

You also need to assemble a U.FL socket to J1 at bottom side of FIFO II PCB. External clock has to be fed into FIFO II through this connector.

External clock signal must be in 3.3V logic level.



Working with S/PDIF interface board:

A S/PDIF Interface Board could be integrated with the FIFO II KIT to have the DIR and DIT function, or to set up a S/PDIF FIFO. Please refer to the user's manual of S/PDIF Interface Board for more details

Application notes and tips

- Selecting the DC power supply

The phase noise performance of the clock is very sensitive to the clock's power supply. Thus the DC power supply should be chosen with care. Low noise, high performance DC power is always preferred. A low noise shunt regulator is a good choice. Batteries are a better alternative. Both 6V lead batteries (>4AH) and 6.4V LiFeP04 batteries (>2AH) were tested with good results. Using batteries as reference is another good idea. By comparing with it, it would be very easy to know if the AC based power supply is good enough.

The DC power of FIFO II is not that significant when there is an isolator board before clock board. But in this case, the power supply of the clock board is.

Please note that, while protection circuits are included on the I2S FIFO II Board, over-voltage or reverse polarity connection may still risk damaging the board.

- Selecting the Oscillator for clock board

Low phase noise clock oscillators are essential to the best sound quality. When selecting an oscillator, parameters of both the phase noise floor and the close-in phase noise (e.g. at 100 Hz off-set) are all important. Some oscillators have very nice-looking phase noise plot, but with a couple of big spurs, try to avoid them.

Trying different clock oscillators is an interesting experience. Even clocks with the same jitter level may sound slightly different because of differences in the phase noise characteristics. Some clocks provide more detail; others sound more "musical." The modular nature of the FIFO KIT encourages you to try different solutions and choose one according to your personal preference and the style of music.

For some generic clock oscillators, the internal crystal may not be that bad. The problem is usually that generic oscillators do not have a well designed power supply and associated circuit. In many cases, if fed with a high quality, low noise power supply and interfaced with a low jitter output buffer, they will perform better than originally.

- Clock jitter and sound quality

Low jitter clock: stereo imaging is better focused on a fixed point; more detailed, more dynamic, crystal clear; the soundstage is more three-dimensional - everything can be distinguished; dark and deep background. Overall, the sound is more real.

High jitter clock: the sound seems to come from a wide area without focus; a mixed up, noisy background; difficult to distinguish different instruments; ear fatigue. Overall, it's a very "digital"sound.

- Connecting I2S input selecting function to front panel

Jumper1, 2 and 3 can be connected to front panel to achieve I2S source selecting function. Jumper 1 can be connected to an on/off switch, while jumper 2 and jumper 3 connected to two LED indicators. Each internal LED drivers has 200ohm current limitation resistor with driven voltage of 3.3V.

- Sampling clock and legacy CDs

Digital recording technology has improved dramatically since the first redbook CD was introduced decades ago. Most of the new digital music tracks were recorded with very good sampling clocks. The FIFO concept works very well with them. However, some older digital music tracks and legacy CDs, for example, disks from 1980's, were recorded with poor sampling clocks. For these older tracks and CDs, the sound quality will be very limited.

- Integrating with isolator board and clock board

MCLK of a DAC needs to be treated as analog signal. The isolator board can make the clock board as a local analog section of a DAC and galvanic isolated from all digital frontend. Ground loop can be eliminated. EMI noise introduced from ground loop is reduced.

Anti-vibration solution is also very important to a low jitter system, because of XO is based on mechanical oscillation of crystal. An anti-vibration grommet solution is highly recommended when a clock board is integrated with FIFO II.

Both the isolator board and the clock board can be stacked on top of the FIFO board to save space.

Reference

I2S bus specification: http://www.classic.nxp.com/acrobat_download2/various/I2SBUS.pdf