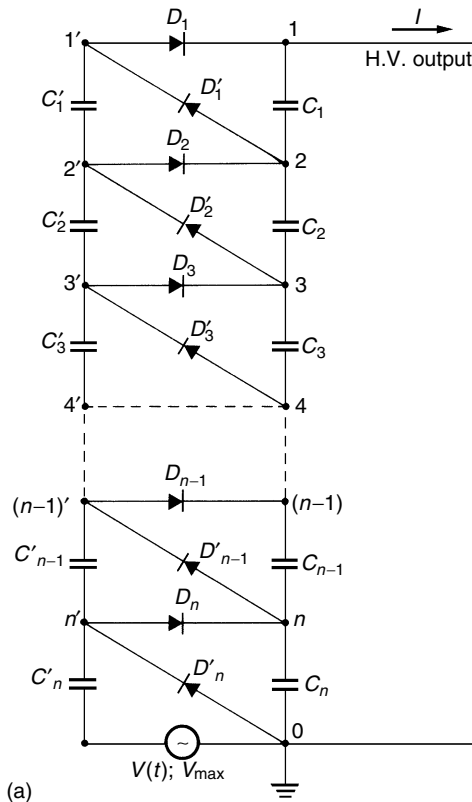
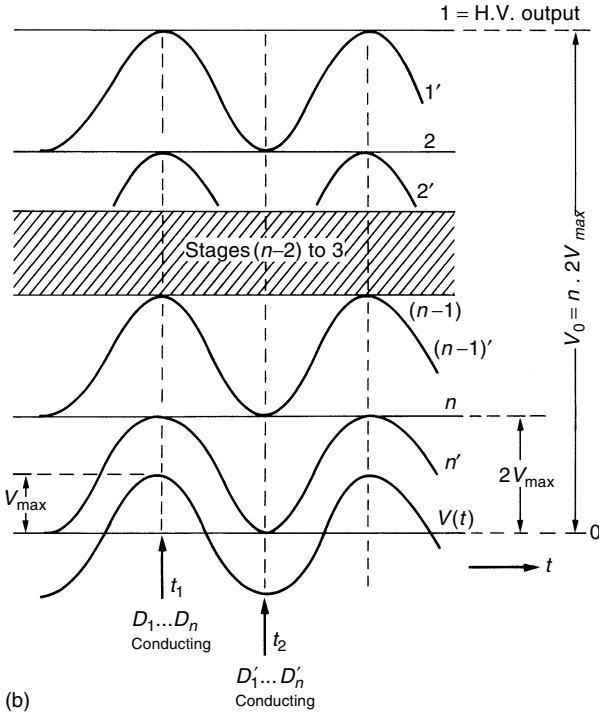


In 1920 Greinacher, a young physicist, published a circuit<sup>(6)</sup> which was improved in 1932 by Cockcroft and Walton to produce high-energy positive ions.<sup>(7)</sup> The interesting and even exciting development stages of those circuits have been discussed by Craggs and Meek.<sup>(4)</sup> To demonstrate the principle only, an  $n$ -stage single-phase cascade circuit of the 'Cockcroft–Walton type', shown in Fig. 2.3, will be presented.

*HV output open-circuited:  $I = 0$ .* The portion  $0 - n' - V(t)$  is a half-wave rectifier circuit in which  $C'_n$  charges up to a voltage of  $+V_{\max}$  if  $V(t)$  has reached the lowest potential,  $-V_{\max}$ . If  $C_n$  is still uncharged, the rectifier  $D_n$  conducts as soon as  $V(t)$  increases. As the potential of point  $n'$  swings up to  $+V_{2\max}$  during the period  $T = 1/f$ , point  $n$  attains further on a steady potential of  $+2V_{\max}$  if  $V(t)$  has reached the highest potential of  $+V_{\max}$ . The part  $n' - n - 0$  is therefore a half-wave rectifier, in which the voltage across  $D'_n$  can be assumed to be the a.c. voltage source. The current through  $D_n$  that



**Figure 2.3** (a) Cascade circuit according to Cockcroft–Walton or Greinacher. (b) Waveform of potentials at the nodes, no load



**Figure 2.3** (continued)

charged the capacitor  $C_n$  was not provided by  $D'_n$ , but from  $V(t)$  and  $C'_n$ . We assumed, therefore, that  $C'_n$  was not discharged, which is not correct. As we will take this into consideration for the loaded circuit, we can also assume that the voltage across  $C_n$  is not reduced if the potential  $n'$  oscillates between zero and  $+2V_{\max}$ . If the potential of  $n'$ , however, is zero, the capacitor  $C'_{n-1}$  is also charged to the potential of  $n$ , i.e. to a voltage of  $+2V_{\max}$ . The next voltage oscillation of  $V(t)$  from  $-V_{\max}$  to  $+V_{\max}$  will force the diode  $D_{n-1}$  to conduct, so that also  $C_{n-1}$  will be charged to a voltage of  $+2V_{\max}$ .

In Fig. 2.3(b) the steady state potentials at all nodes of the circuit are sketched for the circuit for zero load conditions. From this it can be seen, that:

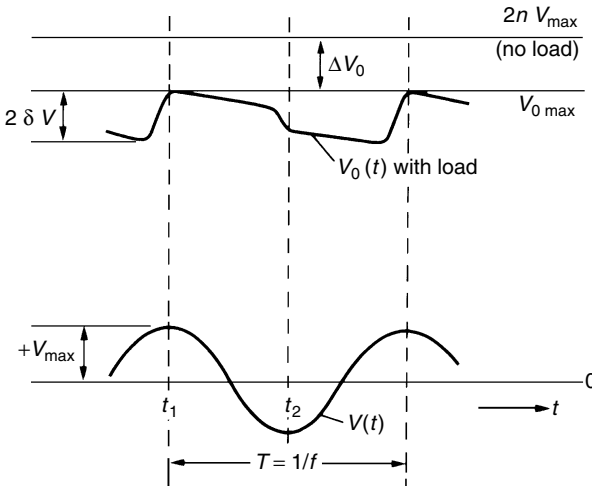
- the potentials at the nodes  $1', 2' \dots n'$  are oscillating due to the voltage oscillation of  $V(t)$ ;
- the potentials at the nodes  $1, 2 \dots n$  remain constant with reference to ground potential;
- the voltages across all capacitors are of d.c. type, the magnitude of which is  $2V_{\max}$  across each capacitor stage, except the capacitor  $C'_n$  which is stressed with  $V_{\max}$  only;

- every rectifier  $D_1, D'_1 \dots D_n, D'_n$  is stressed with  $2V_{\max}$  or twice a.c. peak voltage; and
- the h.v. output will reach a maximum voltage of  $2nV_{\max}$ .

Therefore, the use of several stages arranged in this manner enables very high voltages to be obtained. The equal stress of the elements used is very convenient and promotes a modular design of such generators. The number of stages, however, is strongly limited by the current due to any load. This can only be demonstrated by calculations, even if ideal rectifiers, capacitors and an ideal a.c. voltage source are assumed.

Finally it should be mentioned that the lowest stage  $n$  of the cascade circuit (Fig. 2.3(a)) is the Cockcroft–Walton voltage doubler. The a.c. voltage source  $V(t)$  is usually provided by an h.t. transformer, if every stage is built for high voltages, typically up to about 300 kV. This source is always symmetrically loaded, as current is withdrawn during each half-cycle ( $t_1$  and  $t_2$  in Fig. 2.3(b)). The voltage waveform does not have to be sinusoidal: every symmetrical waveform with equal positive and negative peak values will give good performance. As often high-frequency input voltages are used, this hint is worth remembering.

*H.V. output loaded:  $I > 0$ .* If the generator supplies any load current  $I$ , the output voltage will never reach the value  $2nV_{\max}$  as shown in Fig. 2.3(b). There will also be a ripple on the voltage, and therefore we have to deal with two quantities: the voltage drop  $\Delta V_0$  and the peak-to-peak ripple  $2\delta V$ . The sketch in Fig. 2.4 shows the shape of the output voltage and the definitions of



**Figure 2.4** Loaded cascade circuit, definitions of voltage drop  $\Delta V_0$  and ripple  $\delta V$

$\Delta V_0$  and  $2\delta V$ . The time instants  $t_1$  and  $t_2$  are in agreement with Fig. 2.3(b). Therefore, the peak value of  $V_o$  is reached at  $t_1$ , if  $V(t)$  was at  $+V_{\max}$  and the rectifiers  $D_1 \dots D_n$  just stopped to transfer charge to the ‘smoothing column’  $C_1 \dots C_n$ . After that the current  $I$  continuously discharges the column, interrupted by a sudden voltage drop shortly before  $t_2$ : this sudden voltage drop is due to the conduction period of the diodes  $D'_1 \dots D'_n$ , during which the ‘oscillating column’  $C'_1 \dots C'_n$  is charged.

Now let a charge  $q$  be transferred to the load per cycle, which is obviously  $q = I/f = IT$ . This charge comes from the smoothing column, the series connection of  $C_1 \dots C_n$ . If no charge would be transferred during  $T$  from this stack via  $D'_1 \dots D'_n$  to the oscillating column, the peak-to-peak ripple would merely be

$$2\delta V = IT \sum_{i=1}^n (1/C_i).$$

As, however, just before the time instant  $t_2$  every diode  $D'_1 \dots D'_n$  transfers the same charge  $q$ , and each of these charges discharges all capacitors on the smoothing column between the relevant node and ground potential, the total ripple will be

$$\delta V = \frac{1}{2f} \left( \frac{1}{C_1} + \frac{2}{C_2} + \frac{3}{C_3} + \dots + \frac{n}{C_n} \right). \quad (2.7)$$

Thus in a cascade multiplier the lowest capacitors are responsible for most ripple and it would be desirable to increase the capacitance in the lower stages. This is, however, very inconvenient for h.v. cascades, as a voltage breakdown at the load would completely overstress the smaller capacitors within the column. Therefore, equal capacitance values are usually provided, and with  $C = C_1 = C_2 \dots C_n$ , eqn (2.7) is

$$\delta V = \frac{I}{fC} \times \frac{n(n+1)}{4}. \quad (2.7a)$$

To calculate the total voltage drop  $\Delta V_0$ , we will first consider the stage  $n$ . Although the capacitor  $C'_n$  at time  $t_1$  will be charged up to the full voltage  $V_{\max}$ , if ideal rectifiers and no voltage drop within the a.c.-source are assumed, the capacitor  $C_n$  will only be charged to a voltage

$$(V_{C_n})_{\max} = 2V_{\max} - \frac{nq}{C'_n} = 2V_{\max} - \Delta V_n$$

as  $C_n$  has lost a total charge of  $(nq)$  during a full cycle before and  $C'_n$  has to replace this lost charge. At time instant  $t_2$ ,  $C_n$  transfers the charge  $q$  to  $C'_{n-1}$

equal amounts  $q$  to  $C'_{n-2}, \dots, C'_2, C'_1$  and  $q$  to the load during  $T$ . Therefore,  $C'_{n-1}$  can only be charged up to a maximum voltage of

$$\begin{aligned}(V_{C'_{n-1}})_{\max} &= \left(2V_{\max} - \frac{nq}{C'_n}\right) - \frac{nq}{C_n} \\ &= (V_{C_n})_{\max} - \frac{nq}{C_n}.\end{aligned}$$

As the capacitor  $C'_{n-1}$  will be charged up to this voltage minus  $(n-1)q/c'_{n-1}$ , etc., one can easily form the general rules for the total voltage drop at the smoothing stack  $C_1 \dots C_n$

If all the capacitors within the cascade circuit are equal or

$$C_1 = C'_1 = C_2 = C'_2 = \dots C_n = C'_n = C,$$

then the voltage drops across the individual stages are

$$\begin{aligned}\Delta V_n &= (q/c)n; \\ \Delta V_{n-1} &= (q/c)[2n + (n-1)]; \\ &\vdots \\ \Delta V_1 &= (q/c)[2n + 2(n-1) + 2(n-2) + \dots + 2 \times 2 + 1].\end{aligned}\tag{2.8}$$

By summation, and with  $q = I/f$ , we find

$$\Delta V_0 = \frac{1}{fC} \left( \frac{2n^3}{3} + \frac{n^2}{2} - \frac{n}{6} \right).\tag{2.9}$$

Thus the lowest capacitors are most responsible for the total  $\Delta V_0$  as is the case of the ripple, eqn (2.7). However, only a doubling of  $C'_n$  is convenient, since this capacitor has to withstand only half the voltage of the other capacitors; namely  $V_{\max}$ . Therefore,  $\Delta V_n$  decreases by an amount of  $0.5nq/c$ , which reduces  $\Delta V$  of every stage by the same amount, thus  $n$  times. Hence,

$$\Delta V_0 = \frac{1}{fC} \left( \frac{2n^3}{3} - \frac{n}{6} \right).\tag{2.10}$$

For this case and  $n \geq 4$  we may neglect the linear term and therefore approximate the maximum output voltage by

$$V_{0\max} \cong 2nV_{\max} - \frac{I}{fC} \times \frac{2n^3}{3}.\tag{2.11}$$

For a given number of stages, this maximum voltage or also the mean value  $V_0 = (V_{0\max} - \delta V)$  will decrease linearly with the load current  $I$  at constant

frequency, which is obvious. For a given load, however,  $V_0$  may rise initially with the number of stages  $n$ , but reaches an optimum value and even decreases if  $n$  is too large. Thus – with respect to constant values of  $I$ ,  $V_{\max}$ ,  $f$  and  $C$  – the highest value can be reached with the ‘optimum’ number of stages, obtained by differentiating eqn (2.11) with respect to  $n$ . Then

$$n_{\text{opt}} = \sqrt{\frac{V_{\max} f C}{I}} \quad (2.12)$$

For a generator with  $V_{\max} = 100 \text{ kV}$ ,  $f = 500 \text{ Hz}$ ,  $C = 7 \mu\text{F}$  and  $I = 500 \text{ mA}$ ,  $n_{\text{opt}} = 10$ . It is, however, not desirable to use the optimum number of stages, as then  $V_{0\max}$  is reduced to 2/3 of its maximum value ( $2nV_{\max}$ ). Also the voltage variations for varying loads will increase too much.

The application of this circuit to high power output, which means high products of  $IV_0$  is also limited by eqns (2.9) and (2.11), in which again the large influence of the product  $fC$  can be seen. An increase of supply frequency is in general more economical than an increase of the capacitance values; small values of  $C$  also provide a d.c. supply with limited stored energy, which might be an essential design factor, i.e. for breakdown investigations on insulating materials. A further advantage is related to regulation systems, which are always necessary if a stable and constant output voltage  $V_0$  is required. Regulation can be achieved by a measurement of  $V_0$  with suitable voltage dividers (see Chapter 3, section 3.6.4) within a closed-loop regulation system, which controls the a.c. supply voltage  $V(t)$ . For fast response, high supply frequencies and small stored energy are prerequisites.

For tall constructions in the MV range, the circuit of Fig. 2.3(a) does not comprise all circuit elements which are influencing the real working conditions. There are not only the impedances of the diodes and the supply transformer which have to be taken into consideration; stray capacitances between the two capacitor columns and capacitor elements to ground form a much more complex network. There are also improved circuits available by adding one or two additional ‘oscillating’ columns which charge the same smoothing stack. This additional column can be fed by phase-shifted a.c. voltages, by which the ripple and voltage drop can further be reduced. For more details see reference 8.

Cascade generators of Cockcroft–Walton type are used and manufactured today worldwide. More information about possible constructions can be found in the literature<sup>(9,10)</sup> or in company brochures. The d.c. voltages produced with this circuit may range from some 10 kV up to more than 2 MV, with current ratings from some 10  $\mu\text{A}$  up to some 100 mA. Supply frequencies of 50/60 Hz are heavily limiting the efficiency, and therefore higher frequencies up to about 1000 Hz (produced by single-phase alternators) or some 10 kHz (produced by electronic circuits) are dominating.