

Fig. 11. Differential-to-single-ended converter.

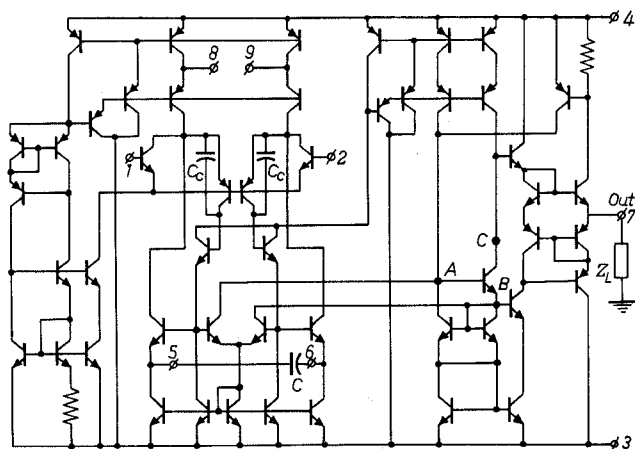


Fig. 12. Complete operational amplifier.

stabilization factor for supply-voltage variations was measured and a value of $1/I \cdot \partial I / \partial V_B = 1$ percent/V can easily be attained. I is the current of the stabilizer and V_B is the supply voltage.

Complete Operational Amplifier

The whole amplifier circuit is shown in Fig. 12. Offset control is carried out by controlling the difference between the collector currents of the input transistors (points 8 and 9).

The output stage is short-circuit protected for negative output voltages by the well-defined current gain of the lateral p-n-p transistors and for positive input voltages by measuring the collector current of the output transistor (lateral p-n-p transistor the collector of which is connected to point A in Fig. 12). Only one external capacitor is needed to shape the amplifier frequency response. The feedback capacitors C_C are MOS capacitors of about 3 pF. The chip size is 1.1×1.6 mm.

Amplifier Data: Supply voltage: ± 4 to ± 15 V; open-loop gain: $3 \cdot 10^5$ typical; unity gain bandwidth: 50 MHz; maximum slew rate: 50 V/ μ s at gain of 10; input bias current: 10 nA; CMRR: 100 dB; frequency compensation with one capacitor: 1000 pF; and output current: 15 mA, short-circuit proof.

In conclusion we may say that it is possible, using controlled current gain transistors, to construct a high-performance amplifier comprising a minimum of resistors and with a small chip size.

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A High-Voltage Monolithic Operational Amplifier

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Abstract—An operational amplifier capable of operating with power supplies up to ± 40 V is discussed. The device exhibits output voltage and input common-mode swings to within a few volts of either power supply has an input offset current of 1 nA, a slew rate of 2 V/ μ s, and is internally compensated. This paper describes special circuit and device techniques used to reliably fabricate this amplifier with essentially standard monolithic diffused technology.

INTRODUCTION

THERE ARE a number of applications, especially in airborne military systems, in which an operational amplifier with large output voltage swing and common-mode input voltage range are needed. The monolithic operational amplifier described in this paper has an output voltage swing of ± 32 V and a common-mode range of ± 34 V when operated on ± 36 -V supplies. These ratings are approximately twice those of previous

monolithic operational amplifiers. In addition, the amplifier exhibits an input offset current of 1 nA and a slew rate of 2 V/ μ s, characteristics equal to those of the better diffused monolithic amplifiers available today.

BASIC AMPLIFIER CONFIGURATION

A major consideration in choosing the basic configuration for an operational amplifier includes the simultaneous realization of both high open-loop gain and wide bandwidth. Possible approaches to the amplifier are illustrated in Fig. 1(a) and (b), which are single-ended analogs of three- and two-stage complementary common-emitter cascades. The three-stage circuit is useful to achieve the high desired gain but has the disadvantage of requiring fairly complex and critical frequency-compensation networks as shown. The two-stage circuit produces sufficient gain (about 500 000) due to the use of the common-base (CB) first-stage output device, the current-source interstage load, and the common-collector (CC) second-stage input device; and it is easily frequency compensated. The compensation is provided by a single small-valued "pole-splitting" capacitor [1], which is easily fabricated in integrated form and provides nearly ideal open-loop characteristics.

Fig. 2 shows a differential analog of the two-stage amplifier in Fig. 1(b), which provides the small voltage offset and drift needed in an operational amplifier, but otherwise has the same characteristics as Fig. 1(b). A simplification of Fig. 2 is shown in Fig. 3, which employs a "differential-to-single-ended" conversion circuit¹ and requires only one compensation capacitor. This is the basic circuit from which the high-voltage operational amplifier is developed.

EXTENSION OF AMPLIFIER BREAKDOWN VOLTAGE

The supply-voltage limitation of most monolithic operational amplifiers results primarily from the low common-emitter breakdown voltage BV_{CEO} (approximately 40–60 V) of monolithic n-p-n transistors, which in turn results from present difficulties in fabricating epitaxial collector material with resistivities greater than 3–5 Ω -cm. The p-n-p transistors rarely cause difficulty because they can be designed to have BV_{CEO} breakdowns equal approximately to BV_{CBO} of the n-p-n devices, which is normally greater than 90 V. The collector I - V characteristic of a representative monolithic n-p-n transistor is shown in Fig. 4. The detailed breakdown mechanism is poorly understood, but is explained in terms of avalanche multiplication of leakage current in the collector-base junction [2], and can be characterized by $BV_{CEO} = BV_{CBO}/(\beta_{dc})^{1/n}$, where the empirical value of n is about 6 for silicon transistors.

A reduction in base-emitter resistance R_B shunts avalanche current away from the base and gives a higher

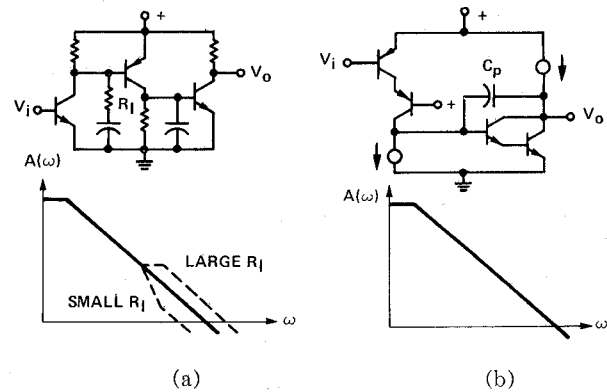


Fig. 1. (a) Single-ended analog of three-stage operational amplifier and open-loop response for various choice of R_1 . The dashed curves are undesirable since they lead to either long settling time (large R_1) or overshoot (small R_1). (b) Analog of two-stage amplifier employing pole-splitting compensation. The single small-valued capacitor produces a nearly ideal open-loop response.

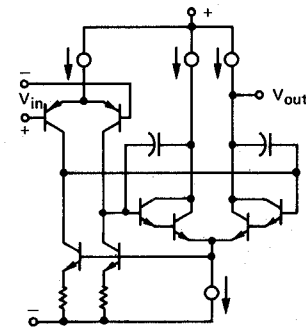


Fig. 2. Differential analog of the circuit in Fig. 1(b).

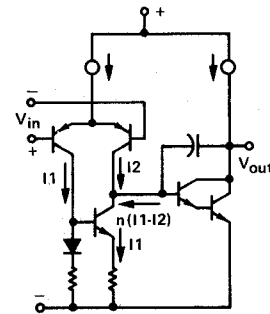


Fig. 3. Circuit equivalent to Fig. 2 employing differential-to-single-ended conversion circuitry.

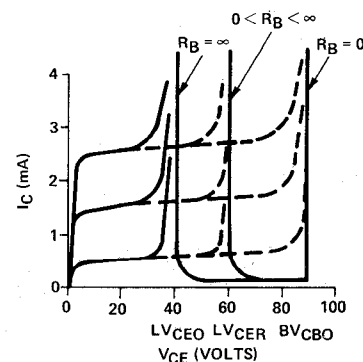


Fig. 4. Common emitter V - I characteristics shown for different base resistors R_B with $R_B = 0$.

¹ To the authors' knowledge the circuit was first used in 1966 by J. E. Thompson of Motorola Semiconductor.

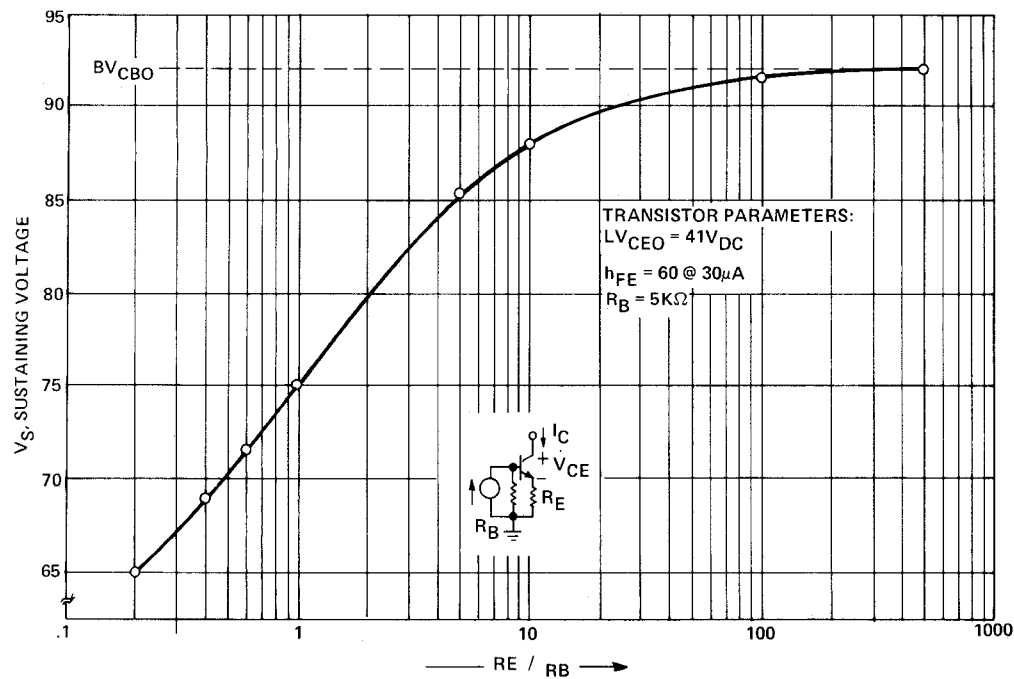


Fig. 5. Measured values of sustaining voltage as a function of R_E and R_B .

value of sustaining voltage, the limiting safe operating voltage in the active region. An increase in sustaining voltage can also be obtained by adding a resistor in the emitter lead since this reduces the sensitivity of the transistor to base-accepted leakage current. Fig. 5 shows the breakdown improvement that is possible from increased emitter resistance R_E as a function of base resistance R_B . Breakdown improvement is seen to be possible for large values of source resistance R_B by the addition of an emitter resistor R_E of value $R_E > R_B$.

CIRCUIT APPROACHES TO BREAKDOWN IMPROVEMENT

From the discussion above it is seen that the conventional breakdown limitation can be avoided if one operates all amplifier transistors in a mode such that $R_E > R_B$, which is essentially equivalent to using the transistors in a common base mode. The amplifier will then stand off approximately BV_{CBO} rather than LV_{CEO} .

Fig. 6 shows a basic monolithic amplifier derived from Fig. 3, which is designed to have low input current and high slew rate [3]. This circuit employs super-gain input transistors, first-stage transconductance reduction to improve slew rate, and internal compensation. However, it does suffer from the LV_{CEO} breakdown limitation since several of the n-p-n transistors operate with an essentially open base.

This circuit can be converted to a high-breakdown equivalent by using the modifications shown in Figs. 7 and 8, i.e., each common-emitter (CE) stage is replaced by a common-emitter common-base (CB) cascade and each common-collector (CC) stage is replaced by a CC-CB stack. CB stages need no modification. As will be shown below, such a conversion is reasonably straight-

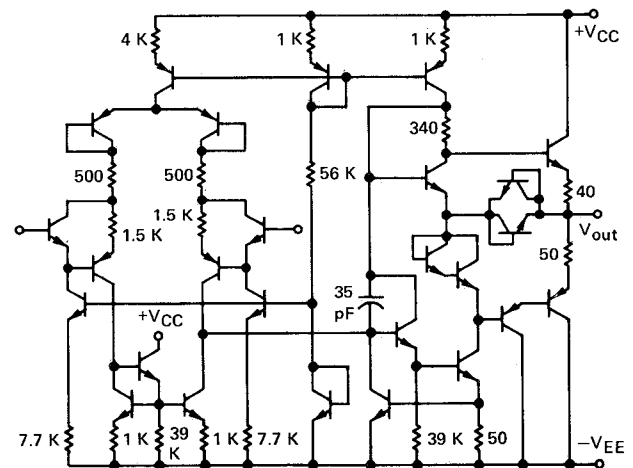


Fig. 6. Monolithic amplifier (Motorola MC-1556) derived from the circuit in Fig. 3.

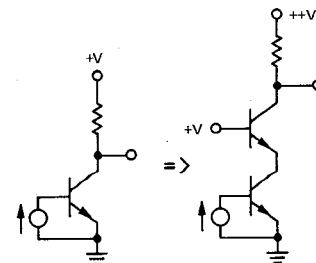


Fig. 7. Conversion of CE stage to CE-CB for high breakdown.

forward, except for two difficulties. During turn-on of the amplifier, and during input or output fault conditions, the transistors may transiently be in an LV_{CEO} condition resulting in burnout. Care must be taken to avoid this. Also a new device difficulty can arise in the integrated

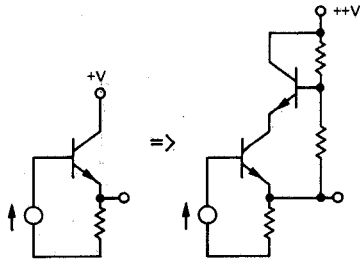


Fig. 8. Conversion of CC stage to CC-CB stack for high voltage.

circuit. MOS channels can easily form at the high voltages and these can cause malfunction of the circuit. The latter problem is discussed in the next section.

PREVENTION OF PARASITIC MOS CHANNEL CURRENTS IN THE HIGH-VOLTAGE DIFFUSED IC

Fig. 9 shows a possible p-channel MOS transistor that is formed from the aluminum interconnect metal (gate) and two p regions (drain and source) that can be diffused resistors or channel-diffused regions in the high-voltage junction isolated IC. Two types of channels most commonly occur.

1) A channel can form between two p resistors if metal overlays both resistors and if the metal has a negative bias with respect to either of the resistors.

2) A resistor-to-substrate channel can also form if metal crosses from resistor to isolation and if the metal is negative with respect to the resistor. In the normal integrated circuit, no other channels are likely to form because the usual bias conditions inhibit MOS action.

The magnitude of the gate (overlying circuit metal) to source (p resistor) voltage required for a channel to occur V_{GS_T} is given by (see Fig. 9 and [4])

$$V_{GS} > V_T + K\sqrt{V_{epi-s}}$$

where V_T typically varies from 5 to 15 V depending upon n-region epitaxial resistivity, crystal orientation, oxide thickness, and surface conditions; K is in the vicinity of 1.2 for 2 Ω -cm epi, and the presence of V_{epi-s} represents an injection requirement that must be overcome before current can flow. The important thing to note from the above equation is that, if the gate-to-source voltage V_{GS} is greater than some threshold voltage (typically 10–25 V), channeling between p regions will occur. The nature of the channel current is illustrated in Fig. 10. It is seen that no current flows until the threshold voltage is exceeded and then the current is approximately proportional to the square of the applied voltage.

There are two primary ways to eliminate the fault currents. These are listed in order of preferred usage as follows.

1) In circuit layout, metal runs that cross over resistors or run from resistor to substrate and that are negative with respect to any of the p regions over which they cross should be avoided.

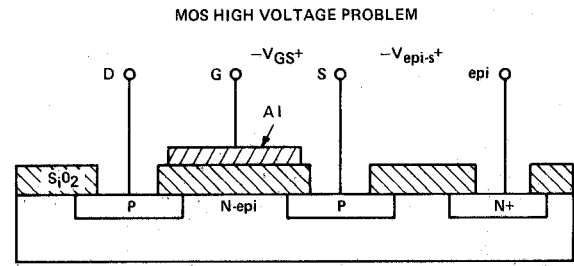
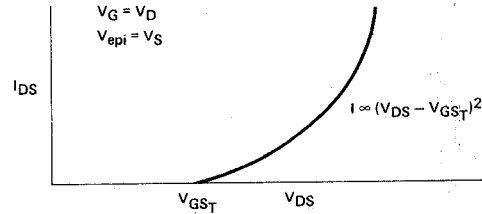

 Fig. 9. MOS device formed by two adjacent resistors and overlying metal. Note that drain D is assumed negative with respect to source S .


Fig. 10. Typical channel current for device in Fig. 9.

2) If metal crossovers, which might cause channeling cannot be avoided, n^+ regions must be diffused between the p regions where the metal crosses over to prevent channel formation.

The theory above indicates that channels from the n-p-n transistor base-to-substrate, lateral p-n-p collector-to-substrate, or substrate p-n-p emitter-to-substrate will not form. The reason for this is simply that the normal metalization of these devices always guarantees that the gate-to-source potential is below threshold. There are other devices or layout conditions not listed that can produce channeling, so the layout must be checked to be sure that a negative gate-to-source condition does not exist under any operating circuit conditions.

HIGH-VOLTAGE CIRCUIT

The diagram for the final high-voltage operational amplifier is shown in Fig. 11. This circuit incorporates all of the ideas discussed above; CE stages are replaced by CE-CB cascades and the CC output n-p-n transistor is replaced by a CC-CB stack. The p-n-p transistors are not modified since they are high breakdown devices. MOS parasitics are eliminated by routing metal runs so that negatively biased metal never crosses a positively biased p region. It was possible to satisfy this requirement for arbitrary power-supply sequencing and arbitrary input overvoltage, as well as for normal operating modes. Fig. 12 is a photomicrograph of the high-voltage circuit.

The amplifier generally has the same small-signal characteristics as the MC-1556 (see Fig. 6 and [3]). The input transistors are super-gain devices that exhibit a typical β of 3000 and have a BV_{CEO} of about 4 V. They are operated in circuitry that clamps the collector-base voltage to less than 0.15 V, regardless of supply or input

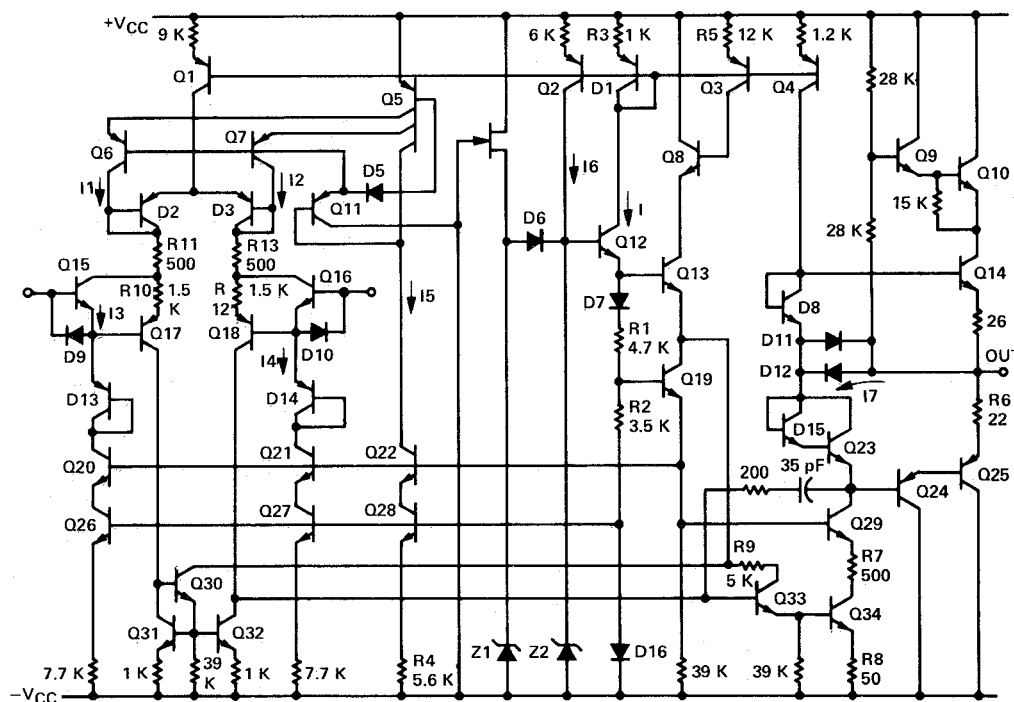


Fig. 11. Complete monolithic high-voltage amplifier developed from Fig. 6.

voltage. Reasonably high slew rate is obtained by employing emitter resistance in the first stage and increasing the stage operating current (to about $50 \mu\text{A}$) so that a low ratio of gm/I_1 is obtained. It is shown in [3] that, other than technology improvements, gm/I_1 reduction is the only approach available for speed improvement.

SPECIAL CIRCUIT MEASURES FOR HIGH-VOLTAGE OPERATION

Due to the potential dissipation problem in the amplifier, it is desirable to prevent the biasing currents from increasing with supply voltage. This is accomplished by using an internal regulator that develops a constant reference current I from which all bias currents and voltages in the circuit are established. The JFET Z_1 and D_6 (Fig. 11) comprise the start circuit for the regulator. At turn-on, the JFET furnishes a small current to the base of Q_{12} , which causes the reference current to be established. The diode D_6 then becomes zero biased decoupling the poorly predictable JFET from the reference circuit and preventing power-supply ripple from entering the main reference Z_2 .

When opamps are used in a comparator application, large differential input voltages often exist. In such an application, breakdown would normally occur in the base-emitter junctions of the input n-p-n transistors. This is prevented by using high breakdown diodes D_2 and D_3 in series with the input transistor base-emitter junctions. The current sources I_1 and I_2 bypass D_2 and D_3 preventing the input n-p-n transistors from saturating under this condition. These current sources (I_1 and I_2) are designed to track with the current sources I_3 and I_4 to assure that the input-stage operating point is always correct.

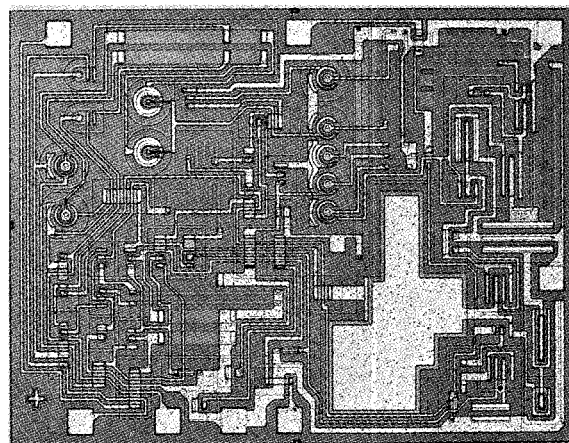


Fig. 12. Photomicrograph of high-voltage operational amplifier die. Dimensions are 70×91 mils.

If the collector of the biasing transistor Q_{13} were directly connected to the positive supply line, omitting Q_8 , Q_3 , and R_5 from the circuit, a startup destruction mode could occur. This is possible since the impedance seen by the base of Q_{13} , before the current I is established, is high and Q_{13} is therefore in a BV_{CEO} mode at turn-on. Application of a large supply voltage would cause the destructive breakdown of Q_{13} and then Q_{33} and Q_{34} . The transistor Q_8 prevents this by sharing part of the turn-on voltage until the bias current I is established.

The negative short-circuit current limit occurs when the voltage drop across R_6 turns on D_{12} and a current I_7 flows from the output through D_{12} , the Darlington D_{15} and Q_{23} , Q_{29} , R_7 , Q_{34} , and R_8 . The circuit is designed to deprive Q_{24} of additional drive current during this current-limit mode. In the circuit of Fig. 6 (MC-1556) the analogous current was limited to 14 mA by using an

n-p-n transistor to monitor the emitter current of Q_{34} and to limit the drive current to Q_{33} during the short circuit. In the new circuit, Q_{34} saturates when increased current flows in R_7 and then Q_{29} becomes a constant current source that accepts only 2 mA. The lower limiting current is more desirable since it reduces dissipation.

There is a possibility that the inputs to an opamp will be subjected to large rapidly changing voltages. The slew-rate limitation at the emitters of the input transistors can cause these devices to experience a transient emitter-base breakdown when such an input is applied, and this could produce a long-term degradation of the input super- β transistor characteristics. This mode is avoided by the addition of diodes D_9 and D_{10} that shunt the input emitter-base junctions under reverse bias.

Consideration must also be given to abnormal conditions imposed on the device. For instance, if the resistors R_{10} – R_{13} were placed in an n island tied to the positive supply and the positive supply were removed during operation of the device, a parasitic substrate p-n-p (with the resistors acting as emitters) would be turned on causing large destructive currents to flow into the amplifier. This is avoided by tying the resistor islands to bias points other than the supplies.

SUMMARY OF CHARACTERISTICS

The amplifier typically exhibits an open-loop voltage gain of 500 000, has an input bias current and offset current of 8 and 1 nA, respectively, a voltage offset of 3 mV and an offset drift of $8 \mu\text{V}/^\circ\text{C}$. The 40-V peak-to-peak power bandwidth is 18 kHz, the small-signal bandwidth is 1 MHz, and the unity-gain voltage-follower phase margin is 65° . The amplifier is well behaved while slewing and is quite stable under all feedback conditions. One can arbitrarily sequence the power supplies, apply input overvoltage, or output short circuit without damaging the device. Finally, the performance characteristics remain essentially unchanged over a power-supply range of ± 5 to ± 40 V.

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A Computer-Aided Evaluation of the 741 Amplifier

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Abstract—Although the basic operation of modern IC opamps is well understood, no detailed evaluation has been published concerning the characteristics of the transistors and the performance limitations resulting from the devices and the individual stages of the amplifier. In this paper, the results are given of an investigation of a typical example of the 741-type IC amplifier. Complete data are given on the transistor characteristics and parameters. Computer simulation is used to study the performance and limitations of the stages and the overall amplifier.

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I. INTRODUCTION

THE 741-type amplifier is representative of many presently available and widely used integrated-circuit operational amplifiers (IC opamps) [1], [2]. Certainly, subsequent improvements in the design have been made with respect to input current levels [3], large-signal slew rate [4], and low quiescent power [5]. Nonetheless, the 741 exhibits many of the design decisions, opportunities, and problems that are typical of general-purpose IC opamps [6]. Although the basic operation of this type of IC is well established, no detailed evaluation has been published relating the performance limitations to the various devices and stages. In addition, no detailed information is generally available on the typical characteristics and parameters of the devices in this type of IC. In this paper, such an evaluation is made for a representative example of the 741 amplifier. The results are based