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HIGH VOLTAGE PRINTED CIRCUIT DESIGN & MANUFACTURING NOTEBOOK

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Table of Contents

		Page
	Forward	3
Chapter 1	Overview of High Voltage Printed Circuits	4
Chapter 2	Manufacturing of High Voltage Printed Circuits	5
Chapter 3	Design of High Voltage Printed Circuits	7
Chapter 4	High Voltage Multilayer Design	16
Chapter 5	High Voltage on Heavy Copper Circuits	17
Chapter 6	Material Specifications	19
Chapter 7	Survivability	22
Chapter 8	Planar Transformers	24
Chapter 9	Testing High Voltage Boards	27
Chapter 10	Assembly Considerations	31
Chapter 11	Outer Space Boards	34

The information in this book is current to November 2004. As material specifications and manufacturing practices change and evolve, please ensure you are using up to date information.

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Written by Robert Tarzwell
Additional notes by Ken Bala

Foreword

With potentials as high as 40 000 Volts, an engineer now has the ability to design one printed circuit that can carry large voltages and support the fine traces and features of the computer circuits needed to drive the high voltage. The high voltage circuits of today can contain from 1 to 40 layers. I had to learn using the good old fashion trial and error method. New and different ways of manipulating the same materials were required without the help of large databases of information from which to draw from. Many experiments were successful and some failed. These experiments allowed me to keep a detailed diary of high voltage design ideas. I have also included a chapter on the different methods used to manufactured high voltage circuits.

Robert Tarzwell, November 2002.

Chapter 1

Overview of High Voltage Printed Circuit Design

A few years ago, the notion that a printed circuit board could effectively handle a large voltage in excess of 40,000 Volts was unheard of. Today that reality not only exists, but also is orbiting the earth, imaging through our bodies and controlling our power grid. Through years of research and experiments, I slowly developed and improved the high voltage copper printed circuit board. In 1998, my company was contacted to develop a high voltage board for a critical space operation. Through countless experiments, I developed a system, which could offer totally encapsulated, very high dielectric multilayer circuits. I developed High Voltage Polyimide Film (HVPF), a very special printed circuit material that has a dielectric breakdown of over 3000 V/mil. It can be used as a stand alone thin material or be inserted into FR4 material boards to enhance the voltage characteristics.

A new exciting product emerged. And I ran out to tell the world. Success was quick to follow. Quotes came in and new methods were developed in the lab creating such exotic circuits as high voltage planar multilayers, bendable high voltage circuits and high voltage flexible circuits. The result was an engineering system designed to handle just about any high voltage situation imaginable.

The basic underlying principle is the ability to carry very high voltage with a thin layer of HVPF material. Yes, the cost is higher but so is the savings in other areas of the project. What was previously mechanically attached off the circuit board through special insulated wire, terminal blocks and potted black boxes, could now be located on the high voltage circuit board.

For outer space and high altitude airplanes, printed circuits designers must realize that low atmospheric pressure lowers the arc over voltage and allows easier corona production. Outer space printed circuits must not outgas in the vacuum or it will contaminate other critical components of the spacecraft. Through my research I have found procedures to lower such outgassing in the printed circuit materials.

In some cases, printed circuits which I manufactured for companies were suspected of being faulty when a high voltage board would function for only a short period of time and then self destruct. After a serious study of the effects of corona it was determined that, this near silent force could quickly destroy any organic materials ability to insulate. The effects of corona through ionization and particle bombardment of the epoxy will cause the epoxy to become carbonized and conduct electricity.

Chapter 2

Manufacturing of High Voltage Printed Circuits

The manufacturing process used in high voltage circuits is essentially the same steps as a normal printed circuit. There are however, differences in the material used and the properties of those materials. When a low voltage printed circuit meaning, 5 to 600 Volts, is designed and manufactured it is more about spacing and circuit design than material, as all printed circuit materials can support up to 1000 Volts.

Medium voltage boards of typically 600 to 3000 Volts require greater care in selecting the base material and the subsequent processing as this voltage can easily support arcs and corona.

High voltage boards of 3000 Volts to a maximum limit of about 100kVolts are limited to HVPF, Teflon and in some cases BT epoxy with serious effort and testing in areas of corona, field strengths and temperature control.

Typically, the circuit is designed on a CAD system and the files e-mailed to the board fabricator. They are preferred in Gerber 274x format. The manufacture steps and repeats the circuits to fit on a large panel of 24 by 18 inches, and adds borders and other details at this time. The data is plotted onto 7 mil clear Mylar and used as either the master from which copies are made, or on short runs, shot directly on the board. The material is cut to size and drilled on large CNC drilling machines with the desired hole pattern. The panel is then deburred and cleaned of any release residue from manufacturing. To provide an imangible surface, the printed circuit material is coated with a photosensitive plastic coating. The area that is exposed through the film is hardened by the powerful ultraviolet light. A subsequent developing stage with a mild alkaline solution removes the unhardened dry film. For direct etching, single sided or non-plated double sided boards, an etching type resist is used and a direct pattern exposing the areas to be etched away is exposed on the base material. For plated through hole boards, the holes are metalized either with carbon or reduced copper solutions. After the holes are metalized, the plating type dry film is laminated on and exposed to create bare copper traces and pads. The board is then plated with 1.5 mils of copper on the exposed traces and in the holes. To prevent etcher fluid from harming the traces and holes, a coating of tin/lead or tin only is then plated on the tracks and in the holes. The plating dry film is then stripped off in a mild caustic solution and the unwanted base copper is etched off in an ammonia solution. The basic shape of the tracks and vias is now visible. The tin is now stripped off in nitric solution and the board cleaned. Solder mask is applied and a coating of tin/lead (solder) applied with a hot oil leveling machining. White marking and final routing to shape is done. The board is inspected, wrapped and shipped.

For multilayers, the internal layers are imaged and etched as in a single sided board. They are laminated together with core material using uncured prepreg material. The cores provide the support and insulation between the copper trace layers. After pressing in a 100 ton hydraulic machine, the laminated board is processed like a double-sided board.

For high voltage boards special attention must be paid to the material and its specifications. Careful design of the inner layer construction with high resin percentage prepreg will ensure a void free press package. Typically a printed circuit manufacturer would use 7628 prepreg, a low cost, high volume type material. It is also a low resin, high glass content prepreg with large glass bundles.

High voltage boards require prepregs such as 1080 or 2113 that feature small glass styles for better penetration of the resin. A larger percentage of resin content and a thinner overall thickness will help prevent micro bubbles and improve the density in multiple layers. Construction of this method will slightly increase the cost, but the extra protection for high voltage overcomes this disadvantage.

To further improve the out gassing of the finished board, a long slow bake at 260°F for 20 hours will remove any remain volatiles and drive off any moisture. Both important to good high voltage longevity.

For boards that must operate at low atmospheric pressures, an additional bake of 300°F for 4 to 6 hours will further decrease the outgassing created by a vacuum

Chapter 3

Design of High Voltage Printed Circuit Boards

The design of high voltage circuits is one of proper material specifications and separating clearances.

The destruction of high voltage printed circuit boards is from two sources, direct arc over and corona production. Direct arc over occurs when the voltage potential exceeds the dielectric's ability to withstand it. Corona discharge is a predominant failure mechanism in high voltage circuits because it causes degradation of the insulation system. Corona is produced when the electric discharges only involve a portion of the dielectric between two electrodes rather than bridging the electrodes. There is probably a short period of corona before a direct arc over. In corona fields the gas molecules are ionized by the impact of the electrons. The liberated electrons gain speed in the electric field, ionizing more atoms through impact; therefore an avalanche of electrons is formed. The field strength drives the electrons towards the electrodes, therefore creating a passage of current through the insulation system.

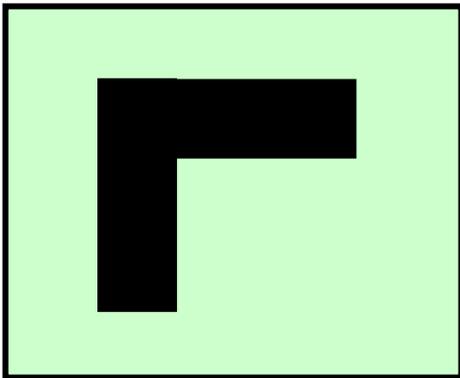


Figure 1: Bad corner design

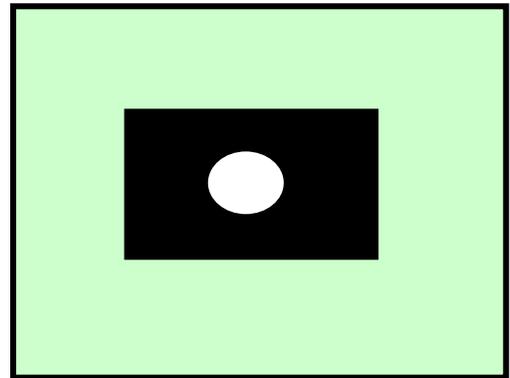


Figure 2: Bad pad design

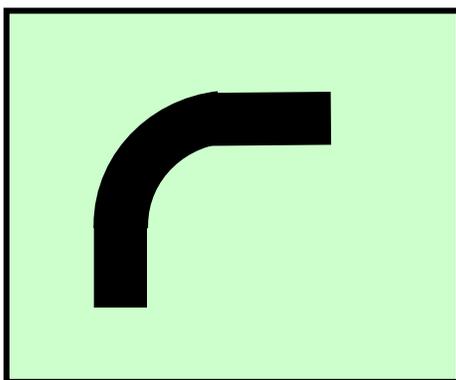


Figure 3: Good corner design

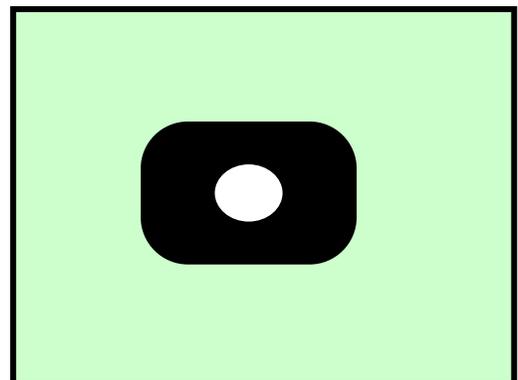


Figure 4: Good pad design

Both the arcing and corona are reduced or eliminated by smooth round curves and control of the field strength through out the design phase. In a printed circuit board we are dealing with a flat conductor, with some triangulated shape to the sidewall. We can do little with the shape of the sidewall and the corresponding sharp edge at the top and bottom, but we can design the traces to lower the potential for corona or arc over. All sharp edges must be avoided. Use round corners instead of 90-degree turns. Pads should have round corners, with as large a radius as possible. Both arc over and corona can be produced in the laminate as well as the air surrounding the traces.

A sharp needlepoint will direct arc over at 1/3 the voltage of a rounded sphere. Example: for a 15 KV circuit, a 25 cm sphere will arc over at a spacing of .42, whereas a 2.5 cm sphere arc over value is only increased to .48 cm, a sharp needlepoint will need 1.3 cm spacing. At the constant spacing of .42 cm a needle will arc at 5 KV, a sphere at 15 KV. The sharp needlepoint will also generate corona three times easier. The starting point for corona is about 30 KV/cm of radius. Other factors of concern for spacing and circuit design are the atmospheric pressure and humidity in which the circuit must operate. When calculating the effect of atmospheric pressure Paschen's law states the breakdown voltage is a function of pressure/distance. If you half the pressure and double the distance the breakdown voltage would remain the same. The surface condition also affects the spacing for direct arc over and corona production. The small bumps and particles on a conductor's surface create small areas of higher field stress within the high voltage area. Using a new, washed and polished surface as a reference point, a scratched or dirty surface will arc over at .7 to .8 percent of that reference voltage.

To approximately calculate the spacing requirement of two rounded smooth surfaces with a low frequency or DC high voltage potential, use the formula $d = KV/30$ where d =distance in cm. For needle or sharp points use $d= KV/85$. For AC high frequency, use a 1.12 times factor as it will arc over easier.

Temperature affects the distance of arc over between two points, as the temperature of metal increases, more electrons are forced off the surface. These extra electrons will add to a negative potential and subtract from a positively charged conductor. A prime example is a spark plug, the center electrode runs near red hot, this heat expels large amounts of electrons, which assists the negative spark voltage and generates a spark at a lower voltage then when the center electrode is at room temperature.

When two opposing potential conductors are on either side of a printed circuit board, the dielectric value of the material must be considered. The problem lies in the lack of good data about the effect of aging of most printed circuit material (see page 18). Also the method and type of construction of your laminate play a vital role in what actual breakdown value you will receive and what it will age to. A printed circuit manufactured from low resin high glass content prepreg will contain a large percentage of micro air bubbles. These micro air bubbles will degrade the initial dielectric rating and increase the effects of corona aging.

FR4 has an initial dielectric rating of 800-900 Volts per mil but due to aging effects, a more realistic value is only 300 Volts. I strongly suggest you manufacture your prototype boards with a few combinations of material thickness.

One board I made carried 15 thousand Volts between two layers and suffered arc over within a few minutes of operation. Upon calculating the breakdown rating of 10 mils of FR4 inner layer material, I realized that we needed more spacing and rebuilt the board with 40 mils of inner layer spacing.

Original manufacture: $10\text{mils} * 800 = 8000$ Volts (aged would be $10 * 300 = 3000$ Volts)

New design: $40\text{mils} * 300 = 12000$ Volts (worse case design scenario).

The high voltage was also comprised of a high frequency, which arcs over at a slightly lower voltage. The designer did not inform me it was a high voltage circuit and what layers carry the potential. When a printed circuit manufacturer lays out the build of an unspecified multilayer he would use a standard core of .40 thick, which leaves only 10 mils to each outside layer. He would do this because it is the cheapest and easiest to build. You must specify the build and the materials to be used and also give the manufacturer the reason why they will need to follow your specification.

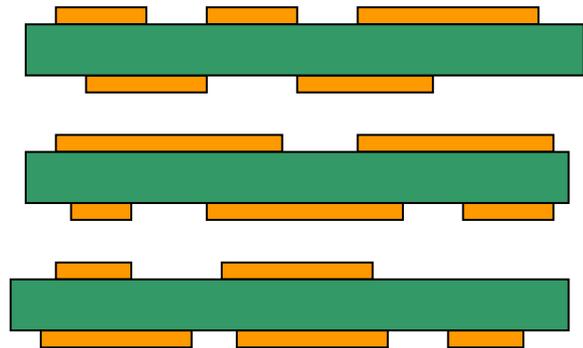
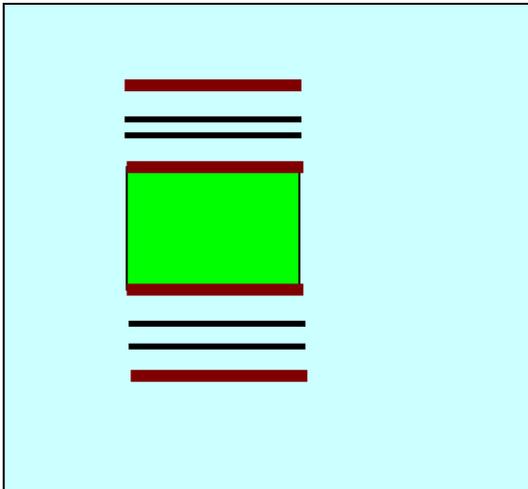


Figure 5: Typical 4-layer uneven construction Figure 6: Typical 6 layer even build construction

Field Grating Rings

It is possible to lessen the effects of arc over and corona by having lower potential circuitry surrounding the main conductors. These intermediate voltage-floating rings can be coupled with resistors or capacitors depending upon the AC/DC composition of the high voltage. A high voltage electrical field will redistribute itself towards an adjacent conductor. This then increases the field distribution area, therefore lowering the field strength per specific area and its potential for corona or arc over.

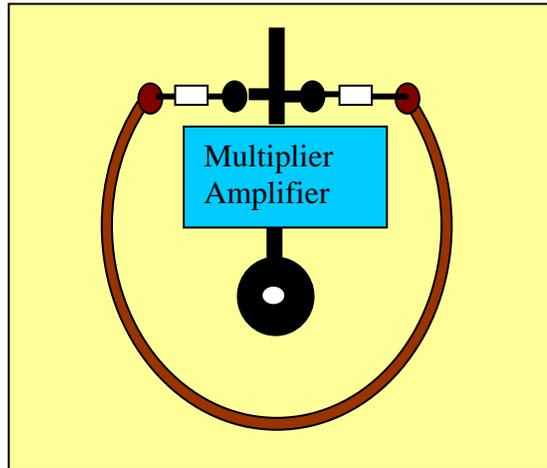


Figure 7: Drawing of field gradient rings

Solder Mask or Cover Coats

Typically printed circuit manufacturers use an epoxy based solder mask applied either by spraying on or roller coating. It is a very good product with excellent dielectric ratings. It does however, suffer from pinholes and voids along the edges of tracks. For low voltage work up to 1 KV, it is probably satisfactory. It will not offer much protection above this value. For mid voltage circuits, it is possible to use solder mask but with multiple applications.

When specifying multiple applications, use a wider clearance around the holes and pads to allow for tolerances. Speak with your manufacturer for the proper allowance. Not all solder masks are the same. The old standby SR1000 is really not up to the dielectric standards of today's photoimageable or roller coated UV cure solder masks.

A typical arc over rating for UV solder mask is only about 500 v/mil. A typical single application is from .7 to 1.5 mils thick depending upon the application method. This thin film is definitely NOT coherent. It will have voids along the sidewalls and pad areas. It will be full of micro air bubbles, and even contaminants such as dust and copper particles. I personally would not use solder mask in much over 1000 Volt circuits if the spacing is tight and 5000 Volt maximum on circuits if the spacing and board layout is very open. Double or even triple coating of the solder mask helps and is worth doing for the small charge the printed circuit shop will add. One problem to be aware of is the voltage rating for solder mask falls quickly with increase in operational temperature.

To increase a UV curable solder mask an additional oven cure and second UV bump will harden and strengthen the mask. For oven baked solder masks a UV bump will also harden and better cure the mask.

There are better options available. The flex industry uses a Kapton covercoat in place of a solder mask. It is pre-routed and drilled to get the openings and then pressed on using acrylic type glue. This Kapton covercoat is available in 1, 2, 3 and 5 mil thick sheets with 2000 to 3000 V/mil rating aged. You must however, design the covercoat with the manufacturing method in mind.

The preferred method of generating the pad openings (and the cheapest) is to drill them. This means your design must only use round openings with the tolerance specified by the manufacturer. You can design for slots and rectangle/square openings but the manufacturer must mill out the design on a CNC milling machine. Your minimum radius would be no smaller than 30 mils (some manufacturers can do smaller; it just costs more).

You therefore must design for the abilities of the milling method. New photoimagable Kapton covercoats are starting to appear but they are very expensive and the chemicals used to develop the image are not very friendly to humans.

You can multiple coat a board with Kapton to even further increase the arc over voltage, but more importantly, the added dielectric value of even one layer of Kapton will significantly reduce the effects of corona. There are three types of covercoats, Kapton with acrylic adhesive, adhesiveless Kapton and Mylar. HVPF can be used in place of Kapton at a higher dielectric value at, of course, a higher cost.

Figure 8:

Property	Units	Kapton with acrylic adhesive	Adhesiveless Kapton	Mylar	solder mask
Thickness	mils	.5 to 5	1-5	.25 to 10	.75 to 1.5
Tear strength	lb/in	1000	700-1200	1000-1500	N/A
Resistance to:					
Strong acids		Good	Good	Good	Good
Strong Alkalis		Poor	Good	Poor	Good
Grease and Oils		Good	Good	Good	Good
Organic Solvents		Good	Good	Good	Fair
Water		Good	Good	Good	Fair
Sunlight		Fair	Good	Good	Good
Fungus		Non-nutrient	Non-nutrient	Non-nutrient	Non-nutrient
Water Absorption	% (24h)	2.9	.8	<.7	
Max use temp	°C	-200 + 300	-200 + 350	-60 + 105	
Thermal expansion	PPM/°C	20	20	27	40
Dielectric Constant	1 MHz	3.4	3.4	3	4
Dissipation Factor	1 MHz	.01	.003	.018	.01
Dielectric Strength	V/mil	3800	6000	3400	1000
Aged 1000 hr	V/mil	2000	3500	2800	500
Volume Resistivity	Ohm-cm	1.0E+16	1.0E+16	1.0E+16	1.0E+14
Cost factor		Medium	Very high	Medium	Low

Prior to designing high voltage circuitry, the designer must be aware of trade-offs in performance, reliability, cost and manufacturability. Particularly for first time high voltage designers, the following steps are highly recommended.

- Scan industry literature and organize a base of high voltage design options and design constraints.

- Review the abilities and capacities of various circuit board manufacturers by reading company literature and data sheets.
- Tour the plants of several facilities, question the engineering staff as to their abilities in solving high voltage circuit problems. Examine their quality system and documentation process. Verify the training and involvement of the work force and their regard to product and quality knowledge.
- Once a suitable manufacturer has been selected, you should involve them in the early design stages of the project. Use their expertise to pre-solve any manufacturing issues.
- Understand the end product requirements and usage clearly, controlling reliability and costs.
- Utilize the ability to manufacture low volume prototype runs for testing and modification improvements.
- Establish communication trails through the process to keep everyone in the loop.

To prevent permanent arc over carbonation of printed circuit boards where there is the possibility of repeated temporary arc over from causes such as lightning or over voltage conditions, a routered slot can be placed so the arc over will occur but the printed circuit material will only carbonize to the edge of the slot preventing further damage. The slot should be designed for minimum width at maximum voltage, due to the printed circuit materials potential low resistance from previous arcs up to the edges of the slot.

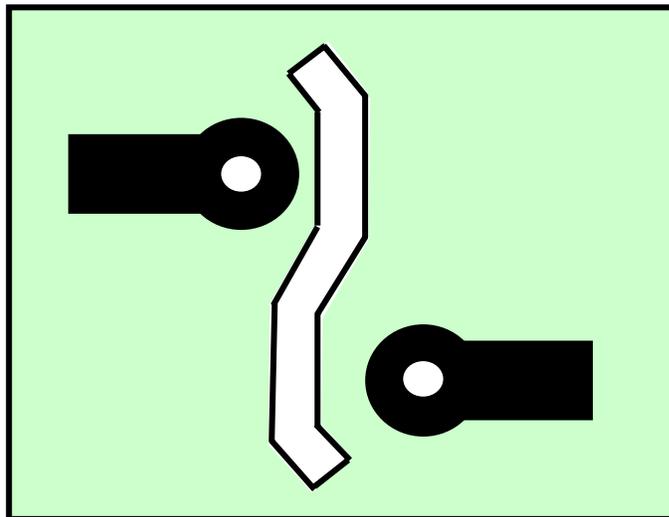


Figure 9: Router slot to prevent arc over permanent damage

All printed circuit machinery today uses Gerber RS-274-X language. The drills, routers, plotters, automatic optical inspectors, electrical testers as well as CAM and quoting software all use Gerber. There are limited converters from other software such as AutoCad, Corel Draw and Quadrant. Please ensure that your design only uses Gerber and all features are explained in a way we can understand. You may know every little detail of your design but we don't. The only place we can get correct information is your Gerber and "read me" files.

Typically circuit manufacturers use a .093" (2.36 mm) carbide router bit. This results in a minimum .047" (1.19 mm) inside radius. As in most production operations, manufacturers can produce a smaller inside radius, however at increased cost. Copper is a very soft metal and difficult to machine smoothly without a rough edge. To eliminate a rough burr, your design needs to keep the copper back from the routed edge, normally .020" (.50 mm) is sufficient. If the outer traces are carrying high voltage, then you need to keep them back from the edge by at least .001" per 100 Volts with a minimum of .020".

If your high voltage traces need to be closer to the edge you can have the circuit cover coated with HVPF, this will add a layer of protection right to the edge of the board.

The same theory applies to solder mask. Routed solder mask can chip. For best results solder mask should be .010" (.25 mm) away from a routed edge. For high voltage, thick copper boards, allow more space for the solder mask to cover the edge of the copper, therefore allowing for complete coverage and increasing the dielectric value.

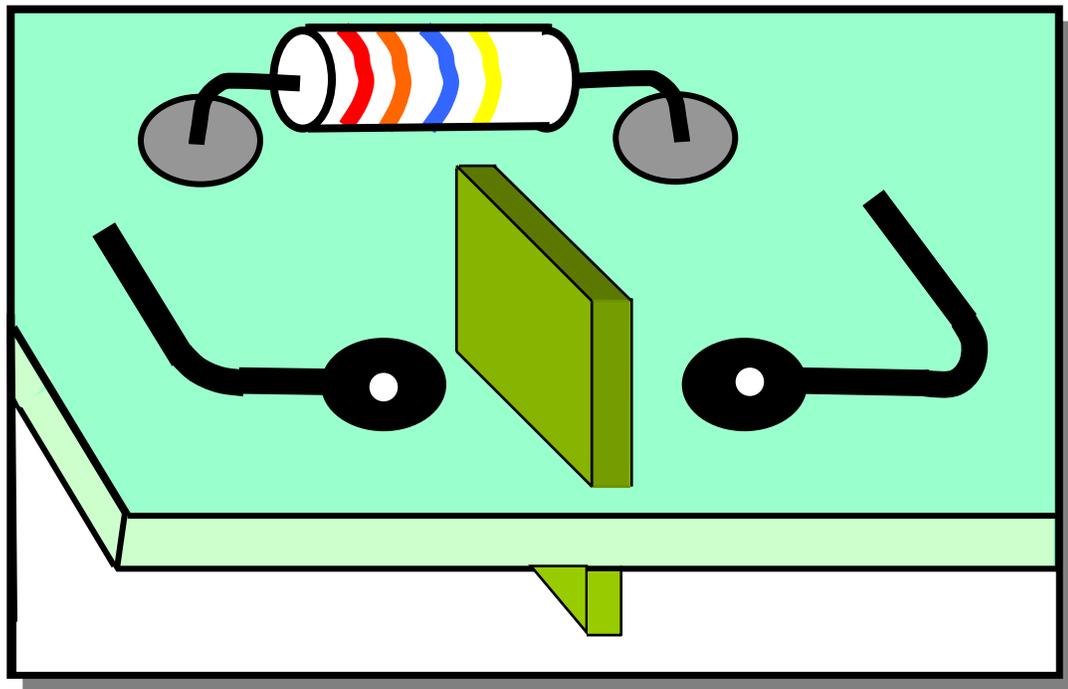


Figure 10: Insulated insert in high voltage areas

To further isolate high voltage areas an inert insulator such as polyester or Teflon can be press inserted in to a pre-routed slot in the board. The insert can be shaped to prevent removal from the board. In addition a suitable glue or retaining clip can be designed. For lower voltage work, the insert can be manufactured from circuit board material.

When using slots, the same theory for drilling applies. The pad must be large enough to allow a larger initial slot, which is then plated to the desired dimensions. There are minimum sizes for slots on the boards, consult your manufacturer.

Milling laminates with a slot width below .060" (1.52mm) is difficult, resulting in excessive broken milling bits, which increases your costs. The best minimum width of a slot is .100" (2.54 mm). Milling bits this large are significantly strong enough to give reasonable life and ease of production. Like most other options manufacturers can typically produce smaller slots; they just cost more.

During the design phase you must be aware of the attraction high voltage circuitry will have for dust and dirt. Typically high voltage circuits will be totally covered with a thick layer of dust after a few months of operation if some provision is not made to pre clean the air in the enclosure with a fan and filter. The dust collected will reduce the dielectric value around the high voltage areas and increase the heat trapped causing potential overheating.

When designing high voltage circuits the leakage current from the field and corona must be calculated, or at least experimented with. As time and degradation of components continues the leakage from increased resistance will also increase, possible to too high of a level.

Low voltage DC circuits have the potential to cause electrochemical migration, or growth of the printed circuit conductors when the correct humidity, voltage and metal materials are present. This growth is of conducting filaments of the metal conductor or its coating metal such as tin or sliver. Copper has been known to also grow filaments if the conditions are correct. These filaments can easily grow to .250" and will continue to migrate between potentials until they short. Avoid the use of pure tin or silver finishes on the printed circuit board. Tin with even a small amount of lead is much harder to create the filament growth.

The ability of a circuit to tolerate an occasional arc is an essential part of the overall high voltage design. Circuit board design and proper packaging techniques play a vital role in the ability to tolerate an arc. Most designs limit current available to an arc through inductive di/dt or resistive limiting combined with rapid turnoff current sensors.

High voltage component stresses must be thought of as field stresses within the component. Reliable equipment requires at least a 1.5:1 margin and more commonly a 2:1 ratio. Knowledge and proper use of corona detection equipment in the design and testing of the board layout is critical to successful designs. AC and DC corona inception voltages (CIV) are the key characteristics to be monitored.

Operating temperatures will determine the expected operating life from insulation degradation. High voltage integrity is critically dependent upon the insulating materials quality.

Circuit partitioning should be observed to isolate the high voltage power section from any low voltage areas as much as possible. Electrical interconnections should be minimized to prevent transient generation and propagation of high voltage fields.

Consideration must be given to the placement of noise sources and potential coupling through the stray capacitance of the insulation system.

The high voltage field is measured by the term called "E" field gradient. The higher the number, the greater the risk. There is an adjunct coefficient called the "utilization factor" that acts as a multiplier to the gradient number and this utilization factor is dependent upon sharp edges and proximity. Corona is generated by concentrations of the voltage field, usually as a result of sharp points, small geometries and their associated spacings.

Utilization factors, based on the minimum voltage stress condition, are obtained with a uniform voltage distribution across the insulating material. Corona inception and associated problems can be avoided by the following.

- Specified geometries should be consistent with the voltages contained within the circuit. A high-voltage "E" field gradient analysis should be performed to ensure that the appropriate utilization factors were used with the specific geometries.
- Component case and even conductor shapes can create concentrated voltage fields and/or fracture planes. Component edges, corners and fasteners should have the largest radius possible.
- Positioning of all components, connectors and cabling should be checked by design and verified throughout the assembly process.
- Conductors exiting from high-voltage planes should not create concentrated voltage fields at the exit point.
- Where connections are made using solder techniques, a minimum solder ball radius should be specified.
- Avoid the use of multiple insulating materials.
- Minimize interfaces and connections.
- Establish and enforce assemble cleanliness procedures to prevent contamination.
- Use vacuum impregnation and pressure curing techniques to minimize voids in conformal coatings and potting materials.
- Prepare all surfaces for bonding using wet, dry, plasma, or etching techniques. Ensure proper cleaning of product before conformal coating.
- De-rate insulating materials based on maximum, not average electrical field stress.

The voltage gradients within a resin system should be less than the age rated VDC/mil across the interface or between the insulating materials, AC voltage gradients should be less than one half the DC gradient. When printed circuit boards are used in high voltage fields they should be shielded or have barriers added. Corona testing is mandatory to demonstrate the level of design margin.

The military printed circuit standard, MIL-STD-275 recommends an approximately 8 Volts/mil spacing between conductors, however it is out of date and exceptions may have to be applied for. The use of Kapton or HVPPF can significantly increase that recommendation to in excess of 1000 Volts/mil.

Chapter 4

High Voltage Multilayer Design

It is possible to make multi-layers with medium voltage on all layers. The major consideration is the proper filling of the spaces between the layers. The thickness of the separation between layers must be at least .005" in order to maintain the integrity of the filling medium, prepreg. Any voids or pockets will degrade the dielectric value seriously. The standard prepreg FR4 type multilayer is not suited to medium or high voltage work. The material breaks down too fast and does not feature a homogeneous internal structure. The excess micro voids degrade the dielectric rating resulting in its poor performance.

The trick when pressing multilayer boards, is to get the amount, thickness and flow rate of the prepreg correct. Too high of a percentage of glue in the prepreg will cause it to squish out. Too much prepreg in the build will cause the final pressed thickness to exceed required dimensions. Too little prepreg will cause dry weave from resin starvation and possible inner layer shorts.

Prepreg can easily press out at a tolerance of $\pm .002''$ (.05 mm) per layer with standard practices and construction. If you require tighter tolerances in the thickness and separations, please talk with your manufacturer. When pressing a multilayer the tolerances can add together or subtract or can even themselves out. Typically prepreg is thicker rather than thinner. The copper is usually thicker because manufacturers want to err on the thick side. Most of the time the cores used as a base of the multilayer are very close to the specified thickness.

Figure 11: Materials Supported in Multilayer High Voltage

Material Type	Max. Operating Temperature (°C)	T/G °C	Voltage (V/mil) Note 1	Aged rating (V/mil)	W°C/m
FR4	105-130	160	800	300/150	0.21
FR4 Hi-Temp.	130-150	170	800	300/150	0.22
BT Epoxy	140-160	180	1300	600/400	0.40
Polyimide	150-190	200	900	700/500	0.25
HVPF*	180-200	210	3000 to 7000	3000/2000	0.28

***HVPF is a trademark of Sierra proto express.**

Note 1: The voltage rating given in figure 11 is from the manufacturers data and is for new material. Voltage ratings will decrease significantly from the effects of high temperature, age, humidity and contamination from oils and chemicals. During one study of FR4 and the effects of aged voltage ratings it was noted that some manufacturers' samples de-rated from 750 Volts/mil to as low as 150 Volts/mil after as little as 6 months of exposure to the environment under an automobile hood.

Chapter 5

High Voltage on Heavy Copper Circuits

Heavy copper boards can operate in a high voltage condition, provided that the standard design and construction rules are followed. I have included a short chapter on heavy copper high voltage design guidelines. For in depth information about heavy copper printed circuit design order sierra proto express book: **High Power Printed Circuit Design Notebook;**

There are a few areas to be aware of, when designing a heavy copper board for high voltage. One is the circuit spacing. High voltage creates shorts by two methods, direct arc over and corona. Arc over suddenly occurs when the voltage potential between two conductors exceeds the ionization value of the insulator between them.

If there is sufficient DC potential superimposed over a high frequency system and you have arc over, the DC component will produce the most brilliant plasma arc you have ever seen. I had one such circuit literally evaporate the printed circuit board and all the components in the area of the arc. It takes only a few thousand Volts of AC with 4 to 10 Volts of sufficient current potential DC combined to produce plasma. The circuit will continue to arc as long as the DC component is present. The high voltage AC arc over starts an ionized path from which the DC will follow. This type of very destructive arc over is similar to the operation of a TIG welder.

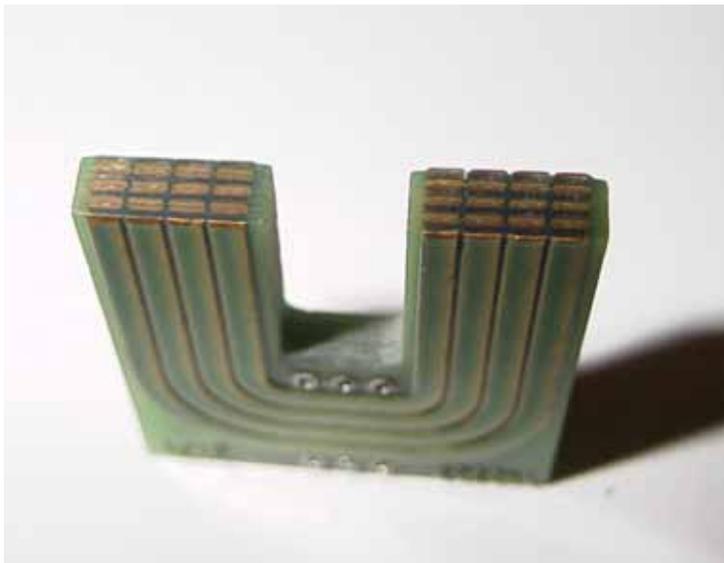


Figure 12: A heavy copper, high voltage, planar board

The main culprit is corona, the invisible destructive force that slowly carbonizes the circuit board material. Corona is the ionization of the air and material immediately surrounding a high voltage

circuit. It has an especially large effect if the high voltage conductor is sharp and pointed. It's potential damage increases with voltage and can be visually seen in really high voltage circuits as faint blue lightning like fingers coming forth from the surface.



Figure 13: Picture of corona

To minimize corona, the shapes of the traces must be as round as possible. Avoid any sharp 90° bends; make the traces flow with rounded corners. The soldering should be round and ball like, avoiding sharp pointed tips that enhance the corona effect. For double-sided circuits, use as thick a board as you can, therefore giving you as much insulative material as possible between potentials. Space the high voltage circuits away from each other as much as physically possible.

On multilayers, allow the manufacturer as much room between the layers as you can. One flaw with high voltage thick copper multilayers is the laminate does not press out fully without some air gaps and micro voids, which decrease the dielectric breakdown potential. On thicker copper multilayers, the common practice is to specify multiple layers of prepreg to lessen the chance of a continuous void between heavy copper layers. Use high resin content small glass bundle prepreg such as 2113 or 1080 in place of regular prepreps such as the thicker higher glass content 7268.

To increase the dielectric strength between multilayers, it is possible to use a single sheet of HVPF material from .001" to .005" thick as a replacement for a layer of prepreg. As it is a film with no voids or holes, the rating is very high at over 3000v per mil aged. To further decrease the incidences of an arc over or the effects of corona, coat the board with two layers of solder mask. Again two layers printed at cross-angles decreases the chance of a continuous pinhole or void. A UV cure bump and an extra solder mask bake further cures the solder mask and increases the dielectric value of the completed circuit. Or alternately a layer of HVPF or Kapton covercoat will significantly increase the dielectric arc over value.

To assist in reducing the arc or corona effects of the completed circuit, a low temperature pre bake and a spray coat with one of the better conformal coatings will further improve the circuit's ability to withstand the ravishing effects of high voltage.

Chapter 6

Material Specifications

Laminate manufacturers voltage ratings are not an aged rating but rather a one-time test result performed in a laboratory on new samples. After some serious research into voltage ratings and the effect of environments, temperature and time have on voltage ratings; I quickly realized that you cannot rely solely on published manufacturers data.

In one test, I manufactured standard dielectric IPC test panels. The dielectric values which were tested and recorded were slightly higher than the manufacturers published specification. The test boards were tie wrapped to the engine bay of a daily driven car in Ontario, Canada during the winter months. At the end of each month, the boards were recovered, washed and dried. They were then thoroughly cleaned with isopropyl alcohol to remove any trace of road salt. The test board dielectric values were tested and recorded. The initial drop was quite large, significantly more than expected actually. From an 1800 Volts/mil reading to 900 Volts/mil in the first 30 days was very surprising. We re-looked at the test samples ensuring a new strip was used every time to reduce the effects of arc over from the testing. The boards were re-cleaned very carefully and retested. The results were the same; a one half drop in voltage rating. The tests continued with the value reducing dramatically every month to a final rating of 150 Volts/mil.

The surprise was that the material was a fairly standard FR4 product. The outer surface showed serious degradation as did the tracks and solder mask. The under hood of a car in the Canadian winter has to be the harshest environment going, very low temperatures of -40°C to high temperatures of 100°C when running and a constant spray of salt and other nasty road chemicals such as alcohol from windshield washers, asbestos from brakes, oil and grease from the engine, and oxidizing exhaust gases.

My experiments, however, concluded that one problem a customer was experiencing with arc over in an automobile ignition circuit was environment based. I redesigned the circuit to use a higher temperature polyimide with a better solder mask coating and an overall coating of a spray on silicon. The new product survived at least a few years under the hood instead of weeks. FR4 material is not suited to extreme temperature excursion. It is also quite porous in nature compared with BT epoxy or polyimide, therefore allowing larger values of environmental contamination. It was also found that FR4 suffers from weak edge structure, on planar coils and other boards that feature circuitry right to the edge. This weak edge allows cracks and therefore degraded voltage ratings to the outside circuits. BT epoxy has the strongest sidewall and is therefore used exclusively on planars and critical medium high voltage circuits.

FR4 also lacks an ability to recover from the carbonation an arc produces. Materials such as Isola F2 paper phenolic laminates Supra-Carta series were designed for use in high voltage circuits in television sets. The arc resistant laminate is ideal for high voltage printed circuit boards, as any

arcs that are generated extinguish immediately so that a non-conductive base material remains. It is limited in its manufacturability to single sided or simple double-sided boards.

Figure 14: Material properties for high voltage laminates

PROPERTY	ISOLA FR4 406	NELCO 5000 BT EPOXY	ISOLA POLYIMIDE	HVPF	TEST METHOD
T/G °C	175	185	267	240	
X/Y CTE PPM	12 to 15	10 to 14	12 to 15	10 TO 12	
Z CTE PPM	180 to 200	3.75 %	50 to 70	50 TO 99	
DIELECTRIC CONSTANT	4.7	4.1	4.49	4.4	ASTM D 150
DISSIPATION	.019	.013	.010	.02	ASTM D 150
CAPACITANCE				PF / SQ IN	ASTM D 150
VOLUME RESISTIVITY	8 * 10 ¹⁴ MΩ	1 * 10 ⁷ MΩ	2.53 * 10 ¹⁸ MΩ	8 * 10 ¹⁸ MΩ	ASTM D 257
SURFACE MΩ	4 * 10 ¹²	1*10 ⁷	4.87 * 10 ⁷	4* 10 ¹⁸	ASTM D 257
COPPER PEEL STRENGTH	9.7 LB/IN	10 LB/IN	10.7 LB/IN	10 LB/IN	IPC-TM-650 2.4.9
WATER ABSORPTION	.24 %	<.5%	.15 %	.14 %	ASTM D 570
FLEXURAL STRENGTH	81,200 PSI	75,000 PSI	61,000 PSI	80,000 PSI	ASTM D 790-95
COMPARATIVE TRACKING	186 VOLTS		274 VOLTS	1275 VOLTS	ASTM D 3638
DIELECTRIC STRENGTH	900 V/MIL	1200 V/MIL	1300 V/MIL	5000 V/MIL	ASTM D 149
CHEMICAL RESISTANCE		.07 %	.074-1.17 %		METHYLENE CHL
			.071-.79 %		N- METHLPRROLI
			.178-2.49 %		BUTYL CARBITOL
FLAMABILITY	94 V-O	94 V-O	94 V-1	94 V-O	
THERMAL CONDUCTIVITY	.24 W/M °C	.44 W/M °C	.26 W/M °C	.24W/M °C	ASTM D 5470
SOLDER BATH RESISTANCE	120 SEC @ 260 °C	200 SEC @ 260 °C	240 SEC @ 260 °C	220 SEC @ 260 °C	IPC SOLDER FLOAT TEST
RELATIVE THERMAL INDEX	140 °C	180 °C	200 °C	200 °C	
COLOUR	GREEN	TAN	BROWN	LIGHT TAN	VISUAL

ALL SPECIFICATIONS DERIVED FROM EACH COMPANIES LITERATURE

Chapter 7

Survivability

Designing Power Supply PCB's for Maximum Reliability

As electronics are required to power, control and run our lives, more of that control is of a critical nature. Electronic devices on aircraft, backup inverters for operating rooms, motor drives for elevators and thousands of other applications require the printed circuit to have an inherent survivability. I define survivability as exposure to internal and external forces that would normally destroy or cause a malfunction. Example: An arc over short on a nonessential feature of an aircraft circuit that may destroy a critical power distribution printed circuit before the fuse blows. In order to improve your product, I embarked on a high voltage survivability study of printed circuits, which is explained here.

The high reliability boards have been named Hi.E.R. which stands for High Electronic Reliability.

Outside independent qualified tests show our new Hi.E.R product exceeded 2000 thermal cycles from -40 to 145 deg C. Additional in house testing qualified the Hi.E.R circuit with stood 30 solder cycles at 550 deg F or 3 times the lead free T288 test.

Typically a normally manufactured 6 layer Fr4 printed circuit when subject to Hats Thermal testing cycles only last 120 to 240 cycles before the via holes crack or open.

To Qualify the new Hi.E.R product 36 samples of mixed construction and control normal boards were sent to Cat IRTS testing service for prolonged thermal cycling on a HATS tester. The samples were pre conditioned at IRTS with IPC PCQR2 assembly cycle standard of 6 simulated solder assembly cycles then put on thermal test, after 13 days and 2000 cycles later the Fr4 6 layer boards passed.

The assembly simulation was performed on an APS convection reflow oven as follows:

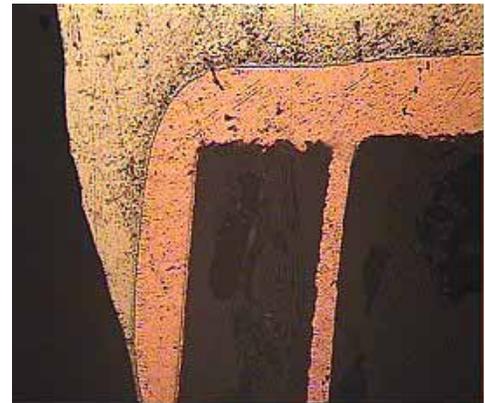
- * 2 minute heat-up to 183C
- * 1 minute dwell between 183 and 215C
- * 3 to 7 minute cool-down (dependent on coupon thickness)

Even the low T/G 135 deg C Fr4 samples survived 1600 to 1800 cycles, far beyond the normal 120 cycles typical in the industry. A solder float test was initiated in which samples of Hi.E.R boards were subjected to repeated solder immersions, the Hi.E.R circuits survived over 30 cycles for 10 sec at 550 deg F, with out any evidence of hole cracking, proving it a very robust board.

The difference between our Hi.E.R. circuits and normal boards is the proprietary plating technology of the copper in the via, because the copper is stronger it is able to withstand the expansion forces involved in a thermally cycles printed circuit board. This means the Tg of the material no longer controls the upper temperature limits or the thermal cycling abilities of the laminate. A better index is the TD or thermal matrix degradation temperature.

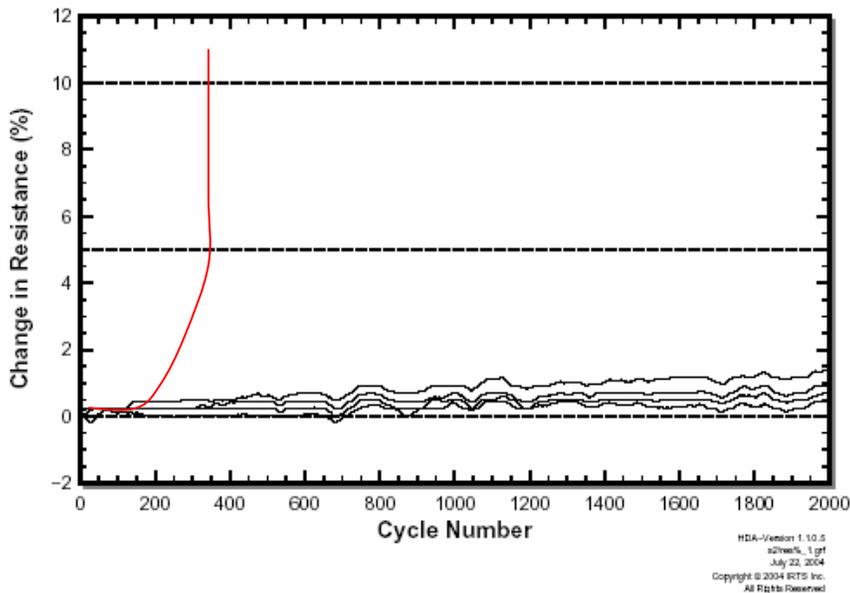
To experiment and learn about via failure, a printed circuit was designed with 100 holes in series. Boards were manufactured with ascending weights of copper 1oz. through to 10 oz.'s A calibrated four wire Stanford low resistance meter was employed to accurately measure the via strings resistance. If the resistance shows a sudden rise after a series of consistent readings, the vias are starting to pull apart, through cracking in the hole. A 5% increase in the resistance is ample indication of a serious failure pending.

The first experiment used a standard IPC test of - 50°C to 130°C for temperature cycling. This test may be satisfactory for normal vias . It is however not severe enough to stress Hi.E.R boards . I could not get HI.E.R. to fail after even 100 cycles. However normal vias failed as expected at about 6 to 10 cycles. I abandoned the IPC cycle test and developed a very tough new test; 750°F for 30 seconds directly to - 70°F for 3 minutes. The sample was given a rest, to stabilize before the resistance measurement. To summarize, the normal vias. failed quickly within 4 to 10 cycles; the Hi.E.R. lasted 200 cycles . The Hi.E.R. boards showed no sign of failure even when the FR4 fiberglass was black and falling apart. I understand that this test was extreme, however I needed to find the failure point, which the first test did not achieve.



Page 6

Net 1 Resistance by Cycle Graph



Thermal cycle test chart showing normal sample in red and Hi.E.R. in black

A major factor in power circuit survivability is the ability to handle large over currents. I have seen many burnt and blackened printed circuits, mostly from exposure to very instantaneous short circuits. In an effort to learn what happens when a circuit “blows up” I did just that, blowing up many circuits in my lab. Unfortunately the stink from burning FR4 did not please my fellow workers, but science must go on.

Typically when a 1 to 3 oz. circuit fails, the vias blow out first. The thin copper cannot withstand any large amount of over current. An 8 layer board of 2 oz. copper can replace a 2 layer 6 oz. power board but it cannot dissipate the heat generated through the multilayer build effectively. I recommend that inner layer copper be de-rated 50% to 60% of normal current carrying ability.



Figure 15: Over-current test board

Survivability also relates to mechanical stress: 1 and 2 oz. vias are easily damaged by bending of a double sided and especially a multi layer board. A 10 oz. FR4 printed circuit is so strong it is difficult to bend. I tested several samples repeatedly through 90° bends in a vise with no failure to the electrical circuits. Even a slight increase to 2 oz.'s of copper in the holes improved the cracking/ bending relationship by over 120%.

A 6” long printed circuit was designed with large pads to attach 00 wires to a 1000 amp power supply (see figure 15). The circuit featured three lines of .250”, .500”, and .750” wide copper in various copper thicknesses.

I experimented with the circuit’s ability to pass current while monitoring temperature. The results were unexpected! I had always used an old IPC current/temperature chart. This was found to be inaccurate. Multiple tests have shown there is no “one” chart. Each thickness and type of board needs a separate chart. Very wide differences were found between bare copper, solder mask and oxide under solder mask. Bare copper features a very low emissivity offering little heat conductivity, equating to a larger temperature rise. Solder mask increases the emissivity but decreases the convection due to lower conduction figures. However, a black oxide over copper, then a solder mask, nets the lowest temperature rise for given current. It was noted that the temperature was not consistent either along or across the track. See figure 16.

Temperature increases towards the middle of the track are created by adjacency heat theory. Simply, it means the center gets hotter because there is heat on both sides. The ends are cooler as there is only heat being generated from one side. To increase the current carrying ability of a long track, increase the surface area in the middle, increasing the heat dissipation and reducing the temperature. See figure 17.

As the temperature of a track increases, the resistance also increases. The extra heat caused by the increasing resistance causes further heat. Soon the temperature is in an upward spiral. The only end to the spiral is the removal of the power or the circuit failing. When a printed circuit board is in the unfortunate situation of carrying more power than it was designed for, a specific chain of events occur. The temperature rises causing the resistance to rise. The FR4 heats up enough to emit smoke. The track will over heat in the center causing the FR4 to reduce its adhesion on the track. The heat will expand the track off the board. The rising of the track can be a problem if the expanding track contacts other electrical parts. There will be increased smoke but no flames. The solder mask will blacken in the center, then burn off. If the power continues, the center of the track will now be red hot, the smoke then turns purple. The time to fusing and an open circuit depends on the copper thickness. A 10 oz. circuit can stay red hot for several minutes. After the over current is removed, the circuit may continue to function. It may look real unhealthy and definitely needs to be replaced. To increase the printed circuit's ability to survive over currents, increased copper thickness directly improves their survivability. Adding vias, which act like copper rivets will keep the track from expanding off the board.



Figure 16



Figure 17

When a serious arc develops the core temperature reaches 20 000°C instantly, the process of vaporization of the metal starts. At that temperature the copper will expand to over 60 000 times its original volume. With that size a volume rise the surrounding air will generate a large pressure. This pressure is significant enough to blow the molten copper off the board and onto surrounding objects.

The formula for calculating arc pressure is $P=(2NUIt)/V$. Where P is the pressure in atmospheres, N is the number of arcs, U is the voltage drop per arc in KV, I is the current of the arc in KA, t is the time in seconds and V is the volume of the enclosure in M3.

Chapter 8

Planar Transformers

High voltage, high frequency switching transformers are effectively manufactured as very small cost effective planar transformers. The printed circuit that replaces the typically wound coils is flat, extremely durable, high temperature resilient, moisture resistant and can feature very high inner layer, voltage dielectric breakdown ratings. The printed circuit planar transformer is rapidly gaining industry approval. The planar has evolved through many improvements to today's strong, tough, high reliability product.

The first planar transformers were manufactured from individual double-sided FR4 printed circuits with FR4 insulators. They featured the technology of the day, however the construction design could not easily handle the higher turn count or higher voltage in an effective small package. Wire and solder type assembly was required to join individual layers to form multilayer turns. This solder tab area added to both the cost and size. The spacers prevented effective high voltage dielectric figures. The construction method dictated the transformer had to be potted after assembly to provide the necessary voltage ratings and for environmental protection at an additional cost. The advantage at that time to the individual layer approach is for higher current applications. The secondary coils can be inexpensively punched from copper sheet. As printed circuit manufacturers learn methods of effectively producing heavy copper circuits, the single layer construction technique is quickly losing favor due to its high assembly cost and bulky size. Also the thickness and material type of the separator could be selected to provide higher voltage ratings.

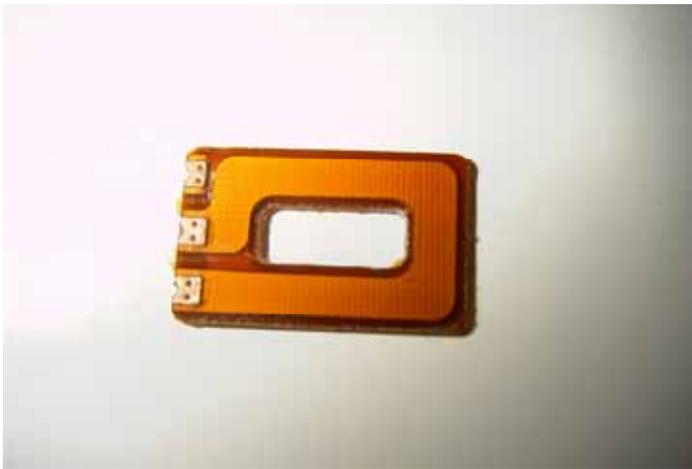


Figure 19: HVPF high voltage planar capable of 2500 Volts

The next generation of planar circuits featured multilayer construction, often with blind and buried vias to connect the many turns and layers. Exotic materials, such as BT epoxy and polyimide improved the low voltage rating of FR4 used in early circuits. The new transformers

were smaller, cost effective and very durable. There were however, problems associated with this construction design.

Planar designs progressed with more turns and more layers. It is not uncommon to manufacture planers today with eight separate coil circuits in twenty-four layers. They feature blind vias between eight layers and buried vias between fourteen layers. The inner layer spacing required to fit this wonder into a standard thin sintered core is .004". As the spaces and layers get thinner, the voltage rating quickly drops below a usable value. UL certification requires three separators between circuits, with the thinnest prepreg available today pressing out at .002" the minimum spacing is .006". This limits the minimum overall thickness and layer count that can be manufactured effectively. The thin design limited the usable voltage rating to as low as 1200 Volts in FR4.

As the thickness of the planar circuit grew to accommodate the rising layer counts a new problem surfaced. A long small via is difficult to plate properly at ratios exceeding six to one. With typical via hole diameters of .018" and board thickness growing greater than .160", this resulted in plating ratios approaching nine to one. At this ratio, the vias presented more than enough of a challenge. As planar designs evolved, engineers found ways to produce more power from the little circuits. Correspondingly, they needed more copper to handle the larger currents. As the copper thickness grew, so did the associated manufacturing problems. Thick copper traces require very controlled plating and etching to manufacture the line edge definition required. Thick copper in multilayer construction prevented proper filling of the space between layers, as the prepreg could not flow to fill in the large gap between the traces, further degrading the voltage dielectric ratings.

For today's thinner, high power planar transformer, a newer advanced construction technique was required. I developed HVPF (High Voltage Polyimide Film). Extremely thin planar circuits can now be manufactured that feature very high voltage dielectric breakdown ratings, high temperature ability and heavy copper traces in a multilayer circuit. With over 3000 Volts/mil dielectric rating, coil layers can be designed with as little as .002" separation. HVPF with the high temperature glue system has an operational maximum temperature of 180°F. An outer cover coat of HVPF creates an environmentally sealed high voltage protective cover, protecting against moisture, electrical contact and physical damage. The HVPF covercoat negates the need to pot the assembly for protection. HVPF uses a thermoset glue system, which eliminates the problems associated with prepreg's poor filling ability. The thermo-set adhesive stays put effectively filling all gaps and spaces between copper traces. By designing .005" thick inner layer separators from HVPF circuits it could operate at in excess of 15 000 Volts.

Designing for heavy current planar transformers requires solving specific manufacturing problems associated with the thicker copper traces. As the copper trace thickness exceeds 4 oz.'s (.0056") new design rules apply. Line width and spaces relative to copper thickness are typically .003" per oz of copper thickness. As the switching frequency rises, the phenomena of skin effect needs to be considered and calculated with the formula $k = \sqrt{F}$. k is the effective depth of the skin effect in mils; F is the frequency in Hz. The depth is from all sides, effectively doubling the usable thickness. Some designs rely on multiple layers in parallel to distribute the higher current.

As the transformer design engineer, you will be responsible for all areas of the board design. You will realize with the first printed board order that the technology involved in planar transformer manufacturing is not known to most printed circuit personnel. The typical printed circuit engineer knows little, if any, regarding magnetic transformer design. You will need to nurture him, tell him your expectations. Just because you spent hundreds of hours creating and designing your little exotic planar monster, does not mean your selected printed circuit shop can correctly manufacture your creation.

Planars feature very thin inner layer tolerances; a technology most printed shops need not readily possess in normal board production. At the beginning of the planar circuit creation process, talk to your board manufacturer, seek their advice, spend valued time learning why and how board shops do things. What software and format do they require? You will probably want to work in AutoCAD; most board manufacturers only willing accept Gerber. Machines such as drills plotters and routers only accept Gerber, nothing else. Spend time defining the tolerance expected. Ask if they're acceptable and if not, what is.

The previous paragraphs were written because the single largest problem in manufacturing planar circuits was the designer's lack of knowledge of standard printed circuit manufacturing practices.

Chapter 9

Testing High Voltage Boards

The testing of high voltage boards is broken down into three main subcategories; Printed circuit incoming receiving inspection, assembly inspection and design testing.

Printed circuit incoming inspections are necessary to ensure the manufacturer of the printed circuit board correctly performed the task. The parcel should be inspected and the part numbers checked. All printed circuit boards must be carefully handled with white cotton gloves. The outside dimensions should be checked to tolerances specified. A hole diameter check is performed, being careful not to damage the holes, again to specified tolerances. A sample amount should be tested for ionic contamination. The thickness and material build should be verified, as should the overall appearance of the board, looking for quality workmanship of solder mask, hole alignment and trace accuracy.

For critical work a thermal cycling/shock sample should be requested. This sample should be clearly marked and packed separately. Use this sample to test for three to five 10 sec solder float cycles and cross section potting. Inspect the integrity of the hole wall with a microscope for cracks at least 100 power. A section of the test sample can be used to test for solder mask adhesion and solder ability. A flux coated specimen is floated in 550°F solder for five seconds then allowed to cool. The specimens should show no adverse effects to the solder mask from the solder nor should the pads show lack of solderability from solder mask bleed. A section of the sample may also be used to test the dielectric strength.

After inspection the boards need to be carefully rewrapped with sulfur free plastic and sealed tightly to reduce the moisture absorbed, even if they are to be used within a couple of days. Boards should only be unwrapped just before use.

The assembled boards require inspection of the solder joints in the high voltage areas to ensure a nice even round ball, as does the placement and orientation of parts. The overall board needs checking for correct parts. A cross section sample should be checked for ionic contamination. All subassemblies that require ESD procedures must take proper precautions. Potting/conformal coating inspection requires a initial visual inspection and possibly a test sample cross section to reveal proper filling, presence of bubbles or micro voids. Completed assemblies are often checked with Hi-pot dielectric testers in specific areas. Only qualified well-trained and supervised employees should use high voltage testing equipment like Hi-pot testers, as they can be very dangerous.

High voltage power supplies represent a special challenge when testing for thermal performance. The presence of thermocouples can create leakage currents, which can create measurement errors and compromise personnel safety.

Where at all possible, use analysis techniques or non-contact inferred measuring devices in place of thermocouples in high voltage sections. Where a thermocouple must be used, an isolation device must be placed between the bead and the measuring equipment to ensure safety of the operator. Provide shields or bleeder resistors to prevent generation of high voltage by leakage-current paths through the thermocouples.

Corona computerized measuring equipment can, with reasonable accuracy, characterize the corona "signatures", there is however a considerable variation due to electrical noise within different measuring methods. Where an oscilloscope is used to measure corona pulses only an approximate CIV can be measured. Test equipment that applies pulse height analysis can define the corona intensity more accurately. Corona is expressed in an average of picocoulombs per second. AC and DC corona test levels should be specified at 120 to 200% above the desired maximum working voltage. The corona level increases at the second to ninth power with increasing voltage. An established limit of 1 to 4 pC will ensure the circuit will be corona free.

A test circuit is connected to the pre calibrated test equipment and an increasing AC voltage (60Hz) is applied until significant corona activity is seen. To improve the sensitivity of the measuring equipment a properly shielded room and correct lead and probe filtering is required. A poor setup will have a lower limit of 50 pC where as an exceptional well shielded test chamber can measure 3-10 pC reliably. The test is repeated to compare values and recorded as the inception value. The test is repeated measuring the point at which the corona extinguishes and recorded. The above test can be repeated for different circuit material or assemble methods to determine the best layout and materials to use.

It is important to measure the corona levels before and after a pre-determined number of thermal stress cycles. Potted assemblies can separate from the components during repeated thermal cycling; as well materials and printed circuit boards do degrade with thermal stress.

High voltage circuit poses an especially high risk of injury to personnel testing or operating these circuits. I have seen many test benches cluttered with junk while testing circuits of 15 KV at considerable current. Keep your area clean, post signs warning of the danger. A rotating red light is helpful in warning of an operational circuit. Arcs during testing can create flashes and showers of molten copper. When testing pressurized containers, danger exists from explosion and spray of hot fluids. Safety glasses or a shield are required.

Personnel assigned to work in high voltage areas should be trained and compliant in all procedures and safety issues; a buddy system is needed in all high voltage areas. At one work site an operator was training a rookie on how to change the large output tube in a transmitter. The operator took a long copper pipe with a huge wire bolted to the frame, and touched the top of the capacitor feeding the tube, drawing a large bright spark. The rookie thinking that the capacitor was safe rushed in to start work, the operator grabbed the rookie and stopped him. He reapplied the shorting bar and drew another bright spark. The rookie stood there realizing the potential deadly mistake he almost made. Large capacitors or high voltage circuits can recharge themselves very quickly. I know, because I was that rookie. We left the shorting bar on and I felt much safer.

All high voltage circuits must be rendered safe for handling by other personnel such as assemblers, inspectors, packing and receiving staff. This means all capacitors must be drained and regenerating assemblies, such as glass or dielectric spheres, be shorted.

Pre-charging capacitors with voltage and leaving them around for someone to touch is not a funny practical joke, but a deadly game. As a precaution, I always treat every capacitor like it is charged.

Arc resistance testing of high voltage power circuits is required to ensure that the circuit can withstand arcs from each output to all other outputs around as well as ground. It's not that your circuit may arc, but more a matter of when. Perform the arc test at both ambient temperature and normal humidity but at elevated maximum specified temperature and humidity. Also test with the line voltage at maximum specified and with incoming surge and spikes.

To test for dielectric strength of solder mask materials used, use a piece of printed material 4 inches by 4 inches copper, clad one side only, and apply a 3 inch by 3 inch solder mask in the center, properly cured and applied as per manufacturer's specifications. The ground lead off the high pot tester is applied to the copper and a two-inch diameter electrode attached to the second lead and placed in the center of the solder mask. The test voltage is applied in increments of 100 Volts rising at the rate of 100 Volts per 10 sec. When breakdown occurs, the voltage is recorded. The sample must be discarded as it now has a hole burnt into the solder mask somewhere within the 2-inch diameter probe area. The thickness of the mask is recorded and divided by the breakdown voltage giving a (Volts/mil) value.

The same procedure can be used with the printed circuit material, a 4-inch square sample with copper on one side is prepared and the 2-inch diameter probe placed on the opposite side to the copper. The voltage required will be significantly more, so extreme care must be used. Use a thin sample to limit the voltage.

Chapter 10

Assembly Considerations

Assembly techniques can effect the operation of a high voltage circuit. Nice tight solder filets used in normal soldering create a pointed needle like effect lowering the corona and arc over voltage potential by up to 3 times. Use a large round solder ball and file off any protruding lead point.

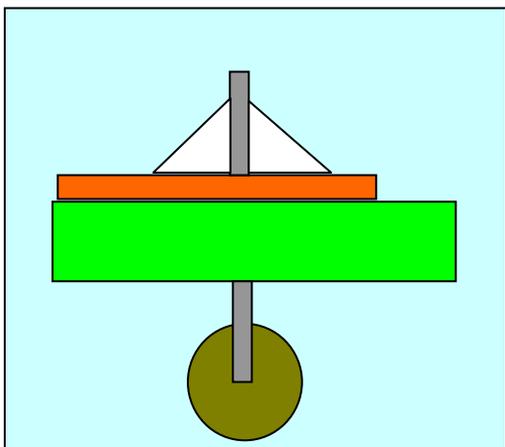


Figure 24: Wrong type of solder fillet

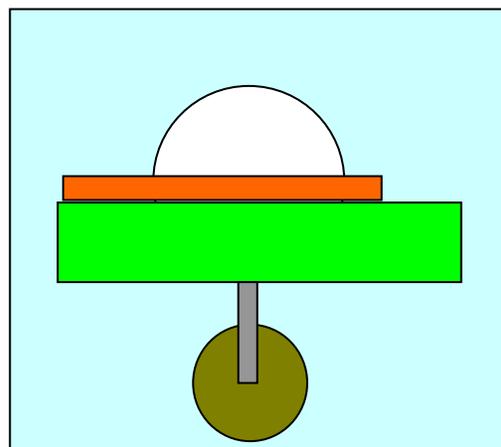


Figure 25: High voltage type solder ball

Additional metal sleeves can be placed over the component leads to increase the area of the field therefore lowering the overall field strength at the fine component lead and increasing the arc potential required.

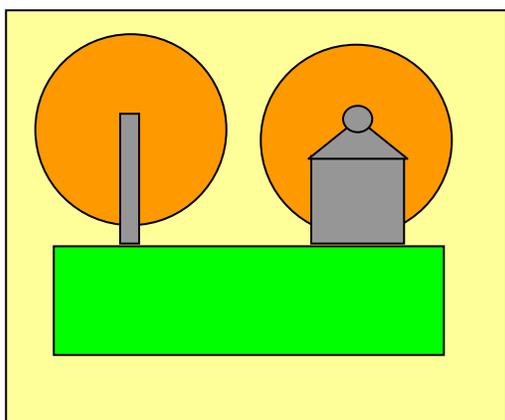


Figure 26: Component lead sleeve

Where the assembly process can really affect high voltage circuits is with leaving a conductive residue. Every effort must be taken to ensure the complete removal of any flux. Rigorous cleaning and proper selection of the flux will help to limit the residue flux. The circuit conductivity should be measured using an ionic chamber. An ionic chamber is filled with purified reagent grade isopropyl alcohol. The solution is cleaned with a charcoal reverse osmosis canister and cleaned until the resistance is greater than 20 megohms. The circuit under test is handled with latex gloves and placed in a pre-measured volume of isopropyl. The circuit is left in the circulating solution for 5 to 10 minutes and the resistance of the solution measured. If the resistance of solution per volume/area calculation falls below 20 megohms it is indicative of contamination. Areas of contamination other than flux is human oils and grease, soldering dross contamination and potentially solder paste removal chemicals if the board was printed and cleaned due to an error.

There is always a chance of contamination from the printed circuit board manufacturer; all high voltage boards should be spot-checked using an ionic tester. Contamination can be cleaned by using a reagent grade isopropyl alcohol and a scrub brush. All human body contact with high voltage boards should be avoided.

Solder balls remaining on the board after wave solder can also present a problem. The small tiny balls are very conductive and when placed within a high voltage field can result in the production of corona. An examination using a medium powered microscope of 20 to 30 power should be used to check for the presence of solder balls. They are removed with a light scrubbing with a soft brush and isopropyl alcohol.

Different types of solder mask and the manufacturing process used is the major associated problem with the production of solder balls. Harder, smoother, solder mask generates less solder balls, as does Kapton or HVPF cover coats. Talk to your board manufacturer to get the best solder mask he has.

Correct storage of the printed circuit board is essential. Use only sulfur free plastic bags wrapped tight and sealed to prevent moisture absorption. "First in- first out" type of inventory control is necessary, as circuit board material is like a sponge and will pick up a considerable amount of moisture in a very short time if left out unprotected. It is wise to store printed circuit boards in an environmentally controlled storage area. If you are going to pot the high voltage circuit after assembly it is therefore necessary to limit the possibility of moisture absorption during assembly by storing "work in progress" boards in a nitrogen chamber when they are not actually being worked on. Further moisture reduction before potting can be realized by the use of a vacuum chamber. The finished, cleaned boards are placed in the vacuum chamber for 24 hours before potting and only removed just before the actual potting operation. Boards do definitely have a best before solder life of no longer than one year if properly stored.

To further reduce any moisture in the printed circuit board a low temperature bake of 280°F for 4 to 8 hours will reduce the moisture without hurting the board.

The potting operation should be in an environmentally controlled, dust free room of at least class 10,000. Typically a plastic box or silicon mold is manufactured and the circuit placed into it with the proper spacers. A potting solution of silicon RTV or rubber is pored in with occasional bumps or bangs to remove any bubbles. After the case is filled it is transferred to a vacuum chamber and a low-pressure cycle is initiated to remove any remaining bubbles from the circuit. Some potting compounds need an oven cycle, as well as vacuum, which necessitates the need for an infrared vacuum oven. Some potting systems generate bubbles during curing, a high-pressure oven is used to force the bubbles back into the solution creating a more coherent cure.

It is essential to properly design the mixing of the potting solution process to obtain repeatable results. That does not mean mixing it in a paper cup by poring in a little of this and a little of that. Be scientific if you want repeatable results. I mention this after one employee figured he knew more then anyone else and mixed the potting solution his way. After repeated oven cycles the stuff would only cure to a semi hard state, and the circuits were garbage.

All potting material should be subject to an incoming inspection of date of manufacture, expiration date, package damage and correct part numbers.

Separate potting cabinets and mixing tools as well as air venting systems for silicon and rubber are required; silicon RTV potting solutions can contaminate the rubber solutions.

Some circuits for low-pressure use are sealed in an enclosure and a solution of pressurized oil and nitrogen are injected to create an artificial higher-pressure environment. This method keeps the circuit at a higher pressure in the vacuum of space where the arc over/corona voltage would be much lower.

For lower voltage circuits a simple sprayed on conformal coating may suffice. These coatings can double the effective voltage usable with low voltage use up to 2000 Volts. Again the circuit board must be clean, as well as the area, for best results.

There are many different types of conformal coatings, "corona dope" is an enamel paint like product that has been used in high voltage applications for years. Alternate clear acrylic spray-on paint can be used but their coating thickness is quite thin. Glyptal is one example of premixed commercial high voltage paints. Today many specialty products are made for conformal coatings, some of the best are made by Loctight. All conformal products require proper mixing and application, often involving spray equipment. It is very important to design and operate a safety spray booth with proper operator air supply and ventilation fans to the outside. Seek professional help in the design and operation.

One approach to reducing corona on wires in the assembled circuit or attachments to other devices, is to use a semiconducting wire with a greater radius. The greater radius of the conducting field reduces the effective voltage at which corona production starts. Wires manufactured by Belden, Canton and Rowe-Tally are among the better known suppliers.

Chapter 11

Outer Space Boards

Many potential problems face a printed circuit board in a spacecraft orbiting our world. The first problem to design around is vibration; at take off the G loading can exceed 10 Gs with many large instantaneous vibration peaks hitting 100Gs. The vibration is severe and constant for 5 to 10 minutes. A serious shaker table research program will be needed to properly ensure a large safety margin. Second, the wide variation in temperature extremes can be very detrimental to a printed circuit card and its components. Design parameters such as expected min and max temperature excursions as well as number of expected cycles need serious consideration. Most circuitry is protected with insulation and foils, however even then the temperature can vary widely.

Additional problems await the printed circuit in space, the vacuum will cause the board to continue expelling volatiles. These volatiles are accelerated by the high voltage plasma fields and can easily damage sensitive optical pieces or other parts of the craft.

When I made boards for outer space work, I selected the prepreg for maximum glass content to limit the amount of outgassing epoxy glue used. The material was also selected for minimum outgassing properties; I found BT epoxy one of the lowest while still having good process ability factors.

The cores and boards were processed through a special manufacturing process to remove the volatiles and significantly reduce out gassing. The boards are then sealed in vacuum packed sulfur free plastic and shipped.

One of the most significant problems facing today's space circuits is the destruction of the dielectric material from plasma and corona. As the spacecraft orbits the earth it cuts magnetic lines of force very quickly, generating very significant voltages on the spacecrafts skin and components.

Since plasma interactions generally result in vehicle surfaces charging negatively, an intense ion bombardment and sputtering of the metal results. Spacecraft surfaces usually consist of thermally controlled coatings that also serve as poor electrical conductors. The most common outer material is anodized aluminum, which is subject to dielectric breakdown. Anodized aluminum does not create an effective faraday shield to properly dissipate the large voltage potential generated by the spacecraft.

Because the aluminum skin allows a high voltage field to develop inside the spacecraft any high field points will generate a corona. If the voltage field is high enough, particles in the environment will be disrupted and possibly expelled with significant force and speed to penetrate components and damage the silicon chips. Several satellites have been lost this way during periods of extreme solar flares. The radiation generated by this large "E" field is significantly strong enough to cause particle type acceleration.

Special shielding and artificial atmosphere may be needed to control the field generated. As the pressure is lowered to 0 Torr levels voltage arc or corona is generated at a very low level of Volts/mil

The potential for an arc is catastrophic in a spacecraft; the large lightweight tanks of hydrogen and oxygen have a potential problem of modular leakage. This leakage, when combined with corona or an arc, can cause the spectacular destruction of the spacecraft.

N.A.S.A. has learned by many hours of detailed experiments and research, but also from hands on standard design practices developed over years of operation.

Power supplies in outer space of 100 Volts are considered high voltage with the potential to arc or corona due to the low atmospheric pressure and the plasma fields which may surround it.

If you are designing or manufacturing a circuit for space application I strongly suggest you spend time with the aerospace boys and girls to find out as much as you can about the expected environment and conditions.

All photographs taken by Robert Tarzwell.
All drawings by Robert Tarzwell.

