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Abstract—In many pulse power applications there is a trend to modulators based on semiconductor technology. For these modulators high voltage and high current semiconductor switches are required in order to achieve a high pulsed power. Therefore, often high power IGBT modules or IGCT devices are used.

Since these devices are based on bipolar technology the switching speed is limited and the switching losses are higher. In contrast to bipolar devices unipolar ones (e.g. SiC JFETs) basically offer a better switching performance. Moreover, these devices enable high blocking voltages in case large bandgap materials as SiC are used. At the moment SiC JFET devices with a blocking voltage of 1.5kV per JFET are available. Alternatively, the operating voltage could be increased by connecting N JFETs and a low voltage MOSFET in series resulting in a Super Cascode switch with a blocking voltage N -times higher than the blocking voltage of a single JFET. In order to evaluate the achievable switching speed of the Super Cascode and its applicability in solid state modulators, the performance of such a SiC switch is examined in this paper. Furthermore, the performance of the Super Cascode is compared with 4.5kV IGBTs made by Powerex, which are mounted in a special low inductive housing for minimising the rise and fall times.

I. INTRODUCTION

In many pulse power applications such as accelerators, medical radiation production/cancer treatment, or pulsed electrostatic precipitators there is a trend to modulators based on semiconductor technology due to higher reliability, longer life time and better controllable/variable pulse parameters as for example pulse length or turn off in case off a fault. In order to achieve a high pulsed power high voltage and high current semiconductor switching devices are required. Therefore, often high power IGBT modules or IGCT devices are used.

Since these devices are based on bipolar technology the switching speed is limited in principle and the switching losses are higher (e.g. tail current), what limits the pulse repetition rate and the converter efficiency and increases the costs for cooling. Part of the switching speed limitation is caused by the parasitic elements of the power module packing e.g. due to parasitic inductances as has been shown in [1], [2]. There, standard 4.5kV IGBT chips for traction applications are mounted in a special low inductive housing, which allows faster switching transitions due a better controllability of the gate.

In contrast to bipolar devices unipolar ones as e.g. SiC JFETs / MOSFETs basically offer a better switching performance. Moreover, these devices enable high blocking voltages in case large bandgap materials as for example SiC is utilised. At the moment SiC JFET devices with a blocking voltage of 1.5kV per JFET [4] and a switching speed in the range of tens of ns are available. In future the blocking voltage of the devices will increase in order to fully utilise the performance of the SiC material making these devices even more interesting for high voltage pulsed power application.

Alternatively, the operating voltage could be increased by connecting N JFETs and a low voltage MOSFET in series resulting in a Super Cascode switch with a blocking voltage N -times higher than the blocking voltage of a single JFET and the switching speed comparable to a single JFET. In order to

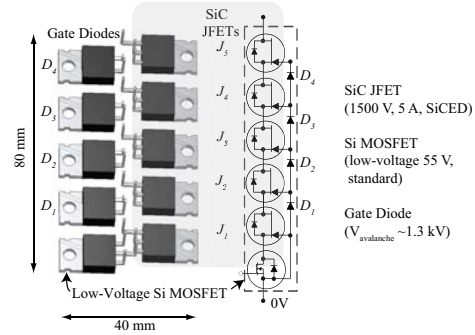


Figure 1: Schematic of the considered Super Cascode consisting of 5 series connected SiC JFETs and a Silicon low voltage MOSFET.

evaluate the achievable switching speed of the Super Cascode and its applicability in solid state modulators, the performance of such a SiC switch is examined in the following. In section II first the basic operating principle is explained shortly and the test platform for the SiC devices is presented. Thereafter, a test platform utilising low inductive 4.5kV IGBTs made by Powerex is presented in section III. This platform is used to evaluate the performance of the IGBTs in comparison to the SiC devices. Finally, measurement results for both devices are discussed in section IV.

II. SiC JFET SUPER CASCODE

The investigated SiC JFET Super Cascode [8] consists of a low voltage Silicon MOSFET and five 1.5kV SiC-JFETs, which are connected in series as shown in Fig. 1, so that a total blocking voltage of 7.5kV for the Super Cascode results. Due to the limited die size the current rating of the SiC-JFETs is limited to 5A for continuous operation at the moment. However, this will increase in future with improved manufacturing capabilities for SiC devices and growing SiC waver sizes. Presently, 40A devices are announced by SiCED. For balancing the voltage distribution 4 low power, avalanche rated Si-diodes with an avalanche voltage of approximately 1000V are required. Unfortunately, such diodes have not been available at the moment, so that diodes with an avalanche voltage of 1.3kV have been applied.

A. Basic Operation Principle

The Super Cascode is controlled via the gate of the MOSFET and for turning the switch on a positive gate voltage is applied to this gate. With a turned on MOSFET also the bottom JFET J_1 (cf. Fig. 1) is conducting, since its gate is connected to its source via the MOSFET, i.e. $V_{gs,J1} = 0$, and the JFET is a normally on device. Also the second JFET J_2 is conducting since the potential of the cathode of D_1 , which is connected to the gate of J_2 , could not be lower than the forward voltage drop V_F of D_1 and the source of J_2 is connected to 0V via J_1 and the MOSFET. Consequently, the gate voltage of J_2 must be higher than $-V_F$, which is above

the threshold voltage of J_2 ($V_{th} \approx -30V \dots -15V$), so that J_2 is definitely turned on. Due to a small leakage current through the balancing diodes, the potential of the cathode of D_1 is usually a bit above 0V resulting in a slightly positive gate voltage of JFET J_2 . The same is true in analog manner for the upper series connected JFETs.

For turning the cascaded switch off, first the MOSFET is turned off via its gate and the drain-source voltage of the MOSFET rises until the pinch-off voltage of J_1 is reached. Then, J_1 turns off and blocks the rising drain source voltage until the avalanche voltage of diode D_1 is reached. Due to the avalanche of diode D_1 the potential of the gate of J_2 does not rise any more. However, the source of J_2 continues to rise with the increasing drain-source voltage of J_1 , so that the gate source voltage of J_2 becomes negative and turns off as soon as its pinch-off voltage is reached. This sequential turn off continues with the next JFETs until the DC link voltage is reached.

Consequently, the static voltage distribution in the off-state (cf. Fig. 2) is mainly determined by the avalanche of diodes $D_1 \dots D_4$. For a controlled and stable avalanche, i.e. for a controlled static voltage distribution, a certain leakage current through the diodes is required [8]. In order to guarantee this leakage current independently of the JFET gate parameters, resistors must be connected between the gate and the source of the upper JFETs as shown in Fig. 3. There, the leakage current is mainly defined by the resistance value and the JFET's pinch off voltage, which is equal to the voltage drop across the resistor in the off-state [6]. Unfortunately, the pinch off voltage varies significantly ($\approx 15V \dots \approx 30V$) from JFET to JFET, so that a preselection of the JFETs is required for a stable operation of the Super Cascode. If in future the tolerances of the pinch off voltages are reduced by new JFET designs and improved manufacturing capabilities, this preselection will not be necessary any more.

By inserting the resistor also a kind of control loop of the voltage distribution in the off-state is initiated (cf. Fig. 3): In case for example J_4 tends to turn off a bit more, i.e. increasing its drain-source voltage, the leakage current through J_4 would decrease. With the reduced leakage current through J_4 also the current through resistor R_3 , which flows via the voltage balancing diodes to ground, would decrease if it is assumed that the leakage current through J_3 is constant. This results in a reduced voltage drop across resistor R_3 . Consequently, the gate-source voltage of J_4 decreases, so that J_4 is turning on a bit, which increases the leakage current through J_4 and stabilises the gate-source voltage as well as the drain-source voltage of J_4 . This control mechanism leads to a stable leakage current through the resistors and the diodes, so that the voltage sharing between the devices is stabilised by the avalanche voltage of the diodes, which determine the gate

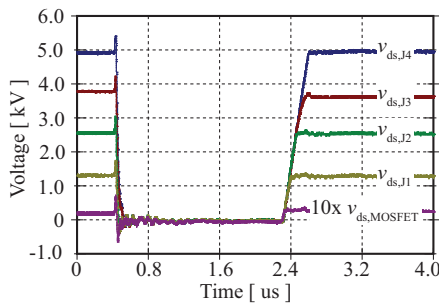


Figure 2: Voltage distribution across the JFETs of the Super Cascode caused by the avalanche voltage of the gate diodes.

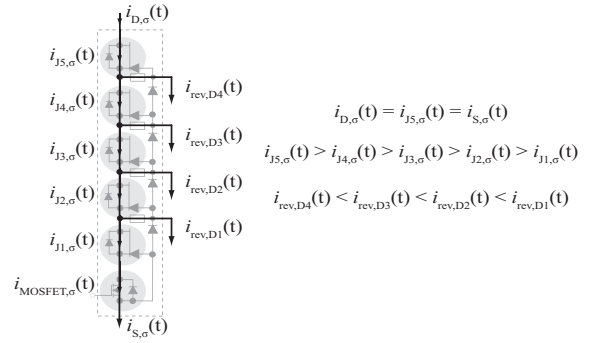


Figure 3: Leakage current distribution in the SiC HV Switch.

potentials of the JFETs.

The leakage current for the lower JFETs flows via the upper JFETs, so that the current in the JFETs decreases from the upper to the lower one and the current in the voltage balancing diodes increases from the upper to the lower one. With this leakage current distribution an operation could be achieved, where the lowest diode reaches its avalanche voltage first and therefore the blocking voltage is built up from the lower to the upper JFET. This also stabilises the turn off switching transition.

During switching process the inner potentials of the switches are changing dynamically and are mainly defined by the capacitances of the JFETs and diodes. In case no additional means except for the mentioned gate-source resistors are applied, oscillations in the gate-source voltage during the turn on could occur, which could lead to an unstable operation during the switching transition.

By inserting additional capacitors between the gate and the source connection of the upper JFETs (J_3, J_4, J_5) the oscillations could be significantly damped and a stable turn on transient could be achieved [6]. Due to the internal and the external capacitances it could be achieved that all JFETs turn on at the same time, if the MOSFET is turned on. There, it is important that the additional damping capacitances of the upper JFETs are not too big, since this would delay the turn on of these JFETs and their drain-source voltage would transiently rise above the static value, since the lower JFETs would turn on faster.

In Fig. 4 for example, the drain source voltage of 2 series connected JFETs during the turn on are shown. There, the parasitic capacitance of the voltage balancing diode has been varied. The larger this capacitance is, the more the turn transient of the two JFETs is synchronised, since the capacitors try to keep the voltage across the voltage balancing diodes

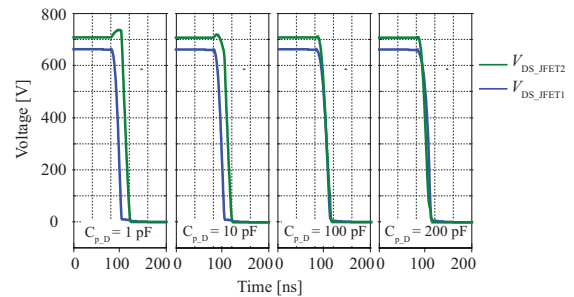


Figure 4: Drain-source voltage of two series connected JFETs during turn on in dependence on the capacitor $C_{p,D}$ parallel to the voltage balancing diodes.

constant during the turn on. This leads to rapidly increasing gate-source voltages of the JFETs as soon as the drain voltage of the JFET below starts to fall.

However, a too large parasitic capacitance of the voltage balancing diode could lead to unbalanced voltages during the turn off transient, since the capacitors try to keep the gate potentials of the JFETs at zero. This causes the upper JFET to turn off faster. Due to the rapid turn off, the leakage current in the JFET is rapidly decreasing and the parasitic capacitors of the lower voltage balancing diodes are only slowly charged. This effect could lead to a transient over-voltage of the upper JFET at turn off.

Consequently, it is very important to select of the components very carefully and to consider the parasitic effects/elements for achieving a stable and robust operation of the Super Cascode. The influence of other parasitics effects on the switching transients is part of the ongoing research.

B. SiC Test Platform

For investigating the switching behaviour of the Super Cascode in detail, a half bridge with two switches consisting of a MOSFET and 5 cascaded JFETs as shown in the schematic Fig. 5 has been designed (cf. Fig. 6). There, a standard 9A gate driver from IXYS is used to drive the MOSFET with a gate voltage of +18V/-5V. The gate signal is transferred via fibre optics and the gate power via a small HV transformer. For minimising the stray inductance of the setup ceramic capacitors mounted closely to the JFETs are applied besides the film capacitors. The load consisted of 10 series connected pulse resistors made by Vishay.

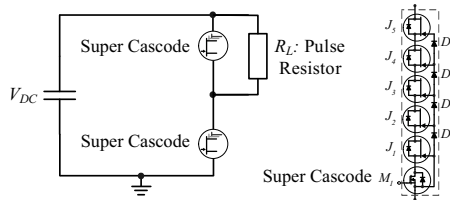


Figure 5: Schematic of the measurement setup for the SiC Super Cascode.

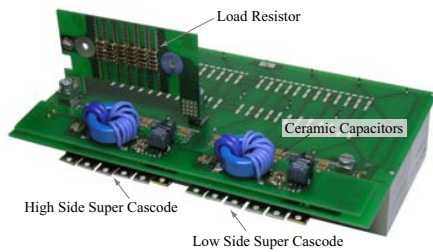


Figure 6: Photo of the measurement setup for the SiC Super Cascode. (Size: 155mm×170mm×50mm / Load: 90mm×50mm×5mm)

Table I: Components and system parameters of the test bench for the Super Cascode with a DC link voltage of 5kV.

SiC JFETs	1.5kV / 5A (TO220/SiCED)
Si-MOSFET	IRL3705 / 55V (TO220)
Balancing Diodes	BYT12PI1000 / 1000V (TO220)
Load Resistors	CMB0207 100Ω (Vishay)
DC-Link capacitor	ICEL 8μF/800V _{DC} (7×2) Syfer 500V/560nF/X7R (12×2)
Gate Driver	IXYS IXDI 9A / 35V
Pulsed Power	5kV × 5A = 25kW

For the voltage balancing diodes, which require a stable avalanche voltage in order to guarantee a well defined static and dynamic voltage distribution of the Super Cascode, fast recovery rectifier diodes made by STMicroelectronics are used. These diodes show a stable avalanche behaviour at 1.3kV. In order to reduce the voltage stress of the 1.5kV JFETs to lower values, diodes with an avalanche voltage of ≈ 1.0kV would be required. Unfortunately, such devices were not available at the moment.

III. 4.5kV IGBT WITH LOW INDUCTIVE PACKAGE

For comparing the switching performance of the new SiC JFET devices combined to a Super Cascode to conventional Si devices, a half bridge with QIS4506002 4.5kV IGBTs made by Powerex [2] has been designed and the switching performance has been measured.

The IGBT chips utilised in the QIS4506002 are basically the same as the ones used for traction applications, where large modules with parallel connected chips as e.g. the CM400HB-90H for high currents are applied. In these large modules, which usually are operated at relatively low switching frequencies in the range of a few kilohertz, internal gate resistors are used for balancing the current between the parallel connected chips, for synchronising the switching transients and for damping internal oscillations. These resistors form a low-pass filter in combination with the gate capacitance. This low-pass filter and the relatively large gate/emitter inductance due to the long bond wires from the external gate connection to the gate contact on the chip results in limitations of the minimal achievable rise and fall time.

In the QIS4506002 a single chip without internal gate resistor and very short bond wires is utilised [1], what allows to drive the gate more directly, which is especially interesting for pulsed power applications. This setup reveals the real performance of the HV-IGBTs.

In Fig. 7 a photo of the test bench for the 4.5kV IGBTs with low inductive housing is shown. Part of the DC link ca-

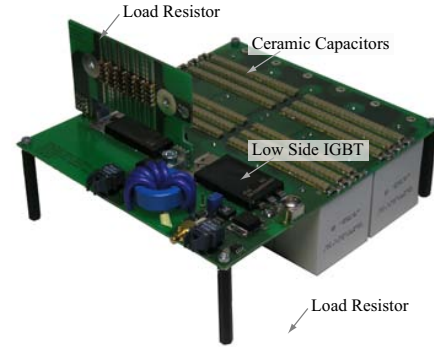


Figure 7: Photo of the prototype with the schematic shown in Fig. 5 utilising low inductive, 4.5kV IGBT made by Powerex. (Size: 155mm×170mm×50mm / Load: 90mm×50mm×5mm)

Table II: Components and system parameters of the test bench for the HV-IGBT with a DC link voltage of 2.5kV.

High Voltage IGBTs	QIS4506002 (Powerex)
Antiparallel-Diodes (TO220)	SiC 1.2kV/10A C2D10120 (Cree)
Load Resistors	CMB0207 100Ω (Vishay) (6×60)
DC-Link capacitor	Foil: 8.0μF / 400VAC (Icel) Ceramic: 630V/100nF (Murata)
Gate Driver	IXYS IXDI 430 / 35V / 30A
Pulsed Power	2.5kV × 250A = 625kW

capacitance is implemented by 630V/100nF ceramic capacitors (cf. Table II) mounted on top of the PCB close to the IGBTs in order to reduce the inductance of the half bridge. For the load the same SMD pulse resistors are used as for the Super Cascode. The gate driver is made of an IXDI 430 which could provide a maximal gate voltage of 35V and a maximal gate current of 30A. As freewheeling diodes four series connected 1.2kV/10A SiC diodes made by Cree are utilised.

IV. MEASUREMENTS

With the test benches for the Super Cascode and the 4.5kV IGBT presented in the preceding sections, measurements of the switch voltage and the load current for a purely resistive load have been performed. The maximal load current for the Super Cascode is limited to 5A due to the relatively small chips, which are available at the moment, and due to the unipolar device characteristic. This characteristic leads to a pinch off of the conducting channel as known from the MOSFET, if the current is too high.

In Fig. 8 the measurement results for the 4.5kV IGBT with a 10 Ω load resistance and a pulse voltage of 2.5kV is shown. The achieved fall time (90%-10%) of the load voltage is approximately 130ns and the rise time (10%-90%) is only 41ns. Similar times are obtained for the current waveform due to the low inductive setup. After the turn off approximately 12A tail current are flowing. The fast falling edge results due to the MOSFET channel of the IGBT, which is based on minority carriers. The generation of the majority carriers in the drift region due to the conductivity modulation [7] takes approximately 400ns. This can be clearly seen in the load current, which rapidly rises up to 225A and then, after some time, reaches its final value 250A. This effect is also visible in the collector-emitter voltage, that slowly decreases down to a few volts after the fast falling edge. Consequently, the IGBT is fully turned on just after 400-500ns. The more inductive the load is, the less critical is the turn on delay due to conductivity modulation, since the current rises not as fast as the voltage. However, in many applications as for example medical pulsed power systems the rise time and the pulse flatness is very critical. There, also the load is low inductive, so that the time for the conductivity modulation must be considered for determining the pulse parameters.

The results for the Super Cascode are shown in Fig. 9. The 90%-10% fall time of the voltage, which is double as high as the voltage of the IGBT, is 190ns and the rise time 200ns. The large rise time results due to the relatively low load current, which charges the output capacitor of the Super Cascode and the parasitic capacitors of the load. The turn-off waveform is determined by the RC time constant formed by the load

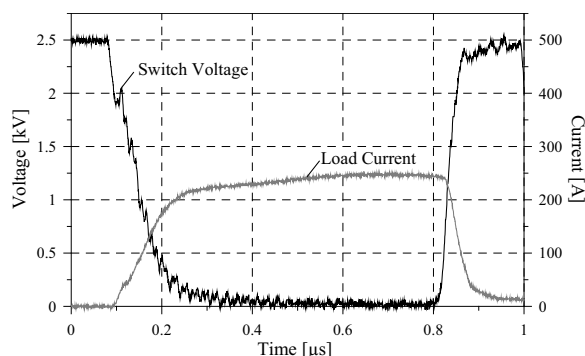


Figure 8: Measurement results for the HV-IGBT with a gate voltage of 18V and 10 Ω purely resistive load.

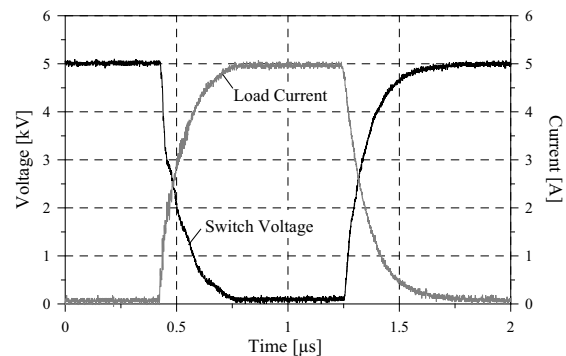


Figure 9: Measurement results for the Super Cascode with a gate voltage of 18V and 1k Ω purely resistive load.

resistor and the parasitic capacitors. The turn off time of the JFET is much shorter as could be seen in the linear voltage rise and its linear dependency from the load current presented in [6]. Consequently, the turn off losses are very low and can be neglected for limited load currents (ZVS-switching).

The turn on transients is very fast at the beginning and then slows down due to RC charging processes of the JFET gates in the Super Cascode. In the ongoing research means are investigated to decrease the turn on time, which is nevertheless significantly faster than the one if the IGBT.

V. CONCLUSION

In this paper the basic operating principle of a Super Cascode based on 1.5kV SiC JFETs and a low voltage Si-MOSFET is presented. There, also the requirement for additional gate-source resistors/capacitors for guaranteeing a stable voltage distribution and damping internal oscillations is explained. For evaluating the switching performance of the Super Cascode measurements for resistive load with a pulse voltage of 5kV and a load current of 5A have been performed. The rise time of the switch voltage is 200ns, which is caused by the relatively low load current charging the parasitic capacitors. The 90%-10% fall time is 190ns determined by internal RC charging processes. Means to decrease the fall time are part of the ongoing research.

For comparison also measurements for a 4.5kV IGBT with a low inductive package are presented. With the IGBT the rise time is 41ns and the fall time 126ns. However, it takes approximately 400ns until the IGBT is fully turned on and the conductivity modulation is finished. Compared to the IGBT the turn off losses of the JFET are very low (ZVS switching) due the tail current.

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