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EFFICIENT MODELING FOR SHORT CHANNEL MOS CIRCUIT SIMULATION

Mark Griffin Johnson

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Efficient Modeling for Short Channel MOS Circuit Simulation

by

Mark Griffin Johnson

Submitted to the Department of Electrical Engineering and Computer Science
on August 13, 1992 in partial fulfillment of the requirements for the
Degree of Master of Science

Abstract

Existing circuit models for short-channel MOS transistors represent a compromise between computation speed and ease of use. Empirical models are very fast to evaluate, but their parameters must be fitted from experimental measurements. Theoretical models require longer computation time, but they may be used to predict the performance of new, unmeasured MOS technologies since their parameters are not curve-fitted from experimental data.

This thesis combines the best features of both types of model, yielding a fast circuit simulator whose input parameters need not be extracted from experimental measurements. A nonlinear optimization algorithm is used to "compile" the parameters of a theoretical model into parameters for an empirical model, providing the superior user interface of theoretical models without sacrificing simulator execution speed. Results produced by a prototype model compiler are presented, showing the modeling error to be approximately 5 percent.

Thesis Supervisor: Stephen A. Ward

Title: Associate Professor of Computer Science and Engineering

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