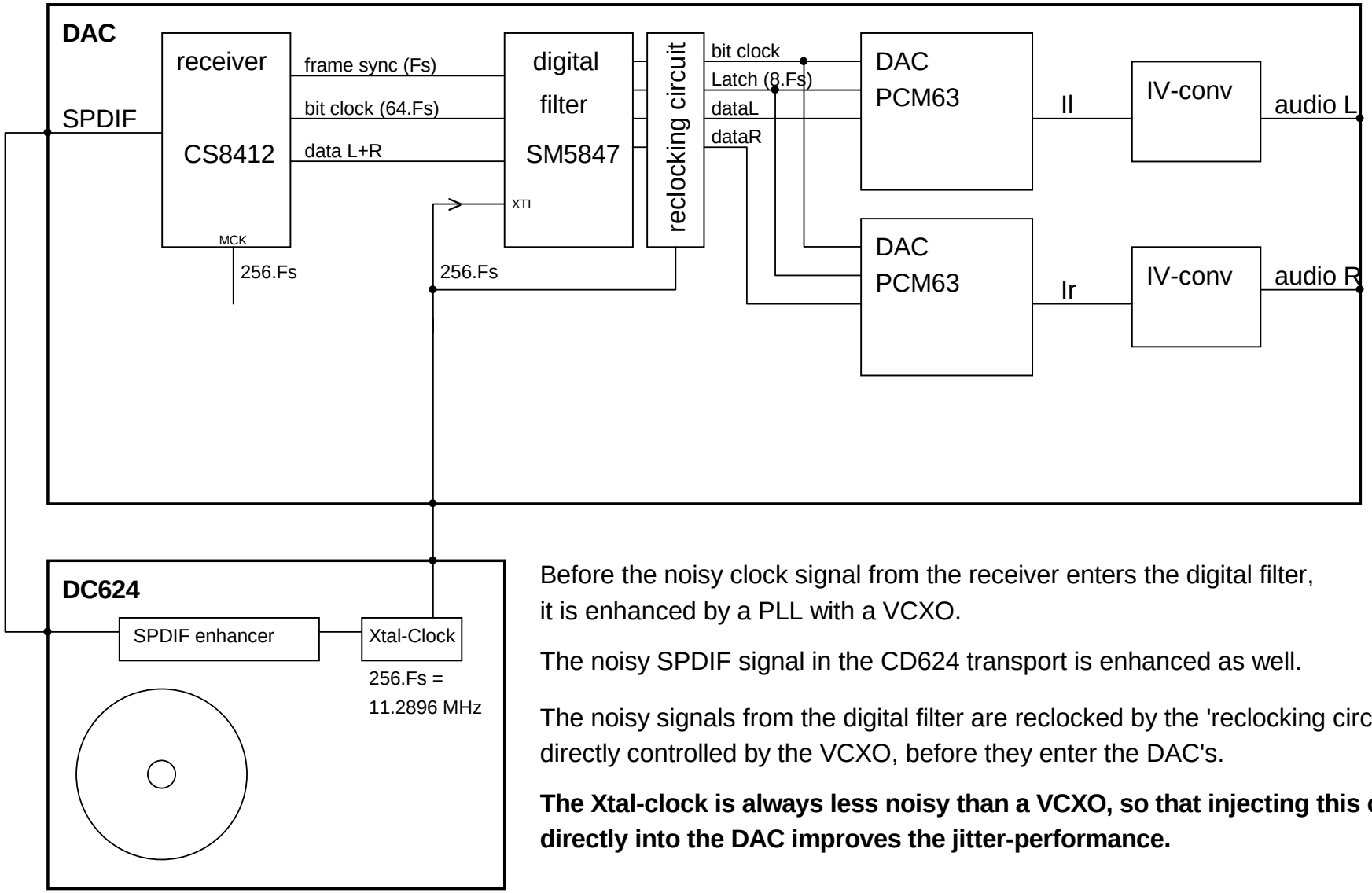

Before the noisy clock signal from the receiver enters the digital filter, it is enhanced by a PLL with a VCXO.

The noisy SPDIF signal in the CD624 transport is enhanced as well.

The noisy signals from the digital filter are reclocked by the 'reclocking circuit', directly controlled by the VCXO, before they enter the DAC's.

The Xtal-clock is always less noisy than a VCXO, so that injecting this clock directly into the DAC improves the jitter-performance.