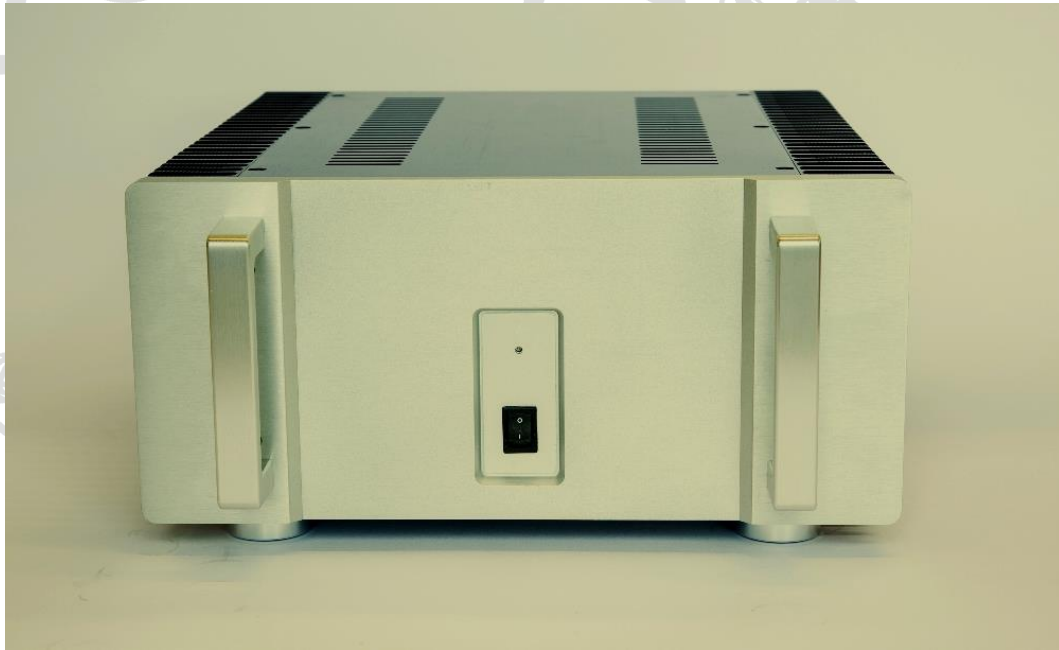


## GoFISS \* – Kaneda's Double Differential with Semisouth

XEN Audio

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### The Wild Goose Chase for SiC

Ever since Semisouth power JFETs have become obsolete, price has shot up, and people have gone crazy looking for alternatives <sup>[1]</sup>. Nelson Pass is now using only one Semisouth per channel in his First Watt J2, instead of 2 in earlier examples.

Numerous circuit designers are also boosting new designs, with emphasis on the use of SiC power devices. But there are no real benefits of these new breeds of SiC FETs. These new SiC devices are mostly designed for high voltage switching applications, such as in solar panels, and not for analogue amplification. They can survive well over 1kV, which is seldom needed in audio, other than electrostatic panels. While the SiC substrate can sustain high temperature, the diffusion layer cannot. And devices are still rated at 150°C, as normal Si-FETs. Even Nelson has not been too impressed by these currently active SiC devices <sup>[2,3]</sup>.

But what makes Semisouth so special ?

Different from other SiC or Si MOSFETs, the popular SJEP120R100 has, for example, high  $Y_{fs}$  (~7s at 1.2A), quite low  $V_{gs}$  (can be advantage or disadvantage), but more importantly very low tempco. These have not been seen in the more recent SiC devices. The thermal resistance  $R_{thjc}$  is comparable to normal TO247 power MOSFETs but not better. It does have high capacitances at low voltages, and is known to have gate leakage, requiring low impedance drivers.

### Semisouth, what else other than J2

One of the most prolific publisher of amplifier circuits using SiC MOSFETs, other than Nelson, is Akihiko Kaneda (金田明彦). Kaneda is not only well known and popular in Japan, but also in France,

thanks to Jean Hiraga's admiration and promotion of his work at L'Audiophile <sup>[4,5]</sup>. The "complete symmetry" topology that he has been using for decades <sup>[6]</sup> is essentially a double differential voltage amplifier front end, with various favours of output stages, quite similar to the JC-2 Phono Preamp or Pro-1 module <sup>[7,8]</sup>. His recent power amplifier circuits based on SiC output devices uses a quasi-push-pull output stage, where only NMOS devices are needed <sup>[9]</sup>. This is also found in the well-known John Linsley Hood Class A, where a matched pair of power devices can be driven in anti-phase for distortion cancellation. In the Kaneda, the output-FET gate-biasing resistor is part of the second differential gain stage. Thus, a higher-value biasing resistor at lower bias current can be used to increase open loop gain, and vice versa.

Earlier, we published an analysis of the gain structure of one of the Kaneda SiC power amplifiers <sup>[10]</sup>. This is quite different from e.g. the J2, in that most of the open loop gain is provided by the first 2 stages, as the Rohn SiC devices used have rather low transconductance. So the question is, what would he have done if he had Semisouth's to his disposal ?

A few years back, we offered curve-tracer-matched SJEP120R100s from a batch of 500 devices <sup>[11]</sup>. Many people subscribed for them, but quite a number did not pay or even bother to inform us. Thanks to them, we have quite a few sets of well-matched quads and twin-pairs. It is too much of a waste to split them into pairs for J2 builders. They should find applications where a matched pair should be applied, in some symmetrical push-pull circuits. So a Kaneda power amplifier using Semisouth's for the output stage is an ideal candidate.

## Design Parameters

The Kaneda topology is well established and widely published. The design choices are therefore down to specific details.

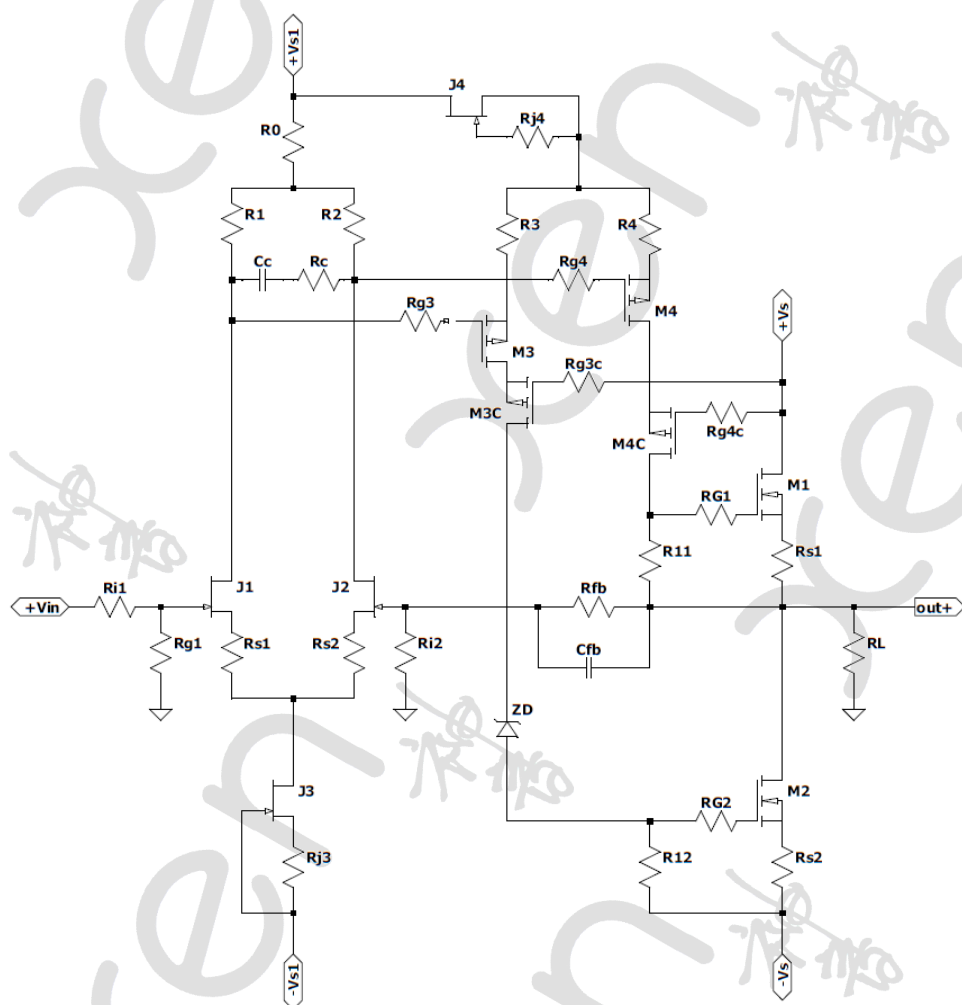
The following design goals were set upfront :

- Minimal source degeneration, just enough for zero tempco, slightly negative for safety
- 30dB closed loop gain
- ~35dB NFB; open loop gain ~65dB into 8R
- Open loop bandwidth into 8R ~10kHz
- Separate frontend supplies for maximum output swing.
- Can be optimised for 4R with lower rails and higher bias of the output stage.

The circuit we proposed is described below.

Ri1 & Rgi isolate the source from the input stage. Ri2, Rfb and Cfb form the feedback network with bandwidth limiting. J1,2 are a matched pair of N-JFETs forming the input differential pair. Rs1,2 allow for DC offset trimming. R1,2 sets the input stage gain, and R0 provides additional voltage headroom for the second stage. J3 is a 8mA CCS for the input stage, with its current adjustable via Rj3.

The second stage is designed to work with a high bias of 24mA, such that any gate leakage of the Semisouth's can be swamped. As such a pair of TO220 P-MOSFETs M3,4 are chosen for the differential pair. The CCS JFET J4 sees a relatively low Vds, and the dissipation is still within reach of a TO92 devices, allowing low-noise devices to be used. The value of R11,12 is determined by the Vgs of M1,2 as well as voltage across the source resistors. ZD is there to balance the voltage as seen by M3c and M4c, as well as to equalise their dissipation. These cascode devices M3c, M4c are necessary to reduce the difference in Miller capacitances between the two legs to retain "complete symmetry" as much as possible.

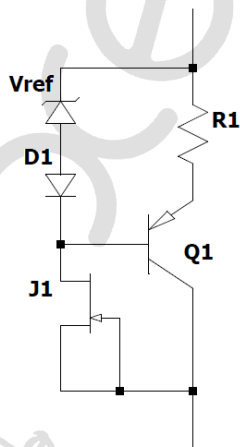


Note that long-tail JFETs such as J111 or J112 have a very high negative tempco at such current values, i.e., the CCS current drops significantly as they warm up. The result is a drop in output stage bias by more than 50% at 30°C temperature rise. The 2SK369V proves to be a better choice in this respect, in addition to having lower noise. But 24mA  $I_{dss}$  is hard to find even for V-grade. So it is still desirable to find another alternative CCS that is thermally stable.

A bipolar transistor has a  $V_{be}$  drift of  $-2\text{mV}/^\circ\text{C}$ , and this can be compensated largely by a small signal diode thermally coupled to it. The CCS is designed with a voltage headroom of  $\sim 6\text{V}$ . The current can be set using a resistor at the emitter, and a voltage reference + a diode at the base, both connected to the top rail at their free ends. For example, an ADR512 has a  $V_{ref}$  of 1.2V and very low noise of  $4\mu\text{V}$  pk-pk. A 50R resistor will conveniently give 24mA. The tempco of the ADR512 is 60ppm/K. That is a change of 3mV for 40°C temperature rise, or 0.24%.

A circuit for the CCS can look like that shown below. The PNP BJT should of course also be a low noise device, but it should also be able to dissipate 150mW at elevated temperature. What better to use than ZTX951, not only because of lowest noise, but also good power rating and a low  $R_{thjc}$ . That means it is better to thermally couple this directly onto the main amplifier heatsink, than to leave it in "free" air inside the amplifier enclosure. A through-hole 1N4148 can be glued to the PNP with thermal adhesive. The ADR512 needs only 0.2mA bias, so that a 2SK208Y can be used as biasing CCS for

best ripple rejection. Alternatively, a 3K thin-film resistor can also be used. Total cost is about the same as a 2SK369V in the end, but at least it is easy to find, and the current is freely adjustable.



A prototype was built and tested before including in the amplifier circuit. The dynamic impedance is about 100kohm, and the temperature coefficient is about  $-6\mu\text{A}/^\circ\text{C}$ , or 240ppm/K. With a heatsink temperature of  $30^\circ\text{C}$  above ambient, the Semisouth's bias will now only reduce by approximately 40mA, or 3%.

As in the J2, the gain of the output stage is load dependent, as it is transconductant in open loop. The two output devices act as push-pull current sources, as in the J2 and the JLH Class A. But different from the J2, where the upper MOSFET delivers an anti-phase current by sensing that of the Semisouth (and therefore including the distortion of the latter), those in the Kaneda are driven in anti-phase by the 2<sup>nd</sup> stage LTP, resulting in better even-harmonic distortion cancellation. In this respect, the Kaneda is similar to the JLH Class A where the output devices are also driven in antiphase by the 2nd stage phase splitter.

The output source resistors are there to provide some bias stabilisation. The SJEP120R100 has a low tempco, but it is still slightly positive. Experiments were carried out first to see what value of  $R_s$  is needed to keep bias current constant with increasing heatsink temperature. The result shows that  $0.1R$  is sufficient; the bias current reduces slightly with temperature, to be on the safe side.

With 24V rails and 1.3A bias, the output stage can deliver 27W into 8R in pure Class A, and only clips at above 36W. If one wishes to optimise for 4R load, one can change the rails to 18V and bias to 1.8A to deliver 25W Class A power.

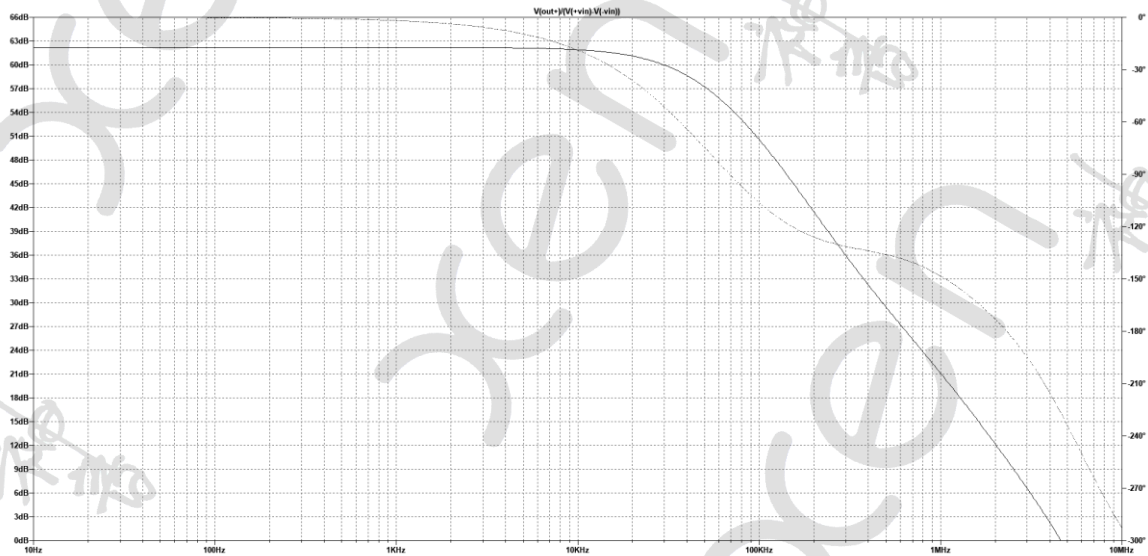
The frontend positive rail should be 15V above the output stage for symmetrical clipping. The frontend negative rail does not need to be much more than -12V, as it only needs to provide some voltage headroom for J3. So it makes sense to use separate power supplies for the frontend and the output stage, as shown above.

## Gain Structure

As mentioned above, the open loop gain (OLG) and hence the amount of negative feedback (NFB) is load dependent. Frontend Gain is about 11, given by drain resistor divided by the effective source resistance. Similarly, the 2nd Stage Gain is about 2. And with 8R load, the gain of the output stage is 64. Total OLG is therefore  $\sim 1400$ , resulting in  $\sim 34\text{dB}$  of NFB. With 4R load, this reduces to 28dB, which is still very acceptable.

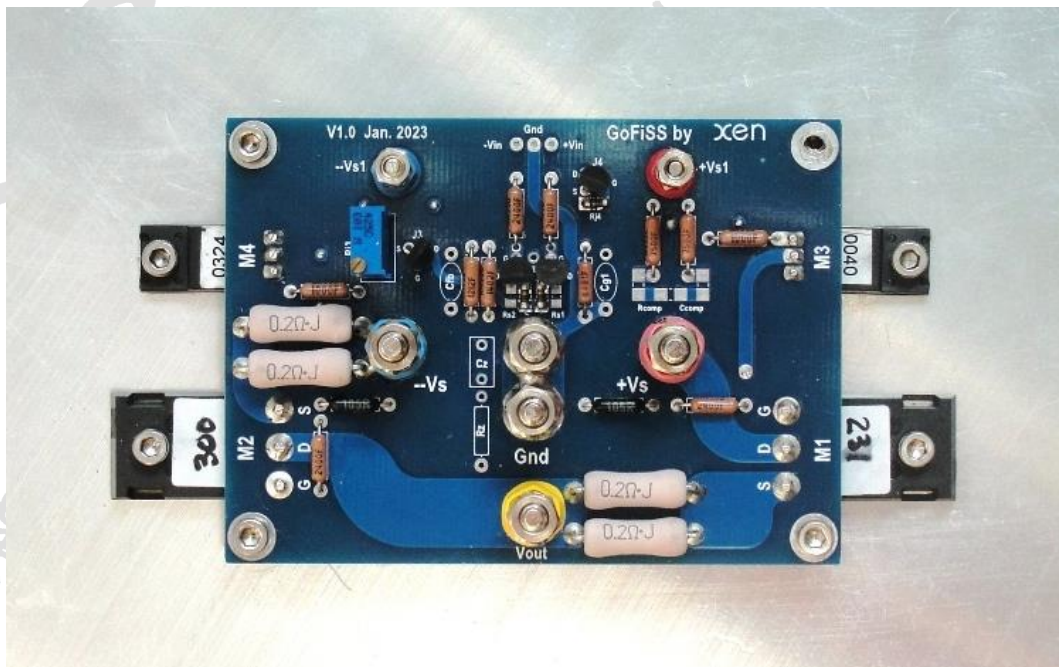
How does that compare with the J2 ?

In the J2, the frontend Gain is  $\sim 6$ , and the OPS gain the same at 64 into 8R. That gives an OLG of 384. But because the CLG is only 10, NFB is 38.4, or 32dB. Very similar.



**Simulated Open Loop Response of the GoFiSS**

## PCB layout



The PCB layout is a natural evolution from that of the J2 clone, with the second differential stage added. The power devices are designed to be some 120mm apart, so that they can make use of the width of the heatsink, and yet are not too far from each other to allow good thermal tracking and minimum DC drift. We always prefer not to use trimpots, so pads are provided for SMD thin-film resistors to replace them after trimming.

The circuit allows separate trimming of output bias (via 2<sup>nd</sup> stage CCS current) and DC offset (via Rs1,2), so adjustment is quite convenient. As in our J2 PCB, M4 brass standoffs are used for power and output wiring for the output stage, whereas the input stage has additional M3 standoffs for power connection. An additional daughter board is designed to stack onto these standoffs, to allow connection of local caps for all 4 rails.

The PCB is equipped with provisions for Zobel networks at the input differential stage, and at the output often found in other Kaneda circuit variants. The PCB can thus also be used for various Kaneda circuits based on the same topology and pin assignments, including those using bipolar transistors.

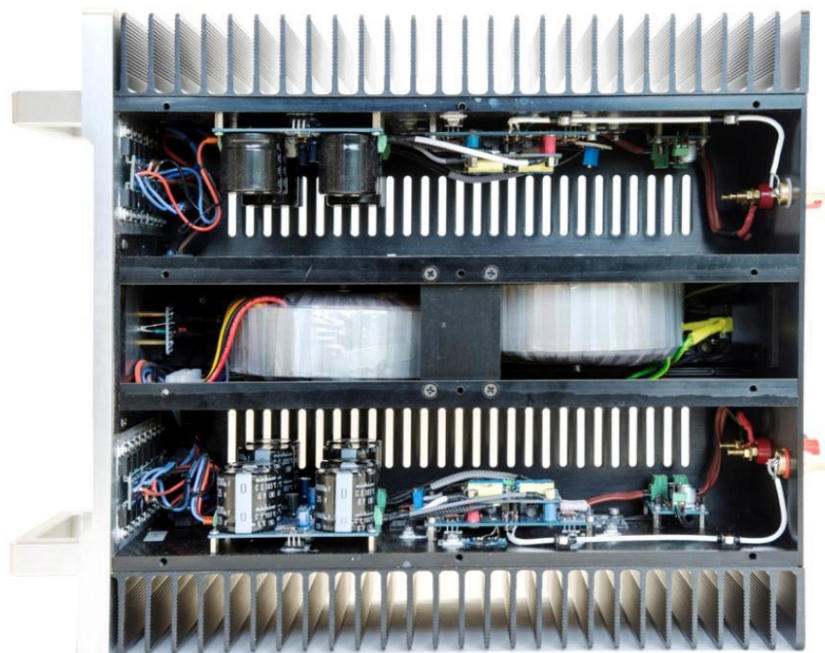
### Alternative Power Devices to Semisouth

As already mentioned in the J2 thread, the Toshiba 2SK3497 has similar Yfs as SJEP120R100, but it has high tempco, making extra bias stabilisation essential. 2SK1530 is another good alternative, and can achieve similar levels of distortion.

The easily available IRFP240 has much higher Vgs and hence R11,12 have to be increased in value. This in turn increases second stage gain by more than 10dB, but output stage gain decreases, due to lower Yfs and larger source resistors required for thermal stability. The two more or less compensate each other. Clipping will occur earlier due to the high Vgs.

### Case Layout

We like the case and the layout of our J2 clone<sup>[12]</sup>. So there is no reason to change. But this time we went for 2x custom transformers in dual mono, for even better channel separation. As a result of the different voltages, separate C-Reg-C boards are provided for output stage and frontend. Our latest version of Simple Speaker Protection<sup>[13]</sup> with power-up delay is also used here, powered by the output stage PSU.

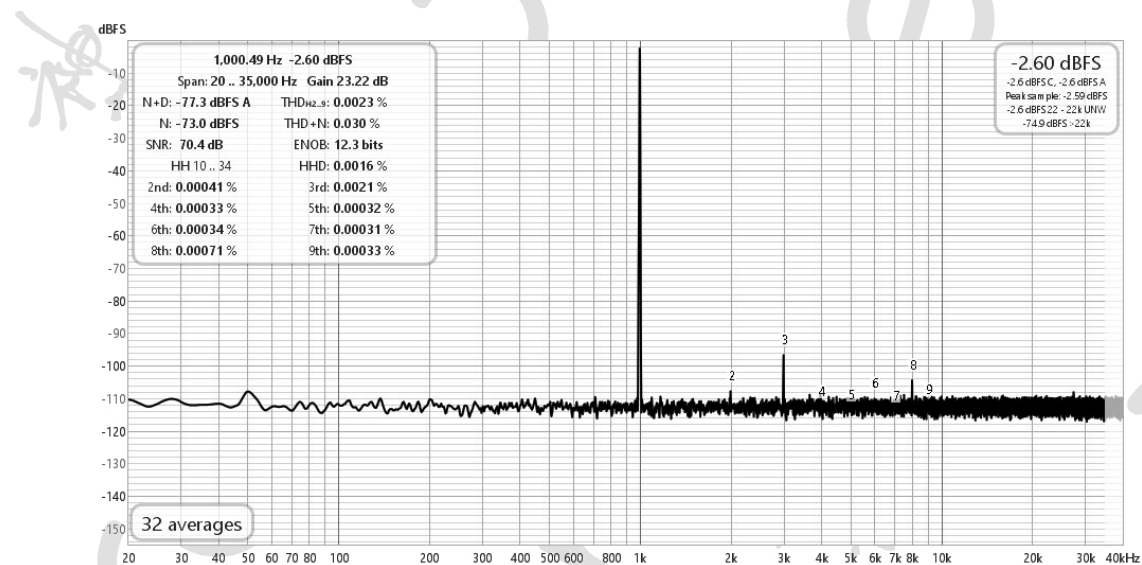


## Measurements

The prototype works first time as expected. Even without any trimming, bias was quite stable, settling at 1.3A at 60°C heatsink temperature. DC offset is 26mV at cold start, drifting to -8mV at 60°C. And that without DC trimming.

Frequency response is ~100kHz -3dB as intended by design, to ensure sufficient stability margin even when driving capacitive load. Due to the huge increase in OLG when the output is not loaded, it is advisable to include a larger-value output resistor, or a Zobel network, to prevent unintended oscillations.

The distortion spectrum for 1W into 8R at 1kHz is shown below :



As one would expect from a fully symmetrical circuit, even harmonics are well cancelled. But this appears to drift somewhat with time. Although all devices are very well matched, the tiny difference in leakage gate current of the two Semisouth's is sufficient to tip it out of symmetry. If so desired, H2 can be trimmed most conveniently by adding a metal film resistor in parallel with the Semisouth source resistors. A distortion analyser is necessary, and the amplifier should be loaded with 8R power resistors during the process.

\* Note – GoFiSS is abbreviation for Gold Field Semisouth. Gold Field is the direct translation (by meaning) of the Japanese word Kaneda.

## References

1. <https://www.diyaudio.com/community/threads/semisouth-goes-dodo-what-now.222098/>
2. <https://www.diyaudio.com/community/threads/semisouth-goes-dodo-what-now.222098/post-7133888>
3. <https://www.diyaudio.com/community/threads/f2j-jig-using-depletion-mode-jfets.394061/post-7224707>
4. <http://dcamp.biz/?p=597>
5. <http://6bm8.lab.free.fr/Documentations/Revue/Audiophile/1977-1988/29/KANEDA/KANEDA.html>
6. <https://www.diyaudio.com/community/threads/kaneda-preamp.10243/post-116710>
7. <http://www.amplimos.it/images/jc-2%20schematic.gif>
8. <https://www.diyaudio.com/community/threads/john-curls-blowtorch-preamplifier-part-ii.146693/post-4938034>
9. <https://www.diyaudio.com/community/threads/semisouth-goes-dodo-what-now.222098/page-18#post-7233757>
10. <https://www.diyaudio.com/community/threads/narsis-kaneda-mosfet-amp-built.416094/post-7767931>
11. <https://www.diyaudio.com/community/threads/interest-for-genuine-semisouth-sjep120r100-curve-tracer-matched-pairs-quads.330916/>
12. <https://www.diyaudio.com/community/threads/firstwatt-j2.151909/post-5999278>
13. <https://www.diyaudio.com/community/threads/group-buy-very-simple-almost-universal-speaker-protection.426224/>