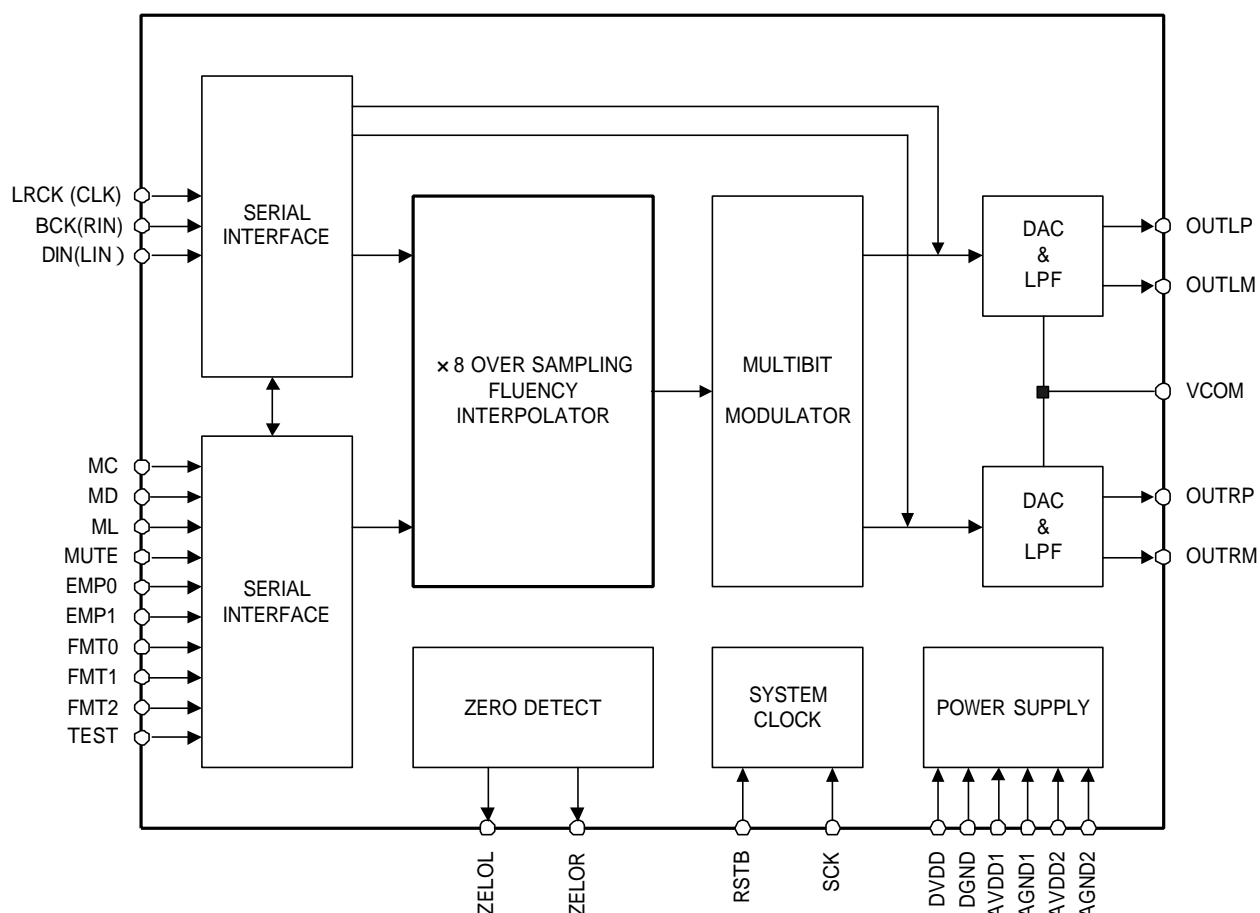


D/A converter

MODEL FN1242

Note: Specifications contained here are tentative.
Functions and pin layout are subject to changes.

Block diagram



Pin Layout

28 Pin SSOP

EMPH0	1	28	TEST
EMPH1	2	27	ZEROL
ML	3	26	OUTLP
MD	4	25	OUTLM
MC	5	24	AVDD1
SCK	6	23	AGND1
DVDD	7	22	VCOM
DGND	8	21	AGND2
BCK(DIR)	9	20	AVDD2
DIN(DIL)	10	19	OUTRM
LRCK(CLK)	11	18	OUTRP
FMT0	12	17	ZEROR
FMT1	13	16	MUTE
FMT2	14	15	RSTB

Terminals

Pin No.	Pin Name	I/O	Function
1	EMPH0	IN	De-emphasis Filter Select. EMPH1,0 = 0 : 32kHz 1 : 44.1kHz 2 : 48kHz 3 : De-emphasis OFF
2	EMPH1	IN	
3	ML	IN	
4	MD	IN	
5	MC	IN	Function control clock
6	SCK	IN	System clock
7	DVDD	-	Digital power supply (3.3V)
8	DGND	-	Digital ground
9	BCK (DIR)	IN	Bit clock . Rch data (DIR) input when formatting DSD
10	DIN(DIL)	IN	Audio data. Lch data (DIL) input when formatting DSD
11	LRCK(CLK)	IN	L/R clock input . Data clock (CLK) input when formatting DSD
12	FMT0	IN	Input Data Format Select. FMT2, 1, 0 = 0 : 16bit MSB first right-justified 1 : Reserve (unused) 2 : 20bit MSB first right-justified 3 : 24bit MSB first right-justified 4 : DSD format 5 : 16,20,24bit MSB first left-justified 6 : 16,20,24bit ISS format 7 : Reserve (unused)
13	FMT1	IN	
14	FMT2	IN	
15	RSTB	IN	
16	MUTE	IN	Reset input.
17	ZEROR	OUT	Soft Mute input
18	OUTRP	OUT	R channel zero data detection output
19	OUTRM	OUT	R-ch analog audio output +
20	AVDD2	-	R-ch analog audio output -
21	AGND2	-	R-ch analog power supply (5V)
22	VCOM	-	R-ch analog ground
23	AGND1	-	Analog common de-coupling terminal
24	AVDD1	-	L-ch analog ground
25	OUTLM	OUT	L-ch analog power supply (5V)
26	OUTLP	OUT	Lch analog audio output -
27	ZEROL	OUT	Lch analog audio output +
28	TEST	IN	L channel zero data detection output
			Test terminal (connect to DGND)

Electrical characteristics

- Absolute maximum ratings (Ta=25 , DGND = AGND1 = AGND2 = 0V)

Item	Symbol	Ratings	UNIT
Power supply voltage	DVDD	-0.3 ~ 4.0	V
	AVDDR , AVDDL	-0.3 ~ 6.5	V
Input voltage	V _I	-0.2 ~ DVDD + 0.3	V
Output voltage	V _O	-0.2 ~ DVDD + 0.3	V
		-0.2 ~ AVDD + 0.3	
Storage Temperature	Tstg	-55 ~ +125	

Note: Absolute maximum ratings is the highest value which doesn't harm the chip.

It doesn't guarantee normal function.

- Recommended operational conditions

Item	Symbol	MIN	TYP	MAX	UNIT
Power supply voltage	DVDD	3.0	3.3	3.6	V
	AVDD1 ,AVDD2	3.0	5.0	5.5	V
Operating Temperature	Ta	-25	-	+85	

- Analog characteristics (fs=44.1 kHz)

Unless otherwise specified, Ta=25 , AVDD1=AVDD2=5V, DVDD=3.3V, SYSCLK=384 fs
24-bit data, Signal = 1KHz, Measuring range 10KHz ~ 20KHz

	Item		Condition	MIN	TYP	MAX	UNIT
1	Resolution				24	-	Bits
2	Dynamic characteristics	THD+N	Vo= 0dB	-	0.004	-	%
			Vo=-60dB	-		-	%
		Dynamic range	Vo=-60dB, EIAJ A	-	100	-	dB
		S/N ratio	EIAJ A	-	100	-	dB
		Channel separation	1 kHz	-	100	-	dB
3	DC characteristics	Gain Error		-	± 1.0	± 5.0	%ofFSR
		Inter Channel Gain Mismatch		-	± 1.0	± 5.0	%ofFSR
		Zero Error		-	± 50	± 60	mV
4	Analog output	Output voltage		-	0.6 × AVVD	-	Vp-p
		Center voltage		-	0.5 × AVDD	-	V
		Load resistance		5	-	-	k
5	Analog filter	-3dB bandwidth		-	100	-	kHz
		Frequency characteristics	20 kHz	-	-0.1	-	dB
6	Power supply	Current of DVDD	f=1kHz/ 0dB	-	9	-	mA
		Current of AVDD	f=1kHz/ 0dB	-	14	-	mA

• Analog characteristics (fs=96 kHz)

Unless otherwise specified, Ta=25°, AVDD1=AVDD2=5V, DVDD=3.3V, SYSCLK=384 fs
24-bit data, Signal = 1KHz, Measuring range 10KHz ~ 20KHz

	Item	Condition	MIN	TYP	MAX	UNIT
1	Resolution			24	-	Bits
2	Dynamic characteristics	THD+N	Vo= 0dB	0.004	-	%
			Vo=-60dB		-	%
		Dynamic range	Vo=-60dB, EIAJ A	100	-	dB
		S/N ratio	EIAJ A	100	-	dB
		Channel separation	1kHz	100	-	dB
3	DC characteristics	Gain Error		± 1.0	± 5.0	%ofFSR
		Inter Channel Gain Mismatch		± 1.0	± 5.0	%ofFSR
		Zero Error		± 50	± 60	mV
4	Analog output	Output voltage		0.6 × AVDD	-	Vp-p
		Center voltage		0.5 × AVDD	-	V
		Load resistance	5	-	-	k
5	Analog filter	-3dB bandwidth		100	-	kHz
		Frequency characteristics	20 kHz	-0.1	-	dB
6	Power supply	Current of DVDD		9	-	mA
		Current of AVDD		14	-	mA

• Analog characteristics (fs=192 kHz)

Unless otherwise specified, Ta=25°, AVDD1=AVDD2=5V, DVDD=3.3V, SYSCLK=384 fs
24-bit data, Signal = 1KHz, Measuring range 10KHz ~ 20KHz

	Item	Condition	MIN	TYP	MAX	UNIT
1	Resolution			24	-	Bits
2	Dynamic characteristics	THD+N	Vo= 0dB	0.004	-	%
			Vo=-60dB		-	%
		Dynamic range	Vo=-60dB, EIAJ A	100	-	dB
		S/N ratio	EIAJ A	100	-	dB
		Channel separation	1kHz	100	-	dB
3	DC characteristics	Gain Error		± 1.0	± 5.0	%ofFSR
		Inter Channel Gain Mismatch		± 1.0	± 5.0	%ofFSR
		Zero Error		± 50	± 60	mV
4	Analog output	Output voltage		0.6 × AVDD	-	Vp-p
		Center voltage		0.5 × AVDD	-	V
		Load resistance	5	-	-	k
5	Analog filter	-3dB bandwidth		100	-	kHz
		Frequency characteristics	20 kHz	-0.1	-	dB
6	Power supply	Current of DVDD		9	-	mA
		Current of AVDD		14	-	mA

• Digital filter characteristics

	Item	Condition	MIN	TYP	MAX	単位
1	Pass Band	-3dB	-	0.42fs	-	-
		-6dB	-	0.51fs	-	-
2	Passband Ripple		-	0	-	dB

• De-emphasis filter characteristics

Item	Symbol	MIN	TYP	MAX	UNIT
De-emphasis error	fs=44.1 kHz	-0.1	-	+0.4	dB
Group Delay		-	2/fs	-	sec

• DC characteristics

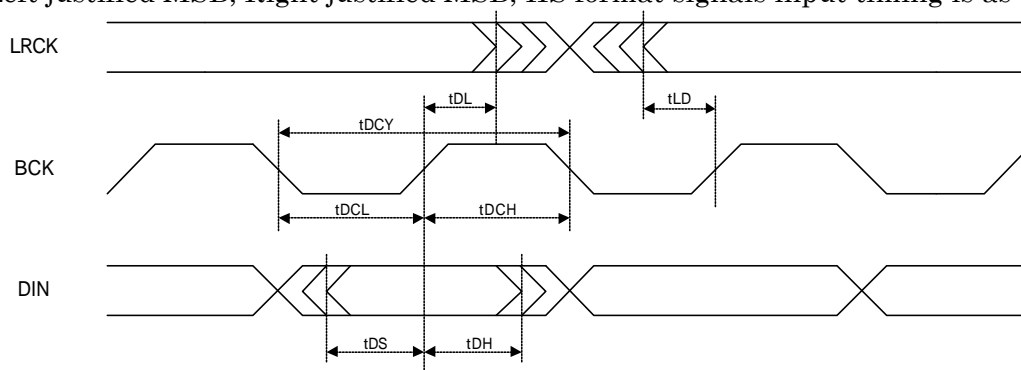
Item	Symbol	MIN	TYP	MAX	UNIT
Input logic level (High)	VIH	$0.7 \times \text{DVDD}$	-	DVDD	V
Input logic level (Low)	VIL	0	-	$0.3 \times \text{DVDD}$	V
Output logic level (High)	VOH	DVDD-0.6	-	-	V
Output logic level (Low)	VOL	-	-	0.4	V

• AC characteristics

Item	Symbol	MIN	TYP	MAX	UNIT
Sampling frequency	fs	10	44.1	200	kHz
System clock frequency	fsck	-	-	40	MHz

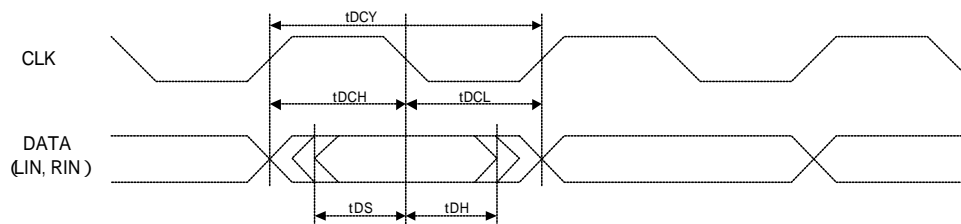
• Signals input timing

Left justified MSB, Right justified MSB, IIS format signals input timing is as below.



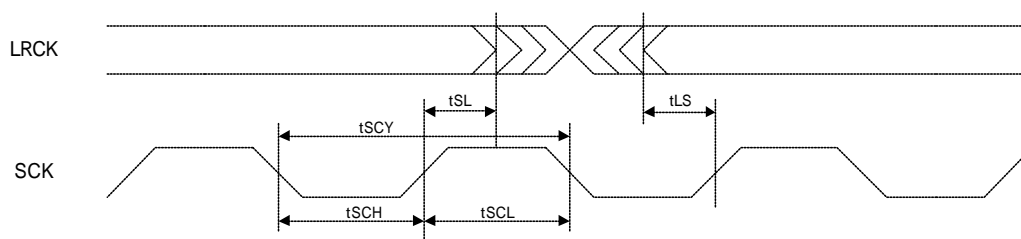
Item	Symbol	MIN	TYP	MAX	UNIT
BCK pulse cycle	tDCY	70	-	-	ns
BCK pulse width "H" level	tDCH	35	-	-	ns
BCK pulse width "L" level	tDCL	35	-	-	ns
BCK rise LRCK edge	tDL	10	-	-	ns
LRCK edge BCK rise	tLD	10	-	-	ns
DIN setup time	tDS	10	-	-	ns
DIN hold time	tDH	10	-	-	ns

- DSD format signals input timing



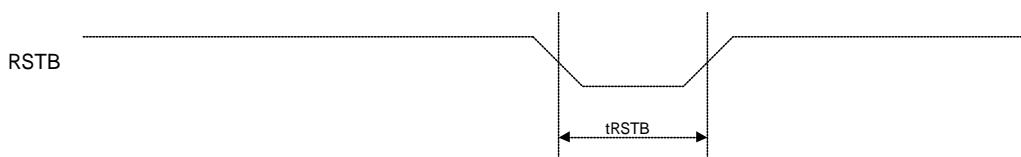
Item	Symbol	MIN	TYP	MAX	UNIT
CLK cycle	tDCY	1.0	-	3.2	MHz
CLK pulse width "H" level	tDCH	20	-	-	ns
CLK pulse width "L" level	tDCL	20	-	-	ns
DATA setup time	tDS	20	-	-	ns
DATA hold time	tDH	20	-	-	ns

- LRCK-SCK Timing



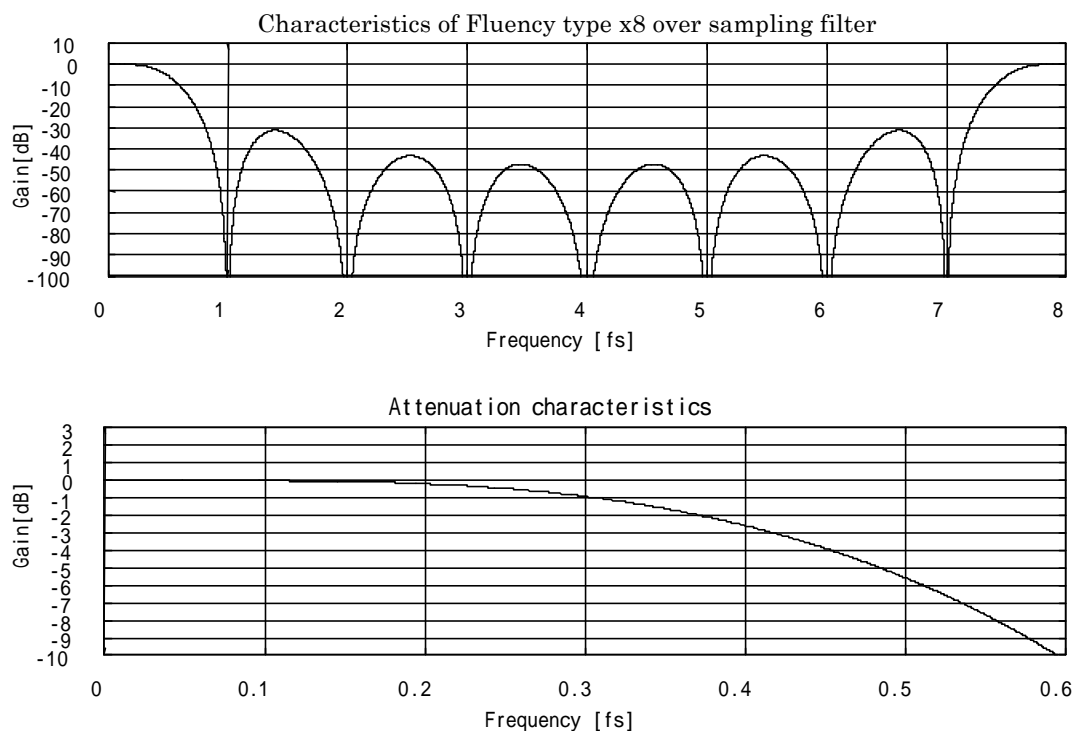
Item	Symbol	MIN	TYP	MAX	UNIT
SCK pulse cycle	tSCY	20	-	-	ns
SCK pulse width "H" level	tSCH	10	-	-	ns
SCK pulse width "L" level	tSCL	10	-	-	ns
SCK rise -> LRCK edge	tSL	0	-	-	ns
LRCK edge -> SCK rise	tLS	0	-	-	ns

- Reset pulse width

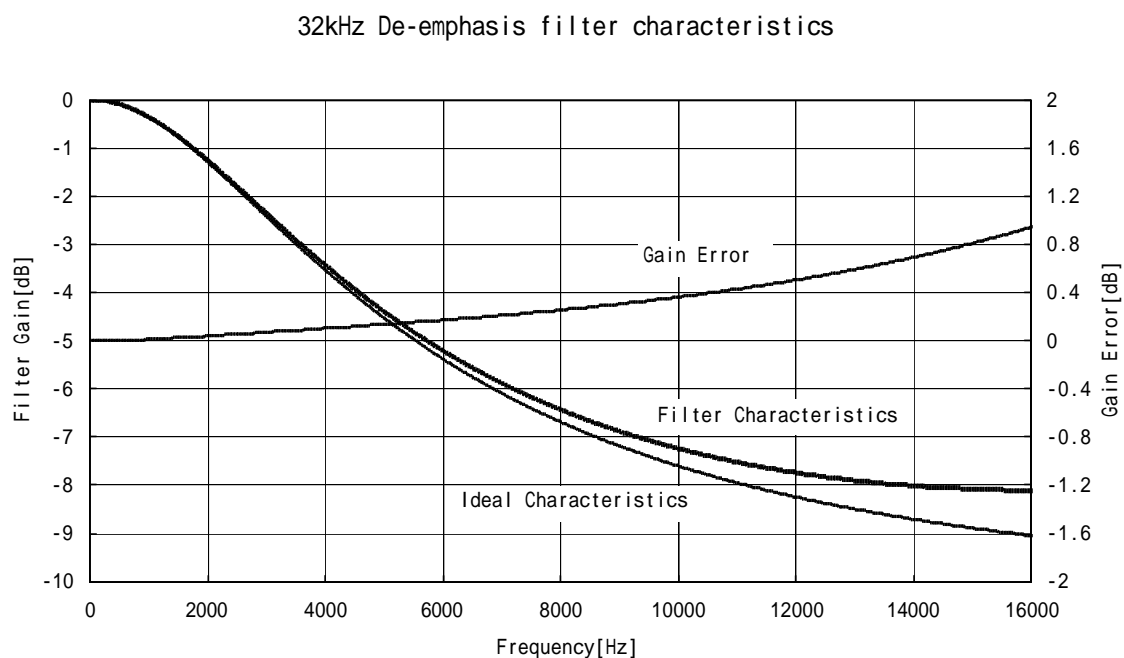


Item	Symbol	MIN	TYP	MAX	UNIT
Reset pulse width	tRSTB	100	-	-	ns

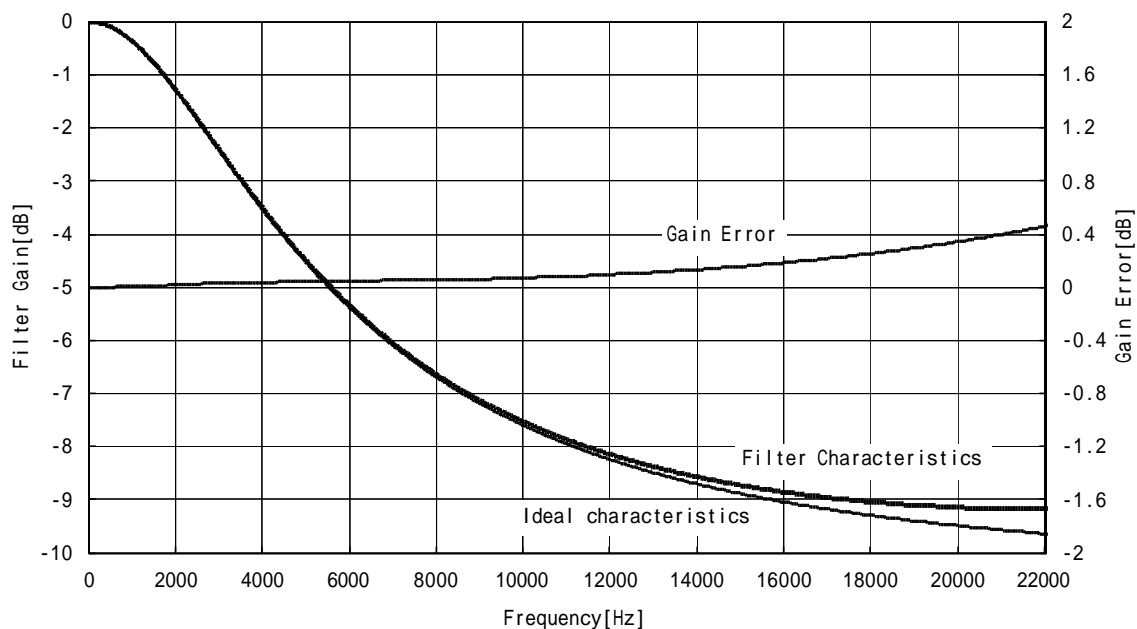
Filter characteristics



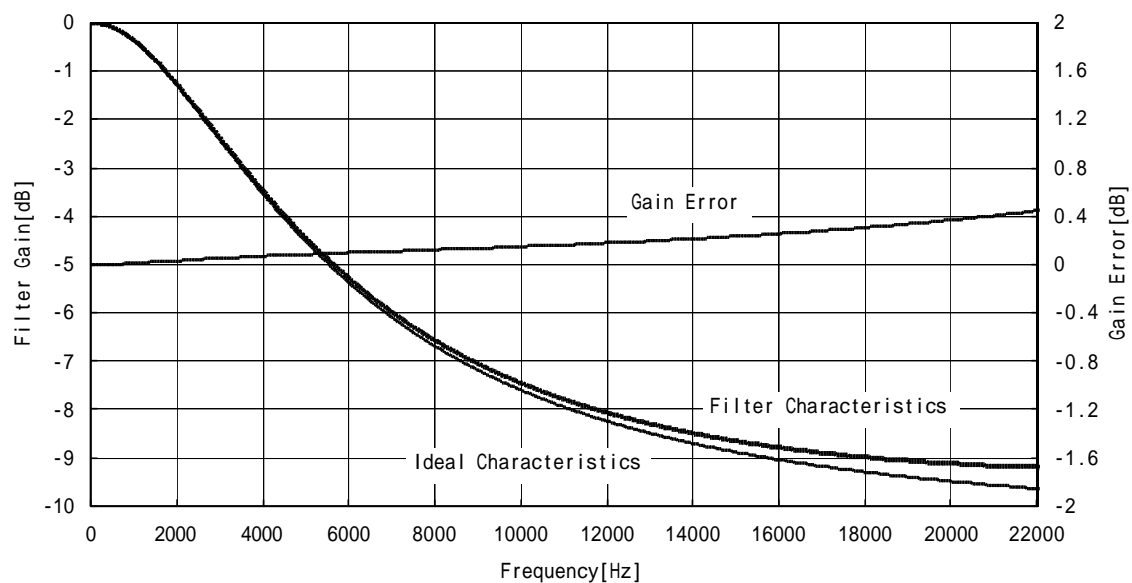
De-emphasis filter characteristics



44.1KHz De-emphasis filter characteristics



48kHz De-emphasis filter characteristics



Terminals

- System clock

FN1242 supports the master clock frequencies of 128fs, 192fs, 256fs, 384fs, 512fs, and 768fs. However, certain combinations of master clock frequency and sampling frequency are not available.

Sampling frequency	128fs	192fs	256fs	384fs	512fs	768fs
32kHz, 44.1kHz, 48kHz						
88.2kHz, 96kHz					×	×
176.4kHz ,192kHz			×	×	×	×

The master clock frequencies are automatically selected internally, however, performance is not guaranteed when the combination of sampling frequency and master clock frequency is “X” as shown in the above table.

- RSTB

Reset the internal circuit by setting this terminal to LOW level. Function setting register is reset. OUTLM, OUTLP, OUTRM, and OUTRP terminals become BPZ while this terminal is set to LOW level.

- ZEROL ,ZEROR

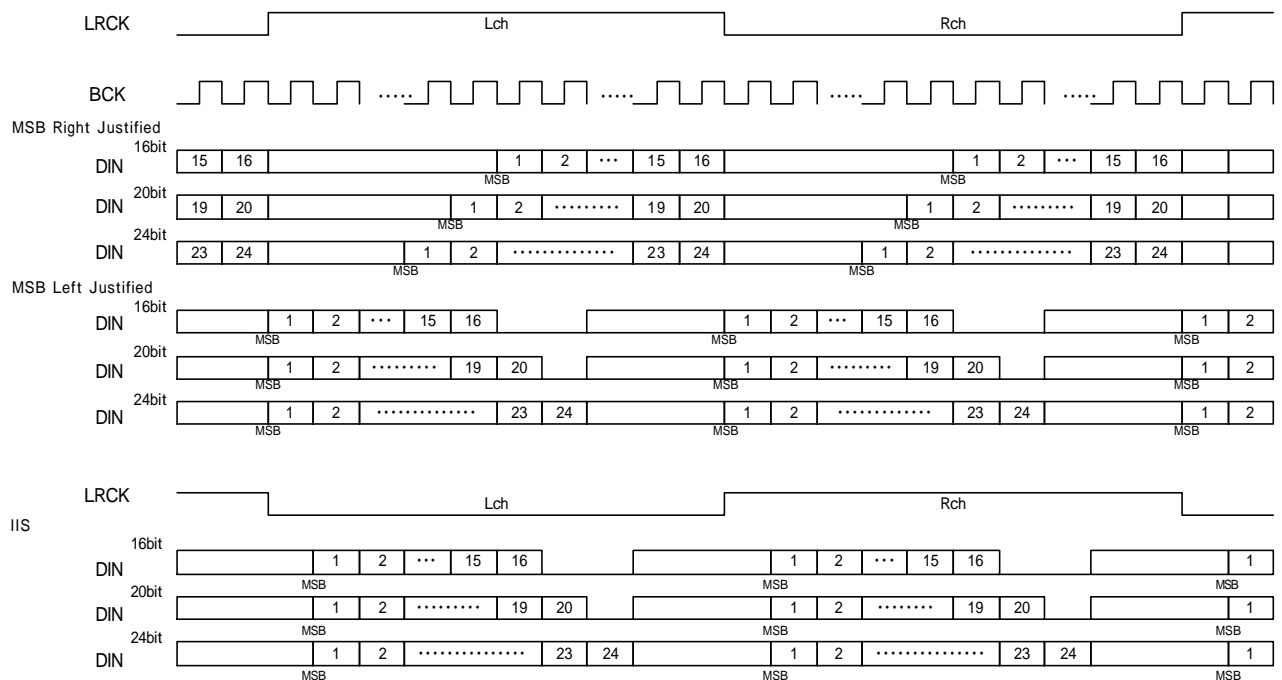
When DIN input data remains binary zero during the 4095/BCK period, ZEROL and ZEROR terminals are set to LOW. ZEROL and ZEROR correspond to Lch and Rch respectively. When the input data is not binary zero, ZEROL and ZEROR terminals are immediately set to HIGH.

- Audio format (FMT2, FMT1, FMT0)

Audio data input formats are shown below. MSB left justified, MSB right justified, and IIS formats with the selected bit length are available by setting with the format setting terminals, FMT2, 1, and 0 as shown in the following table.

FMT2	FMT1	FMT0	Audio format
0	0	0	16 bit right justified
0	0	1	Reserve (unused)
0	1	0	MSB right justified 20 bit
0	1	1	MSB right justified 24 bit
1	0	0	DSD format
1	0	1	MSB left justified 16, 20, 24bit
1	1	0	IIS 16, 20, 24bit
1	1	1	Reserve (unused)

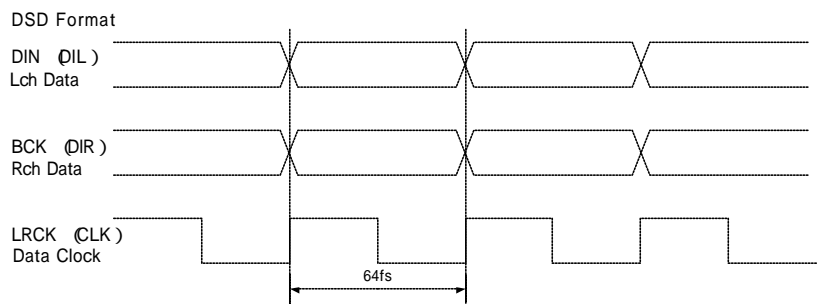
- LRCK, BCK, DIN



For MSB left justified format and IIS format, fix the 8 bit serial data beyond LSB to zero when input 16 bit, and fix the 4 bit serial data beyond LSB to zero when input 20 bit.

- DIL, DIR, CLK (DSD Audio input)

DSD format is shown below.
Input Lch data (DIL) to DIN terminal and Rch data (DIR) to BCK terminal. Input CLK (data clock) to LRCK terminal. The data is valid on the falling edge of CLK. There is no restriction on the phase relationship between CLK and SCK.



Function setting

Functions can be controlled 1) directly from the input terminals or 2) using the serial terminals (ML, MD, MC).

1) Setup directly from the input terminals

The following functions can be set directly from the input terminals.

• De-emphasis (EMPH1, EMPH0)

EMPH1	EMPH0	De-emphasis	シリアル設定時
0	0	32kHz	
0	1	44.1kHz	
1	0	48kHz	
1	1	OFF	

De-emphasis filter ON/OFF and the coefficient corresponding to the sampling frequency are selectable with EMPH1 and EMPH0.

• Soft mute

MUTE	Soft mute	シリアル設定時
0	OFF	
1	ON	

Soft mute is enabled when set at 1.

When you setup the functions using the serial terminals instead of input terminals, set EMPH1, EMPH0 at 1 and MUTE at 0.

2) Setup using serial terminals (ML, MC, and MD)

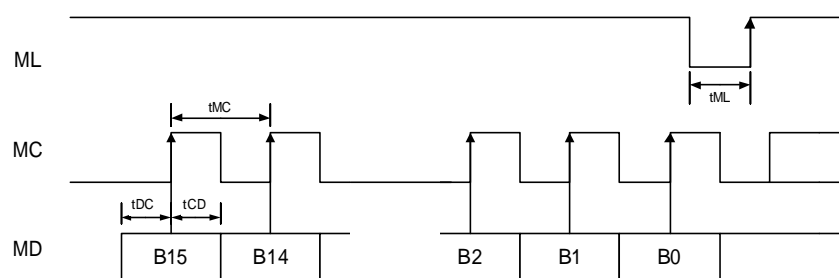
Send the serial control signal to each of the ML, MC, and MD terminals.

The serial control data is set by 16 bit MD data.

The register map is shown below.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
MODE0	res	res	res	A1	A0	LDL	AL9	AL8	AL7	AL6	AL5	AL4	AL3	AL2	AL1	AL0
MODE1	res	res	res	A1	A0	LDR	AR9	AR8	AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0
MODE2	res	res	res	A1	A0	res	res	RST	BIT1	BIT0	ZM1	ZM0	ATC	MUTE	EMPH1	EMPH0

MD, MC, ML signals input timing is as below.



$$t_{MC}(\min) = 200\text{ns}, \quad t_{DC}(\min) = t_{CD}(\min) = t_{ML}(\min) = 100\text{ns}$$

The mode control register basically has three mode registers (MODE0 ~ MODE2), and the registers are selected and set with the 16 bit serial data. First, select the register with A1 and A0 bits, and then control each function with the other bits.

• Control Register Mode (A1, A0)

Register	A1	A0
MODE0	0	0
MODE1	0	1
MODE2	1	0

• Attenuator (LDL, AL9-AL0, LDR, AR9-AR0)

MODE0 and MODE1 are digital control registers. By using each bit of AL9 – AL0 (Lch) and AR9 – AR0 (Rch) (AL7 and AR7 are for MSB, AL0 and AR0 are for LSB), 1024-step attenuator can be controlled independently of Lch/Rch. LDL and LDR are used to set attenuator value. When either LDL or LDR is set at “1”, the attenuator setup value becomes valid. When both LDL and LDR are set at “0”, attenuator setup value is valid, but the actual attenuator value remains at the previous level, and is not updated until LDL or LDR is set at “1”. The minimum time required for attenuator value to shift from 0 dB to - is 1024/fs.

Attenuation, ATT, is given in the following formula.

$$ATT = 20 \times \log(DATA/1023) [dB]$$

DATA :Attenuator setup value

3FFh = 0dB (Default)

3FEh = -0.00849dB

•

•

•

001h = -60.1975dB

000h = - (MUTE)

• Reset (RST)

RST	Reset	Default
0	OFF	
1	ON	

Reset the internal register. Functions are reset to the default. RST register is also reset.

• Bit Length (BIT1, BIT0)

BIT1	BIT0	Bit Length	Default
0	0	16bit	
0	1	20bit	
1	0	24bit	

Select the bit length for MSB left justified format and IIS format. For MSB right justified format, set the bit length to the default.

• Zero Detection Output Mode (ZM1, ZM0)

ZM1	ZM0	Output Mode	Default
0	0	Open Drain + Pull-up	
0	1	Open Drain	
1	0	Push Pull	

Switch the output mode of the zero detection output terminals, ZEROL and ZEROR.

• Attenuator control (ATC)

ATC	Attenuator control	Default
0	Lch/Rch Independent	
1	Lch/Rch Common	

When ATC = 0, AL9 – AL0 are used as the attenuation level for Lch, and AR9 – AR0 are used as the attenuation level for Rch.

When ATC = 1, AL9 – AL0 are used as the attenuation level for Lch/Rch.

• Soft mute (MUTE)

MUTE	Soft mute	Default
0	OFF	
1	ON	

"1" Enables soft mute.

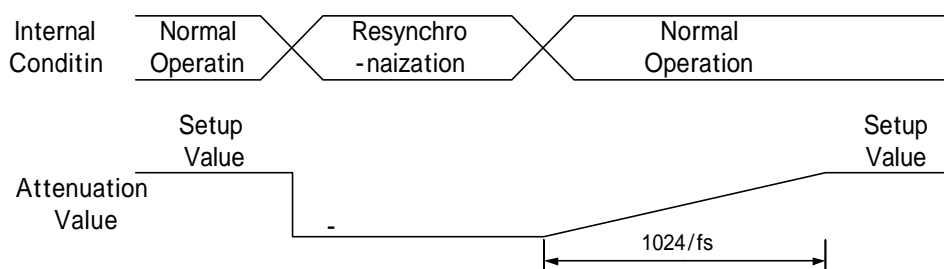
• De-emphasis control (EMPH1, EMPH0)

EMPH1	EMPH0	De-emphasis	Sampling frequency	Default
0	0	OFF	-	
0	1	ON	44.1kHz	
1	0	ON	48kHz	
1	1	ON	32kHz	

Select coefficient according to de-emphasis filter On/Off and sampling frequencies.

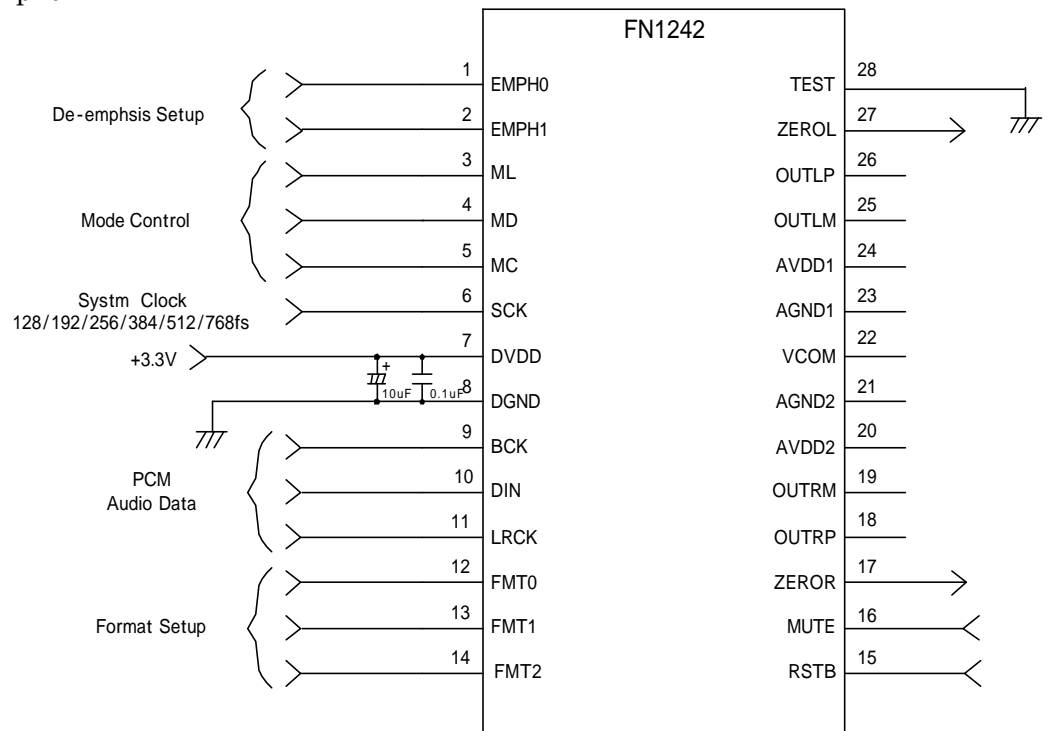
Jitter Free Function

When the difference between SCK and LRCK does not exceed $\pm 10 \times$ (SCK clock period), all the functions continue to operate normally. When the timing error exceeds this value, SCK is automatically resynchronized, and this will cause discontinuous operation. In order to minimize the effect of discontinuous operation on the analog signal, the output data of the digital filter is forced fixed to BZP. When synchronization is established, attenuation value returns to the setup value using the digital attenuator.

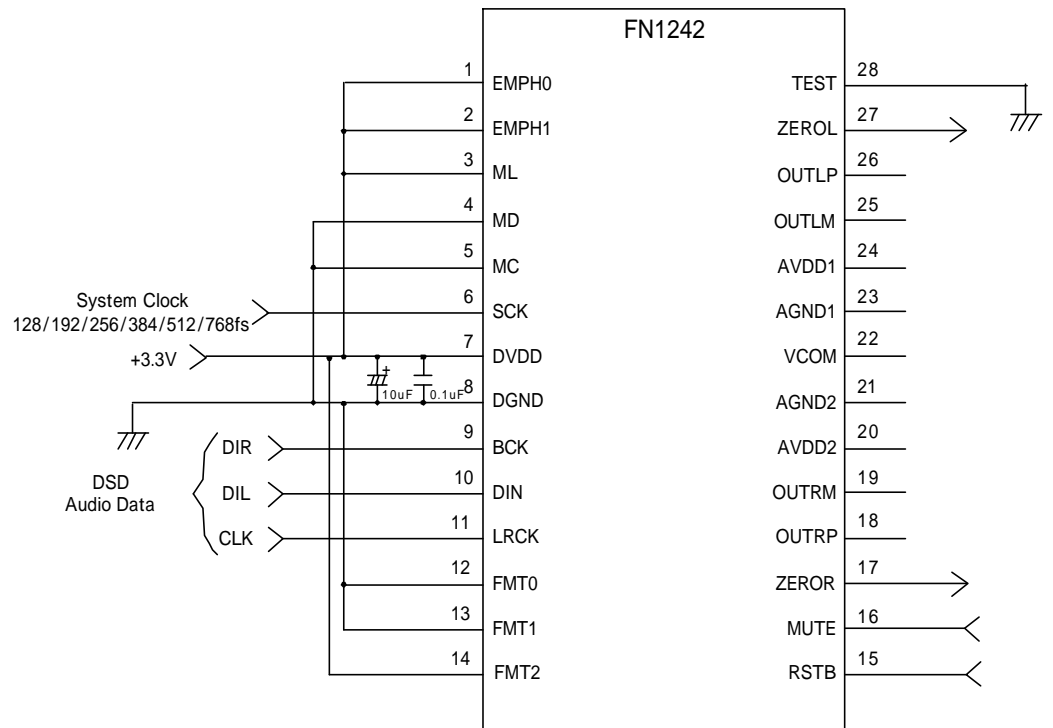


Application example

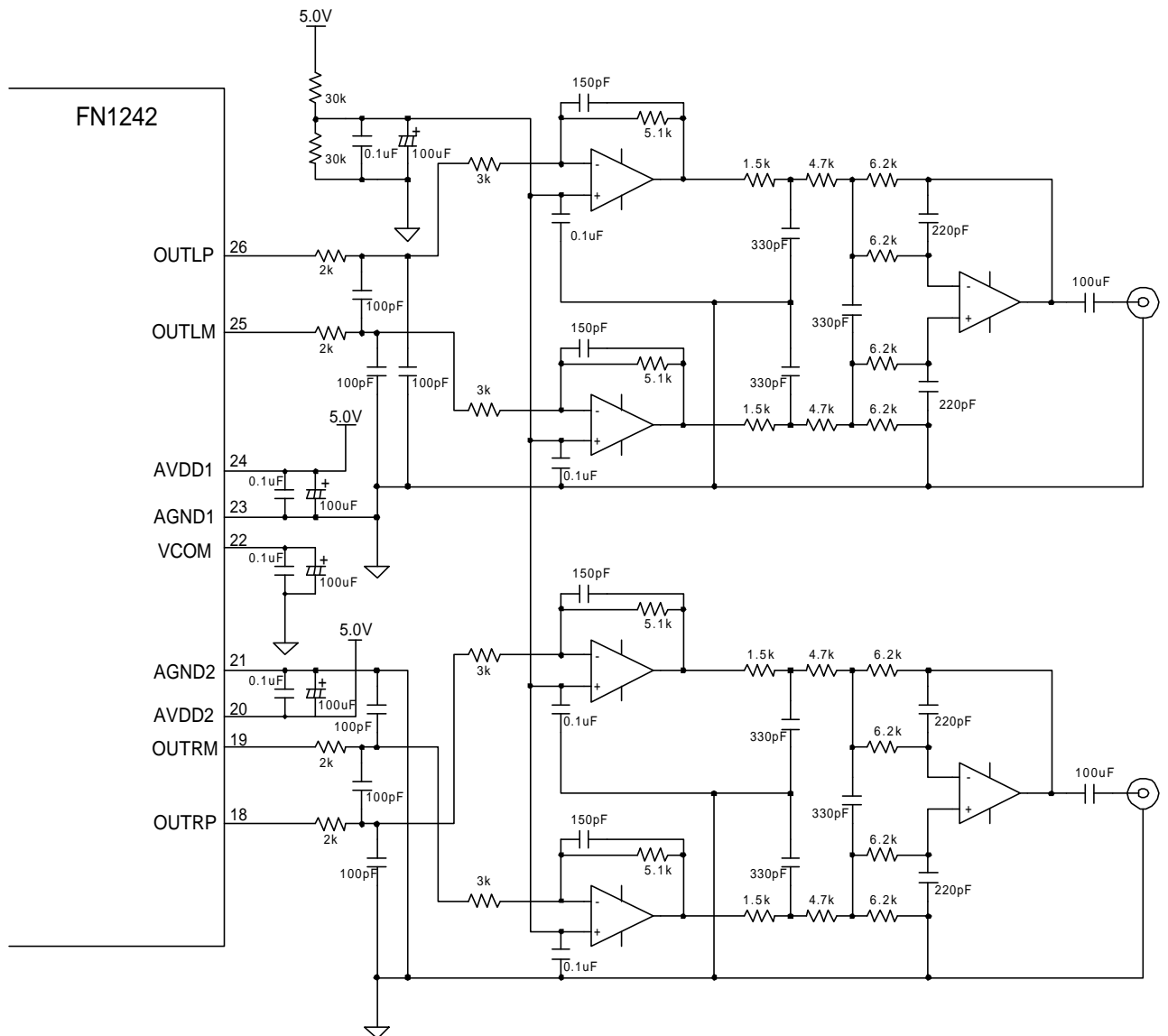
(1) PCM Audio Input



(2) DSD Input



(3) Analog Output

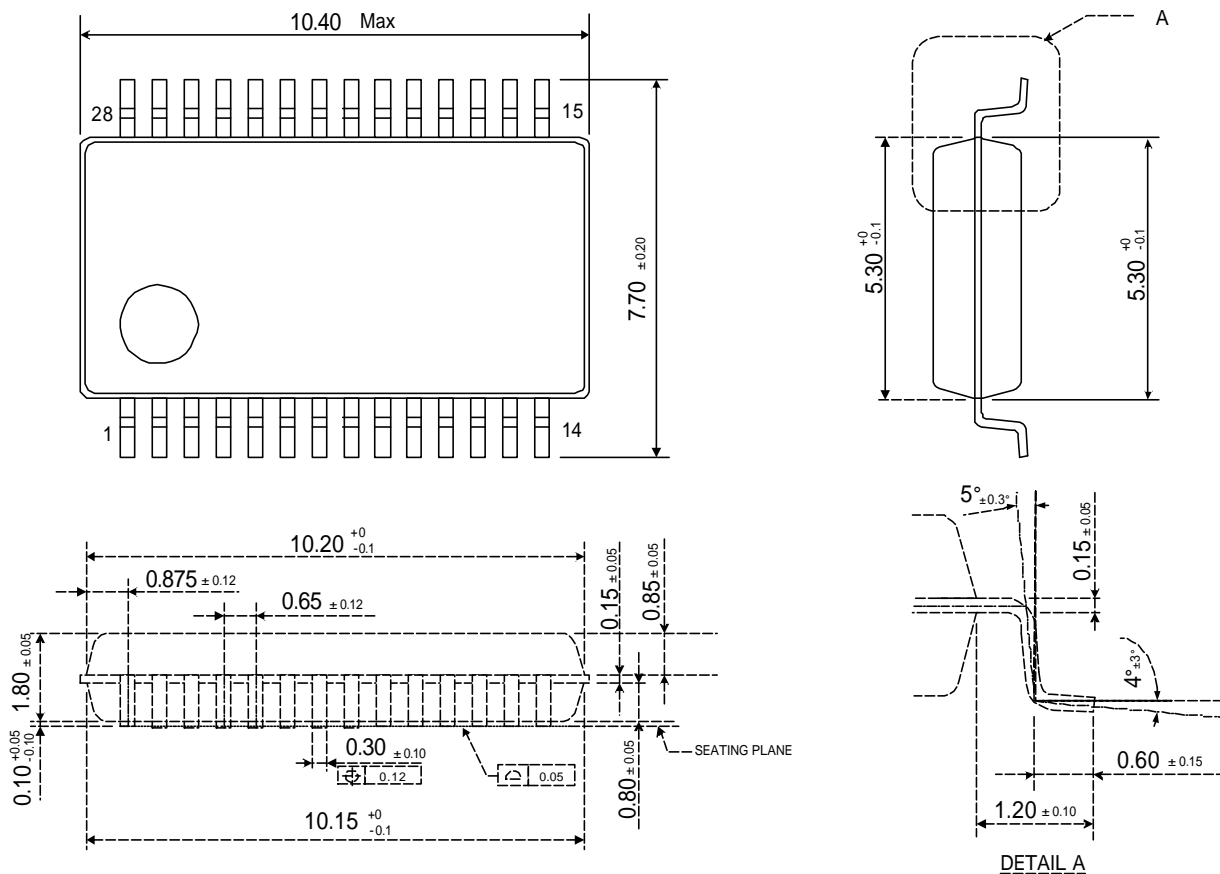


Package Marking

Package

SSOP - 28 (Unit : mm)

ALL DIMENSIONS ARE MILLIMETER



Marking

