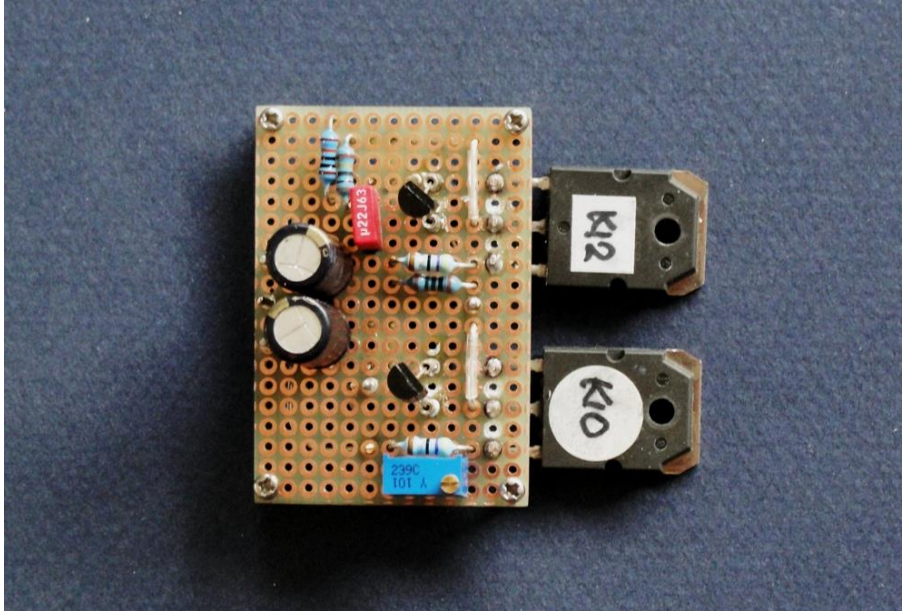


## A Casual Fling with Fetlingtons

(The Fling Headphone Buffer with Trimmable H2)

XEN Audio

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### Background

Recently TI announced a low-noise JFET called JFE150. It is quite low noise, probably a touch better than 2SK170, but it is SMD (not much dissipation), very high  $I_{dss}$ , not graded, and expensive.

I was thinking what to do with it if I had some. They have to operate far away from  $I_{dss}$ , not much more than a few mA because of dissipation limits. That means a negative gate bias voltage, or a large source resistor. So other than a LTP or an expensive CCS, really not much you can do with it.

After some mental jogging, I posted a circuit at DIYA, using this to bias an Exicon MOSFET<sup>[1]</sup>. The purpose is to create a positive bias voltage at the gate of the Exicon while the input signal is at 0V. Essentially, the JFET is acting as a source follower + level shifter. Since the JFET now is only driving the gate of the MOSFET, it can have low bias current, and a large source resistor would not matter.

### Different Variants

The JFE150 is just too expensive to buy 100x to match for  $I_{dss}$  and pick a few.

What is really needed is a JFET that has a large negative  $V_{gs}$  at 1~1.5mA. This has to be bigger in magnitude than the  $V_{gs}$  of the MOSFET at bias. That is also the reason to choose Exicon, as it has low  $V_{gs}$  at 150mA, as well as a negative tempco. And of course, its low capacitances are an added bonus.

The J113 comes to mind. It is quite low noise, has a large enough  $V_{gs}$  at 1mA ( normally < -1V ), and is widely available. If one wants to use other MOSFETs such as IRF610 or FQP3N30, then one has to go to something like the J111 to get >4V at the gate, and raise rail voltage at the same time. Not the preferred solution.

One can now consider the J113-Exicon combo as a compound FET transistor, also known as Fetlington. Two of these with matched effective "Idss" will make a Borbely Source Follower<sup>[2]</sup>, more than sufficient to drive low-impedance headphones.

But unlike the DAO Power JFET buffer, the Fetlington Follower has rather high 2<sup>nd</sup> harmonics. The White Follower (also mentioned by Borbely above) comes to the rescue. This has a modulated CS to act as quasi-push-pull with two N-FETs. By playing with the modulation level, one can adjust the level of even harmonics, theoretically down to zero and then further to reversed phase. This adjustment though is load impedance dependent. You would thus want a somewhat constant load and you need to trim to that load for optimal performance. Alternatively, you can set it to 30R and then use a rotary switch to add a parallel resistor to compensate for other (higher) load impedances.

How about 2SK1058 ? In the examples that we have measured, the Renesas laterals have a somewhat higher Vgs than the Exicon's. So it all depends on your J113's. 2Sk1058's are in general easier to get than the Exicon's from reliable suppliers.

All fine, but laterals are also not cheap. What else can we use for the output devices ? With bias voltage less than 1V, only other choice is an NPN BJT with hfe > 120, such as 2SC4883 or D44H11. One will need some emitter degeneration (say 2.2R) to prevent thermal run-away.

The load seen by the JFET is a bit different from the MOSFET case. In the latter, the JFET is only loaded by the source resistor, and the (low) capacitances of the laterals. And the gate stopper (required for stability) does not really conduct any current and hence drop additional voltage. This is not the case with an NPN.

With an NPN of say hfe 120 and biased at 150mA, the base current alone is 1.25mA. So there is much less current left for the source resistor, and it should be correspondingly higher in value. Furthermore, any base resistor will drop even more voltage under the JFET source. Voltage that is already in limited supply. One can therefore consider leaving out the base resistor altogether. The load seen at the source of the JFET is now the source resistor in parallel with (hfe x emitter resistor of the NPN). The latter will dominate. With hfe of 120 and Re of 2.2R, this comes to 264R, quite a heavy load for the J113. As with the Exicon's, one can just rely on the White Follower to cancel the even harmonics. And the 3<sup>rd</sup> harmonics is not higher than with the laterals, according to Spice. One can also put 2x matched J113's in parallel to share the load. This will certainly improve performance, even before harmonic cancellation.

## Practical Building

As always, when using FETs, you should match devices tightly if you want the best performance and identical channels. There are people who advocate no matching, and use NFB to mask the resulting higher distortions. Fine, if that is what you want to do. You cannot do this in a buffer with no NFB.

So how to determine some nominal values before soldering ?

In the case of the laterals, the MOSFET Vgs at bias (150mA) has to be first measured. The negative Vgs of the JFET at 1.5mA then follows. Select only those JFETs which has a larger Vgs in magnitude than that of the MOSFETs. The biasing resistors (R1,2) are then given by Vgs\_NMOS / 1.5mA. And R3,4 are given by ( | Vgs JFET | - Vgs\_NMOS ) / 1.5mA. You will need to fine trim R3 or R4 in circuit for DC offset and NMOS bias. The bias current is most easily measured across R5,6.

After setting all DC values as desired, it is time to play with the White Follower by soldering in C1. For that you would of course need to have a means of measuring the output distortion spectrum. And as mentioned before, the output needs to be loaded with the desired load impedance. Starting values of

R5,6 & R6a are 6.8R & 100R respectively. Replace temporary R5a,b with a 100R trimmer. After trimming for the desired level of 2<sup>nd</sup> harmonics, replace them with fixed resistors to give same ratio as trimmer, and  $R5a + R5b = 100R$ . Start the trimmer with the wiper at the topmost position (no push-pull) before trimming.

### Bias setting with No Matching

No matching only means that you do not have matched devices. You still need to make sure the JFET has sufficient  $V_{gs}$  to bias the NMOS. So you still need to do the  $V_{gs}$  measurements.

If J1,2 & M1,2 are not matched, You need to set the top and bottom half individually first. Leave out C1 for the White Follower (I have it on sockets). Replace R1,2 & R3,4 with 2x 1k trimmers, pre-set at midpoint. First, connect output to Gnd, leave input open and +Vs unconnected. Connect lab supply with current limit only to -Vs. Adjust lower trimmer until current consumption = 150mA.

Repeat with top half by connecting input & output to Gnd. Leave -Vs open, and connect lab supply to +Vs. Adjust trimmer until current consumption = 150mA.

Now leave output open, connect input to Gnd. Apply power to both rails. Adjust the bottom trimmer for DC offset. Then insert C1 and adjust 2<sup>nd</sup> harmonics as above. Odd harmonics might differ between channels without channel-to-channel matching.

### Bipolar Version

The calculation for the BJT version is rather different because of the base current. The base current  $I_b$  is given by  $I_b = I_c / h_{fe}$ . It is favourable to use a device with high  $h_{fe}$ . The base voltage  $V_b$  is given by  $(V_{be} + I_c \times R_7)$ . It is assumed that  $R_{g1,2}$  are 0R. One can then calculate the value of R1 & R2.

$$R1 = V_b / (1.5mA - I_b / n)$$

where n = no. of JFETs in parallel

$$R2 = (V_{gs} - V_b) / 1.5mA$$

Starting value of R7 can be 2.2R. DC fine trimming is again via R2,4.

For harmonics trimming, starting values of R5,6 & R6a are 10R & 200R respectively.

### What's the Snag ?

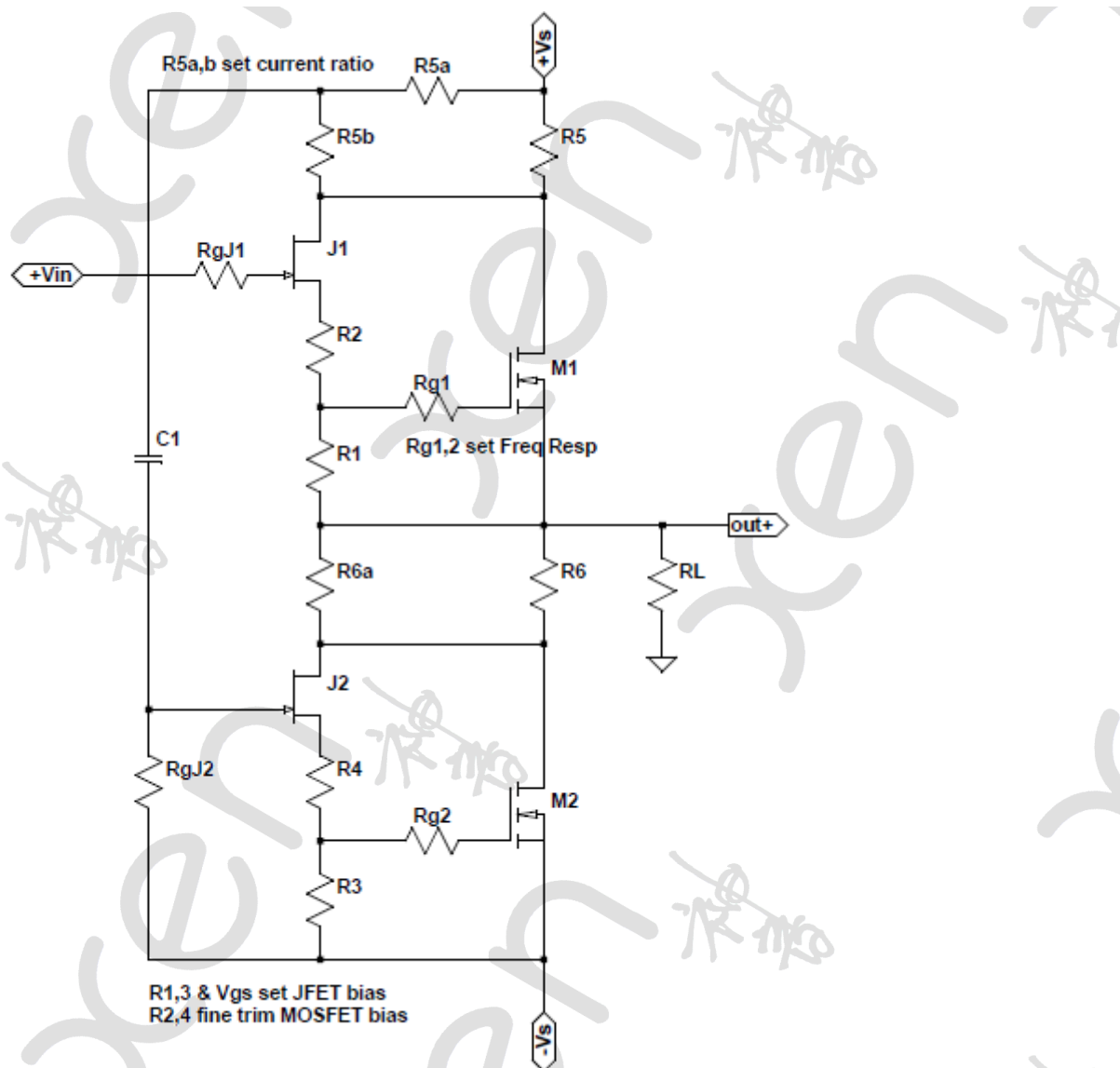
All sound too wonderful ? Correct. What has not been mentioned, but common to all White followers, is that it has no PSRR. So power supply noise will also appear at the output, only slightly attenuated by about 3dB<sup>[3]</sup>. Yes, you can also use TCS, as in the DAO SE, but that makes things complicated, and loses the attraction of easy harmonic adjustments. Much easier to invest in a low noise power supply. As long as both rails drift symmetrically, only noise matters.

Also, at start up, C1 is not charged up, and J2 will see a large positive voltage. The gate current is limited by R3,4 during that transient. To keep that time short,  $C1 / R_{gJ2}$  should be something like 220n / 100k. And you will need a relay to disconnect your headphones during the first couple of seconds.

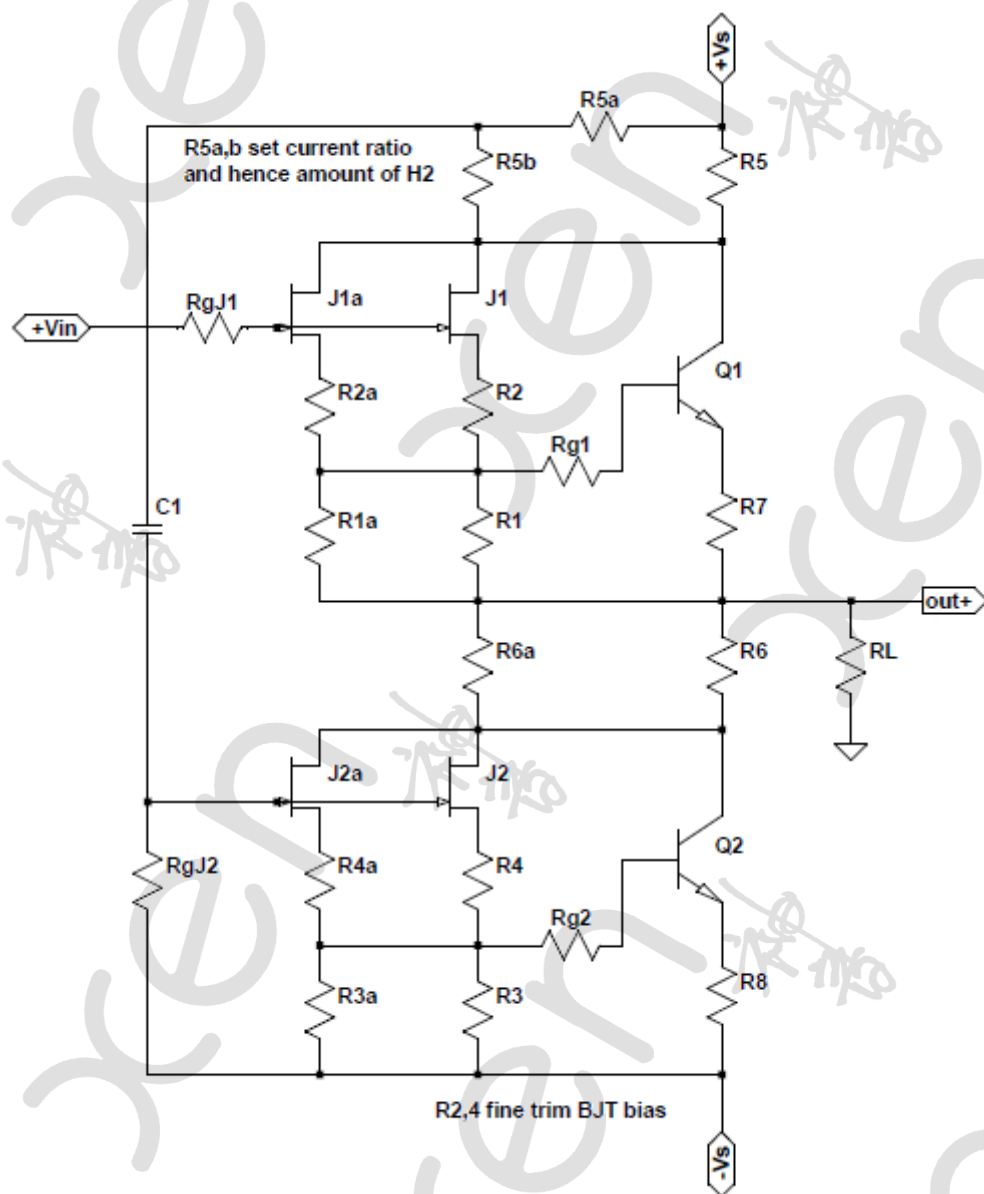
### Applications

Just like the DAO follower, or the XELF, the Fling can be used alone as a power buffer for headphones down to 30R. The JFET input means that it is an easy load for the signal source. If you need gain, you can use an additional gain stage up front, either with an opamp, or something like the XCEN. And in case of opamp, you can still decide whether to wire the buffer inside or outside the feedback loop.

So, time to have fun. 😊



Schematics Fling Headphone Buffer J113 -- Exicon



Schematics Fling Headphone Buffer Dual J113 – BJT

## Reference

1. <https://www.diyaudio.com/forums/vendor-s-bazaar/375079-ultra-low-noise-jfets-texas-instruments-post6755877.html>
2. <https://audioxpress.com/article/JFETs-The-New-Frontier-Part-2>
3. <https://www.tubecad.com/2004/blog0023.htm>



## Appendix 1 Bill of Materials

### For one Buffer Channel with Exicon Laterals

Qty.	Designation	Description	Remark
2	J1,2	J113	matched Vgs at 1mA
2	M1,2	ECX10N20	Vgs larger than Vgs of M1, M2. matched Vgs at 150mA
2	R1,3	RN55 820R 1%	adjust MOSFET bias & DC offset
2	R2,4	RN55 1%	
6	R5,6	RN55, 10R 1%, 3x //	
--	R5a,5b	Sum = 33R	
1	R6a	RN55 33R 1%	
2	Rg1,2	RN55 2k 1%	trim 2 <sup>nd</sup> harmonics
1	Rjg1	220R 1%	
1	Rjg2	1M 1%	
1	C1	WIMA MKP2 1μ	