FET Curve Tracer

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Junction field-effect transistors (JFETs), unlike bipolar transistors, do not easily lend themselves to analytic solutions of bias networks. By their very nature, JFETs are voltage controlled devices. Gate to source voltage (control voltage V_{GS}) variations of several volts can exist within a given part type at the same operating conditions, causing the problem. Multiple suppliers and inadequate or non-existent data sheet curves compound the problem further, requiring data from the suppliers or the use of a curve tracer.

A simple curve tracer, used with any oscilloscope, can be built using a quad op amp and a handful of parts. The circuit displays drain current versus gate voltage for both P and N-channel JFETs at a constant drain voltage.

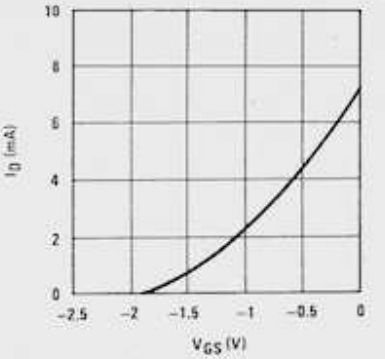
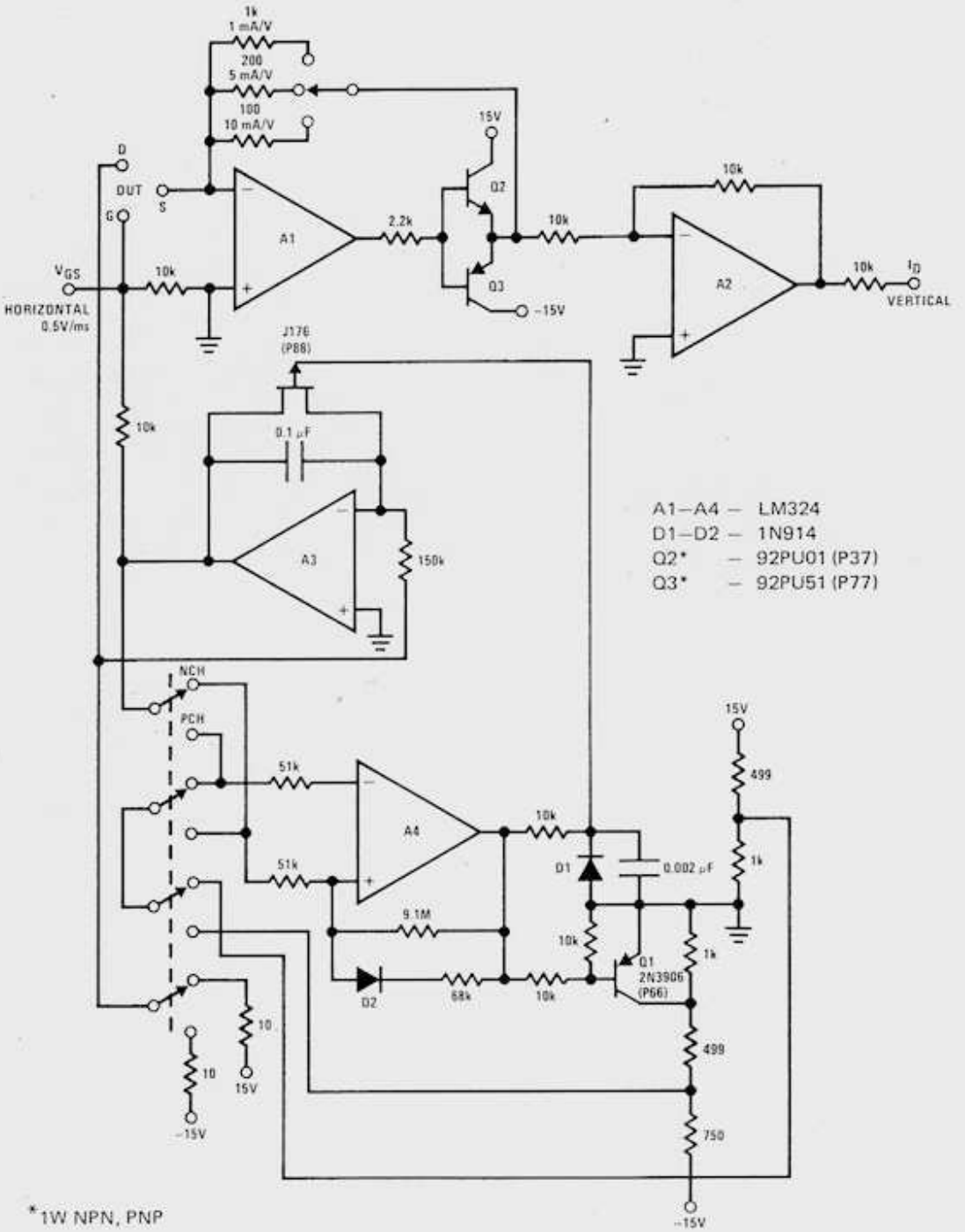


FIGURE 1. Typical N-Channel FET Transfer Curve

The circuit consists of an op amp current to voltage (I/V) amplifier with a positive or negative gate sweep



*1W NPN, PNP

FIGURE 2. FET Curve Tracer

voltage. The I/V amplifier uses 1/4 of the quad op amp and 3 switchable feedback resistors for drain current scaling: 1k for 1 mA/V, 200Ω for 5 mA/V and 100Ω for 10 mA/V. An NPN-PNP emitter-follower buffer is used with the I/V amplifier to handle high FET currents (to 100 mA). A unity gain inverting amplifier is used for proper drain current polarity.

The gate sweep generator consists of 2 parts, a linear ramp generator with a reset and a window comparator. The ramp generator is an op amp with a capacitor in its feedback loop. The sweep rate is set by a constant current supplied to the capacitor through a resistor tied to either the plus or minus voltage supply.

The positive (P-channel) ramp mode uses the positive reference on the plus input of the comparator with the ramp connected to the minus input. The comparator output stays high (15V) pinching the FET OFF until the input exceeds the reference (10V). At that point, the output snaps to the negative supply, turning the FET switch ON, discharging the capacitor. The reference voltage at the plus input is set near ground using the 51k input resistor, D2 and 68k feedback resistor when the comparator output is in the low state. When the capacitor is discharged, the comparator resets, restarting the ramp.

A negative sweep is more difficult to generate using the same comparator. The reference (−10V) is on the minus input with the ramp connected to the plus input. As with the positive sweep, the comparator output is high until the negative sweep exceeds the reference. The difference is that the reference cannot be set to ground for the reset sweep but to a negative voltage such that when the ramp is at 0V the comparator resets. The function of Q2 is to short R1, changing the reference voltage from −10V to −6V.

In both cases, the sweep time is 10 ms. The resistor attenuator on the FET gate terminal divides the voltage in half, yielding a sweep rate of 0.5V/ms with a maximum gate voltage of ±5V. This should be adequate for most FETs used as amplifiers but if additional gate voltage is required, the attenuator can be switched out.

The circuit is limited to displaying only the FET transfer characteristic I_D vs V_{GS}, but this is the curve most needed by designers. It gives insight into parameter variations of bias circuits and it can be used to observe temperature effects on the FET. The oscilloscope vertical input is used for the drain current and the horizontal input is used for the gate voltage. The horizontal sweep can be used if no horizontal input is available where a sweep rate of 0.5 ms/cm corresponds to 0.5V/ms, allowing the curve tracer to be used with any oscilloscope.

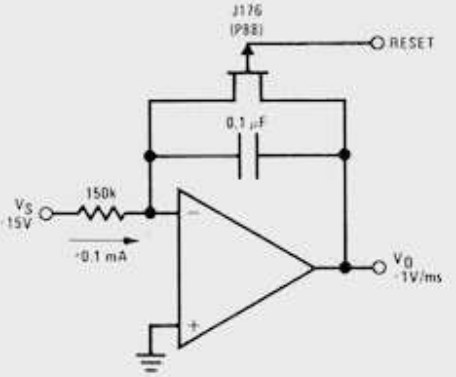


FIGURE 3. Linear Ramp Generator

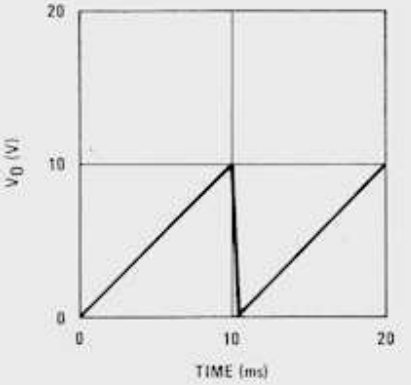


FIGURE 4. Positive Sweep

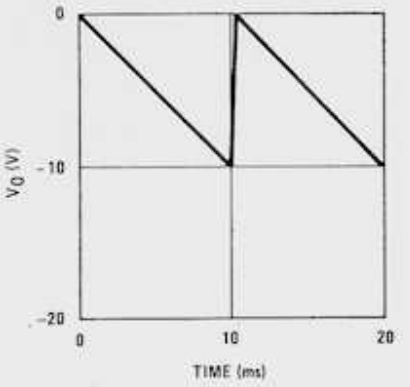


FIGURE 5. Negative Sweep