AKD5394A
Evaluation board Rev.B for AK5394A

GENERAL DESCRIPTION

The AKD5394A is an evaluation board for AK5394A, the 24bit stereo A/D converter for DVD-audio. The AKD5394A has the interface with AKM's D/A converter evaluation boards. Therefore, it is easy to evaluate the AK5394A. The AKD5394A also has the digital audio interface and can achieve the interface with digital audio systems via opt-connector or RCA connector.

■ Ordering guide

AKD5394A --- Evaluation board for AK5394A

FUNCTION

- **On-board 2nd order LPF**
- **On-board clock generator**
- **Compatible with 2 types of interface**
  - **Direct interface with AKM's D/A converter evaluation boards**
  - **On-board DIR(AK4103) which accepts optical output**
- **BNC connector for an external clock input**

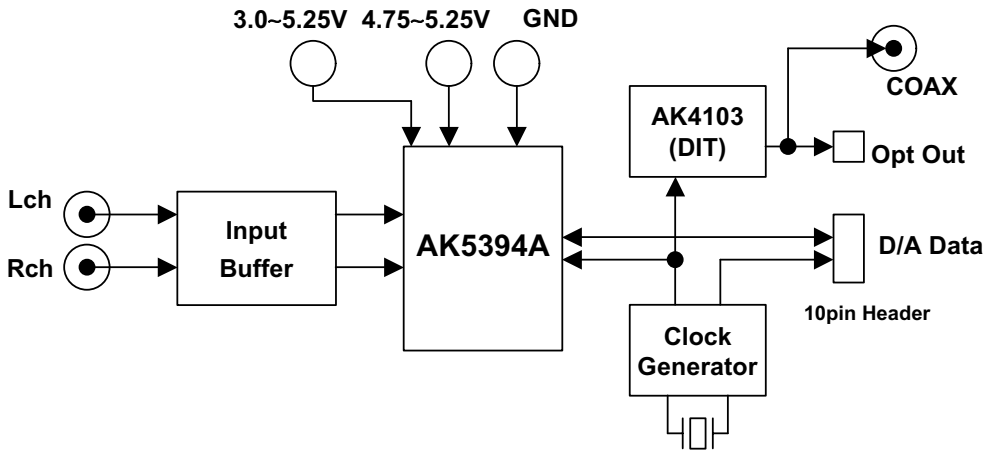


Figure 1. AKD5394A Block Diagram

* Circuit diagram and PCB layout are attached at the end of this manual.

■ Operation sequence

1) Set up the power supply lines.

[-15V] (Blue)	= -15V
[+15V] (Green)	= +15V
[AGND] (Black)	= 0V
[5394_VA] (Red)	= 5V and open JP1 / open and connect JP1
[5394_VD] (Orange)	= 3V~5V
[DGND] (black)	= 0V
[4103] (Red)	= 5V

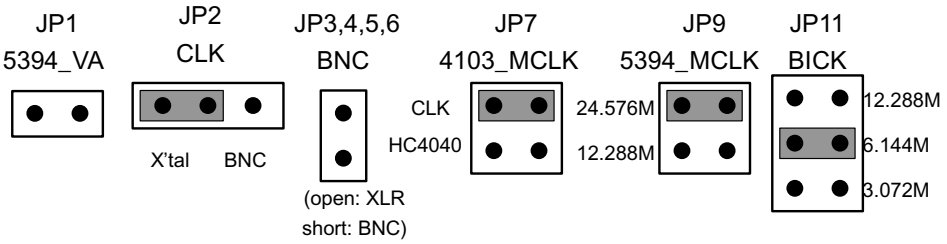
Each supply line should be distributed from the power supply unit.

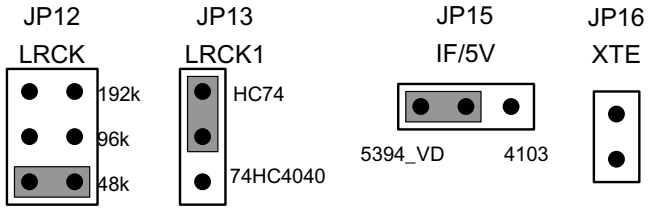
2) Set-up the evaluation modes, jumper pins and DIP switches (See the followings.)

3) Power on.
The AK5394A should be reset once bringing SW1(-PD) "L" upon power-up.

■ Evaluation mode

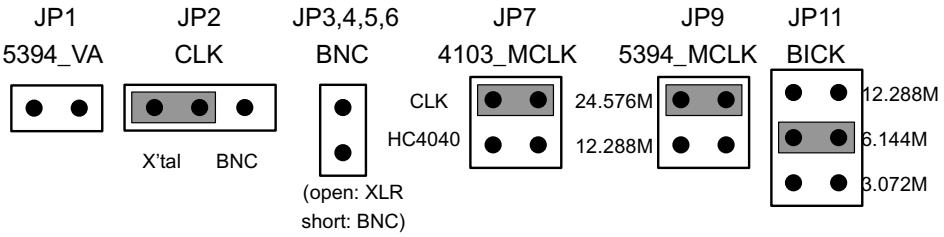
1) DIT (Optical Link and BNC) <default>
PORT2(TOTX176) or J5(BNC) is used. All clocks are supplied to AK4103(DIT). The DIT receives the serial data from AK5394A and output SPDI/F signal through the optical connector (TORX174) or BNC connector. Followings are typical set-up for an evaluation by the optical connection.

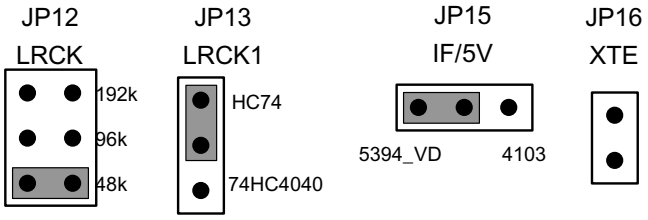




2) Output all serial clocks

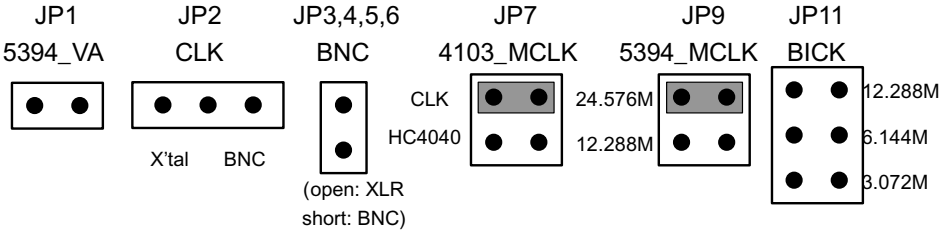
Under the following set-up, all signals can be output through POTR3.
In case of using external master clock through a BNC connector, select “BNC” on JP2(XTI) and short JP16(XTE).
(please refer the schematic diagrams)

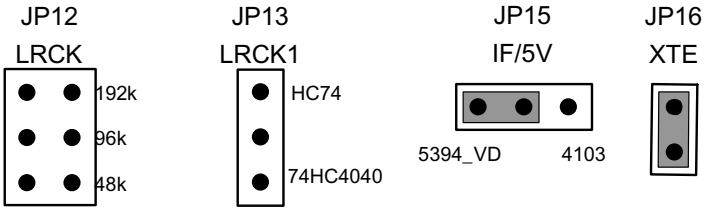




3) Evaluation by analog output (Using AKM’s evaluation board for DAC)

By connecting AKM’s evaluation board for DAC via above two evaluation modes, you can also evaluate AK5394A by analog analyzer. In this mode, please adjust the conditions (clock ratio, data format, etc.) between two boards.





■ DIP switch set up

Normally the upper side is “ON”(“H”), lower side is “OFF”(”L”). Be careful some switches are opposite polarity.

[SW2]:
(please refer AK5394A datasheets)

No.	Pin	OFF	ON
1	DFS1	L (default)	H
2	DFS0	L (default)	H
3	HPFE	L (default)	H
4	SMODE2	L (default)	H
5	SMODE1	L (default)	H
6	ZCAL	L (default)	H

Table 1. SW1 set-up

[SW3]:

No.	Pin	OFF	ON
1	V1	L (default)	H
2	FS0	L (default)	H
3	FS1	L (default)	H
4	FS2	L (default)	H
5	FS3	L (default)	H
6	CKS0	L (default)	H
7	CKS1	L (default)	H
6	DIF0	L (default)	H

Table 2. SW2 set-up

■ System clock example

fs(LRCK)	SCLK	MCLK(AK5394A)	MCLK(AK4103)	DFS1	DFS0	CKS1	CKS0	
48k	6.144MHz	12.288MHz	12.288MHz	L	L	L	L	(default)
96k	6.144MHZ	12.288MHz	24.576MHz	L	H	L	H	
192k	12.288MHz	12.288MHz	24.576MHz	H	L	L	H	

Table 3. clock set-up

■ Serial Data Interface

Format	SMODE2	SMODE1	DIF0	JP11	JP13	
Slave Mode	L	L	L	(Note)	(Note)	
Master Mode	L	H	L	Open	Open	
I^2S Slave Mode	H	L	H	(Note)	(Note)	(default)
I^2S Master Mode	H	H	H	Open	Open	

Table 4. Serial I/F Format set-up
(Note : please refer the jumper list.)

■ Selection of clock

Clock setting of AK5394A and AK4103

LRCK(fs)	MCLK	BICK	JP9	JP11	JP12	JP13	
48kHz	256fs	128fs 64fs	12.288M	6.144M 3.072M	48k	HC74	(default)
96kHz	128fs	64fs	12.288M	6.144M	96k	HC74	
192kHz	64fs	64fs	12.288M	12.288M	192k	HC74	

Table 5. System clock Example

■ Jumper list

[JP1] (AK5394A_VA) : select the power supply source for VA pin of AK5394A.

Open : supply from the jack “5394_VA” (default)
Short : supply from the regulator on board (In case of short, leave the jack “5394_VA” open.)

[JP2] (CLK) : select the master clock frequency for AK5394A and AK4103. (Excepting the case using external BICK and LRCK, BICK and LRCK are generated by the clock from JP2.)

X’tal : supply from on-board crystal oscillator. (default)
BNC : supply from BNC connector(J6)

[JP3,4,5,6] (BNC) : select the connector for analog input.

Short : input through BNC connectors(J2,4)
Open : input through XLR connectors(J1,3) (default)

[JP7] (4103_MCLK) : select the frequency of master clock for AK4103.
(Those values are assumed the X’tal frequency is 24.576MHz)

CLK(24.576M) : feed the frequency selected on JP2 directly to AK4103.
HC4040(12.288M) : feed the half speed of the selected frequency of JP2 to AK4103. (default)

[JP9] (5394_MCLK) : select the frequency of master clock for AK5394A.
(Those values are assumed the JP2 frequency is 24.576MHz)

24.576M : feed the frequency selected by JP2 directly to AK5394A.
12.288M : feed the half speed of the selected frequency of JP2 to AK5394A. (default)

[JP11] (BICK) : select the frequency of serial clock for AK5394A and AK4103.
(Those values are assumed the JP2 frequency is 24.576MHz)

12.288M : feed 12.288MHz SCLK to AK5394A and AK4103.
6.144M : feed 6.144MHz SCLK to AK5394A and AK4103. (default)
3.072M : feed 3.072MHz SCLK to AK5394A and AK4103.

[JP12] (LRCK) : select the frequency of L/R clock for AK5394A and AK4103.
(Those values are assumed the JP2 frequency is 24.576MHz)

192k : feed 192kHz LRCK to AK5394A and AK4103.
96k : feed 96kHz LRCK to AK5394A and AK4103. (default)
48k : feed 48kHz LRCK to AK5394A and AK4103.

[JP13] (LRCK1) : select the source of L/R clock for AK5394A and AK4103.
(Please refer the schematic diagram)

74HC4040 : feed LRCK from 74HC4040 to AK5394A and AK4103.
74HC74 : feed LRCK from 74HC74 to AK5394A and AK4103. (default)

[JP15] (IF/5V) : select the source of the power for digital logic ICs except AK4103.

5394_VD : supply from the jack “5394_VD” (default)
4103_VD : supply from the jack “4103”. Only for the case of “5394_VD”=5V

[JP16] (XTE) : select the on/off of the on-board X’tal oscillator.

Open : use the X’tal oscillator.
Short : not use the X’tal oscillator.

■ The function of the toggle SW

[SW1] : Resets the AK5394A and AK4103. Bring once SW1 from "L" to "H" after power-up, and keep "H" during normal operation.

■ External analog circuit

Figure 2 shows an input buffer circuit example 1. (1st order HPF; fc=0.70Hz, 2nd order LPF; fc=320kHz, gain=-14.5dB). The analog signal is able to input through XLR or BNC connectors. (short JP1 and JP2 for BNC input, open JP1 and JP2 for XLR input). The input level of this circuit is +/-12.7Vpp (AK5394A: +/-2.4Vpp Typ.). When using this circuit, analog characteristics at fs=48kHz is DR=120dB, S/(N+D)=105dB.

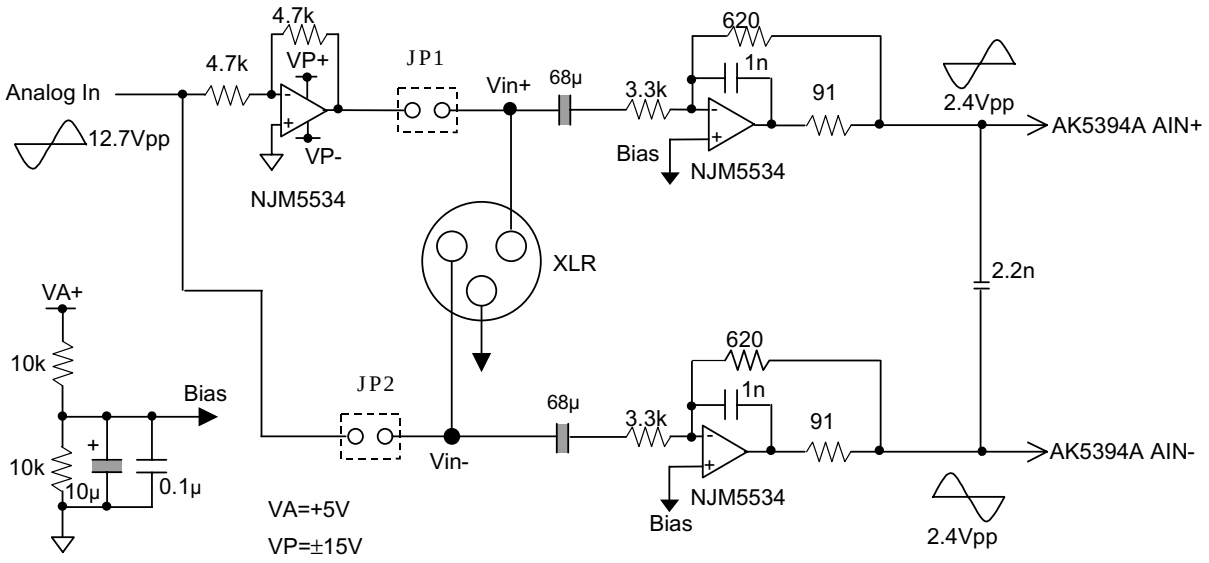


Figure 2. Analog input buffer circuit example 1

Fin	1Hz	10Hz
Frequency Response	-1.77dB	-0.02dB

Table 6. Frequency Response of HPF

Fin	20kHz	40kHz	80kHz	6.144MHz
Frequency Response	0.00dB	0.00dB	0.00dB	-51.36dB

Table 7. Frequency Response of LPF

■ When capacitors more than 10µF are connected between VREF pin and GND

The distortion at low frequency can be improved by connecting large capacitors (C in Figure 3) to VREF pins. (Refer to Figure 4) C = C10, C16, C56, C 58 in Circuit Diagram. However, when the capacitors of VREF pins are larger than 10µF, it is possibility that the offset calibration does not performed correctly if the offset calibration cycle is started right after power-up. Because the internal VREF can not settle to the appropriate voltage when the calibration cycle is completed. In this case, the offset calibration cycle should be started again after the VREF voltage settled. The timing is shown in Figure 5. Table 7 shows the relationship between the capacitance and the VREF settling time.

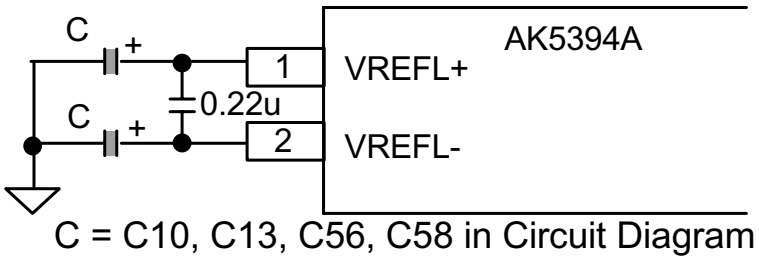


Figure 3. circuit example

Figure 4 shows the relationship between THD+N and Frequency with capacitors on Table 7.
Measurement Example
Ta=25°C; VA=5.0V; VD=3.3V; AGND, BGND, DGND=0V; fs=48kHz; 24 bit Output; BW=10Hz~20kHz; DFS0= "L", DFS1= "L", Measured by Audio Precision System Two.

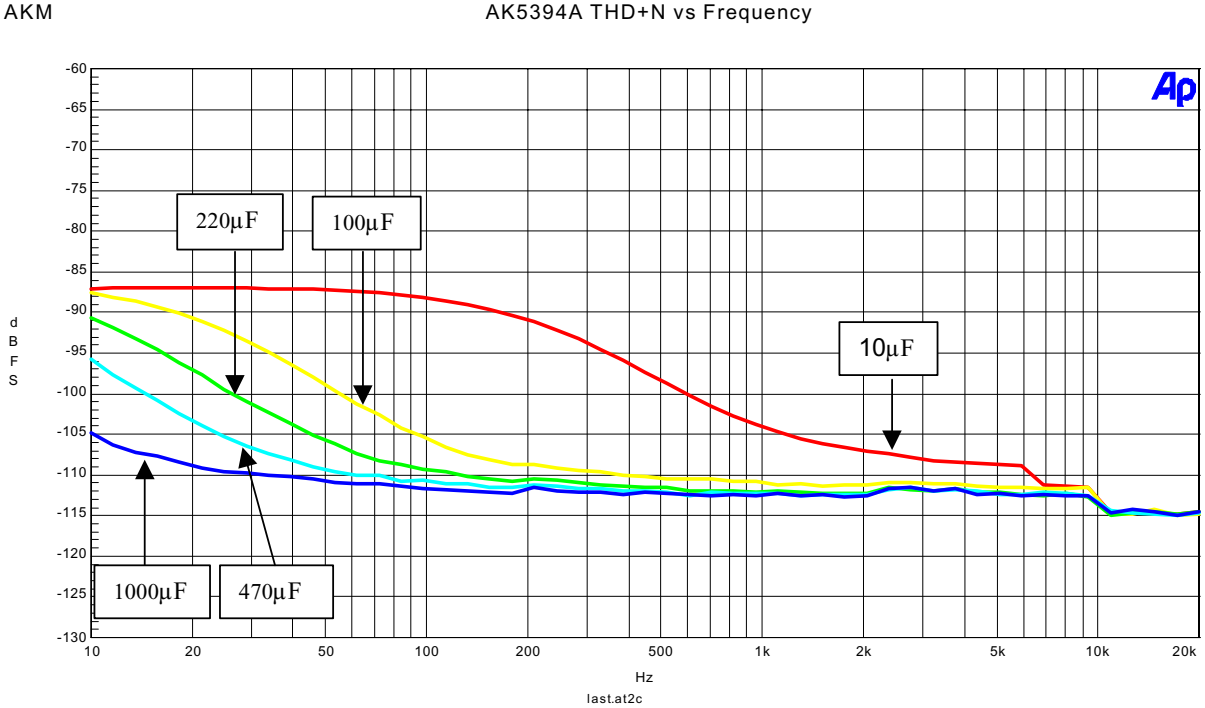


Figure 4. THD+N vs Frequency

Capacitor C [μF]	Settling Time T[s]=0.005 x C
1000	5
470	2.4
220	1.1
100	0.5

Table 7. Settling Time and capacitors connected between VREF and GND

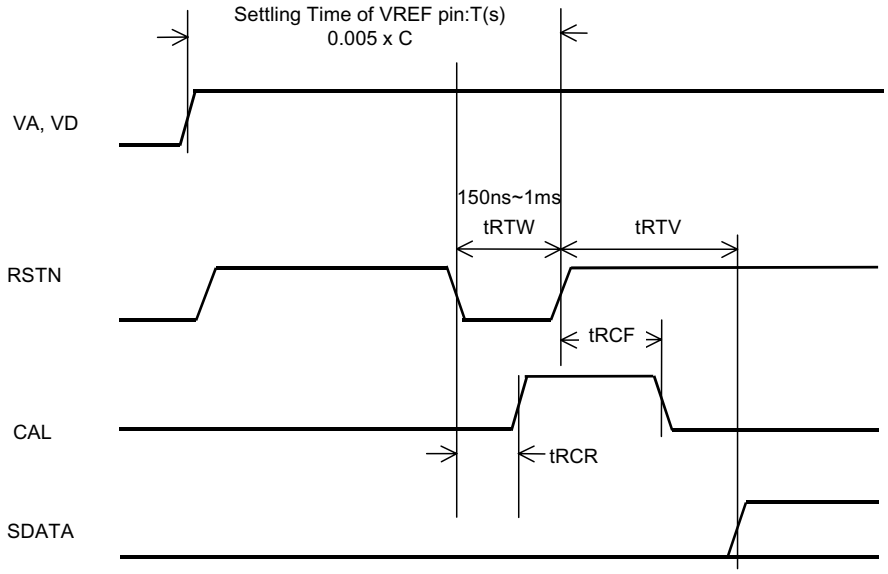


Figure 5. Reset & Calibration Timing

MEASUREMENT RESULTS

[Measurement condition]

- Measurement unit: Audio Precision System Two Cascade(AP2C) / ROHDE & SCHWARZ, UPD04 (R&S)
- MCLK : 12.288MHz
- BICK : 128fs for 48kHz, 64fs for 96kHz and 192kHz
- fs : 48kHz, 96kHz, 192kHz
- BW : 10Hz~20kHz (fs=48kHz)
- Resolution : 24bit
- Power Supply : VA=5V, VD=3.3V
- Interface : DIT / Serial MUX
- Temperature : Room

1. VREF cap = 10µF✍ Measurement Unit = AP2C ; I/F = Optical

Parameter	Input signal	Measurement filter	Results	
fs			48kHz	96kHz
BW			20kHz	Fs/2 (=48kHz)
S/(N+D)	1kHz, -1dB	-	106.0	105.6
	1kHz, -20dB	-	98.1	94.1
	1kHz, -60dB	-	57.3	54.1
DR	1kHz, -60dB	A-weighted	121.0	121.0
S/N	no signal	-	118.7	115.1
		A-weighted	121.1	121.2

[dB]

2. VREF cap = 10µF✍ Meas. Unit = R&S ; I/F = Serial MUX

Parameter	Input signal	Measurement filter	Results
fs			192kHz
BW			80kHz
S/(N+D)	1kHz, -1dB	-	105.1
	1kHz, -20dB	-	91.0
	1kHz, -60dB	-	54.1
DR	1kHz, -60dB	A-weighted	119.0
S/N	no signal	-	111.5
		A-weighted	120.3

[dB]

3. Example measurement, VREF cap=1000µF, Meas. Unit = AP2C; I/F = Optical,

Parameter	Input signal	Measurement filter	Results
fs			48kHz
BW			20kHz
S/(N+D)	1kHz, -1dB	-	111.1
DR	1kHz, -60dB	A-weighted	121.6
S/N	No signal	A-weighted	121.4

[dB]

■ Plots

Measurement unit : Audio Precision, System two, Cascade (fs=48kHz,96kHz),
ROHDE & SCHWARZ, UPD04 (fs=192kHz), VREF cap = 10µF

1. AP2C
(FFT : BW=fs/2, point=16384)
1-1. fs=48kHz
Figure 1-1-1. FFT (1kHz, –1dB input)
Figure 1-1-2. FFT (1kHz, –60dB input)
Figure 1-1-3. FFT (off the input)
Figure 1-1-4. THD+N vs Input Frequency (-1dB input)
Figure 1-1-5. THD+N vs Input Level (1kHz input)
Figure 1-1-6. Linearity (fin=1kHz)
Figure 1-1-7. Frequency Response (-1dB input)
Figure 1-1-8. Cross-talk (-1dB input)
1-2. fs=96kHz
Figure 1-2-1. FFT (1kHz, –1dB input)
Figure 1-2-2. FFT (1kHz, –60dB input)
Figure 1-2-3. FFT (off the input)
Figure 1-2-4. THD+N vs Input Frequency (-1dB input)
Figure 1-2-5. THD+N vs Input Level (1kHz input)
Figure 1-2-6. Linearity (fin=1kHz)
Figure 1-2-7. Frequency Response (-1dB input)
Figure 1-2-8. Cross-talk (-1dB input)

2. R&S
(FFT : BW=fs/2, point=8192)
2-1. fs=192kHz
Figure 2-1-1. FFT (1kHz, –1dB input)
Figure 2-1-2. FFT (1kHz, –60dB input)
Figure 2-1-3. FFT (off the input)
Figure 2-1-4. THD+N vs Input Frequency (-1dB input)
Figure 2-1-5. THD+N vs Input Level (1kHz input)
Figure 2-1-6. Linearity (fin=1kHz)
Figure 2-1-7. Frequency Response (-1dB input)

1. AP2C

1-1. fs=48kHz

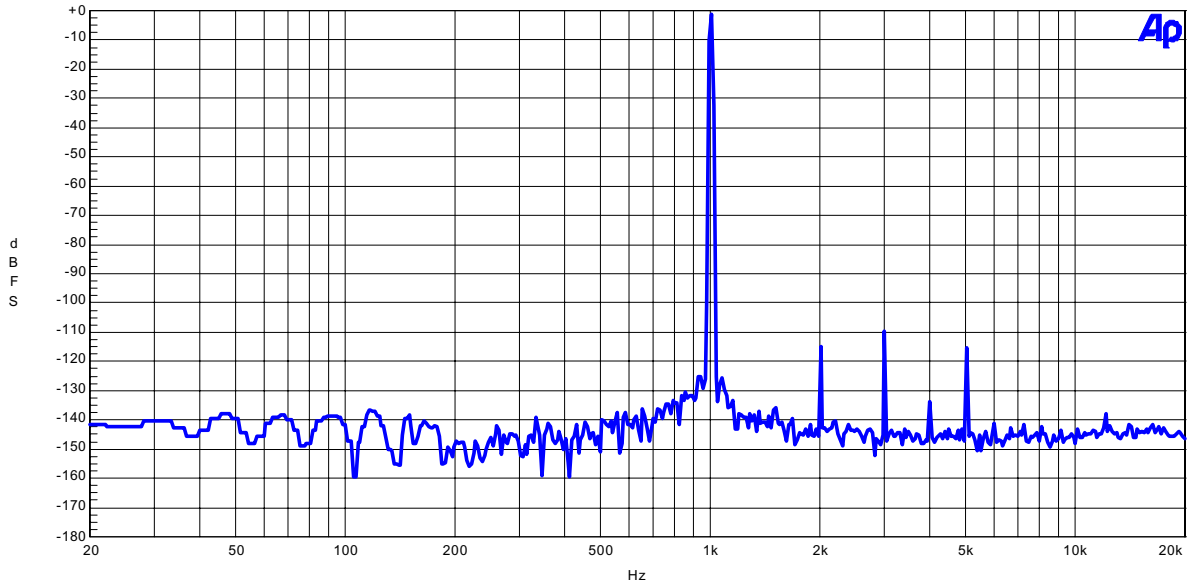


Figure 1-1-1. FFT (1kHz, –1dB input)

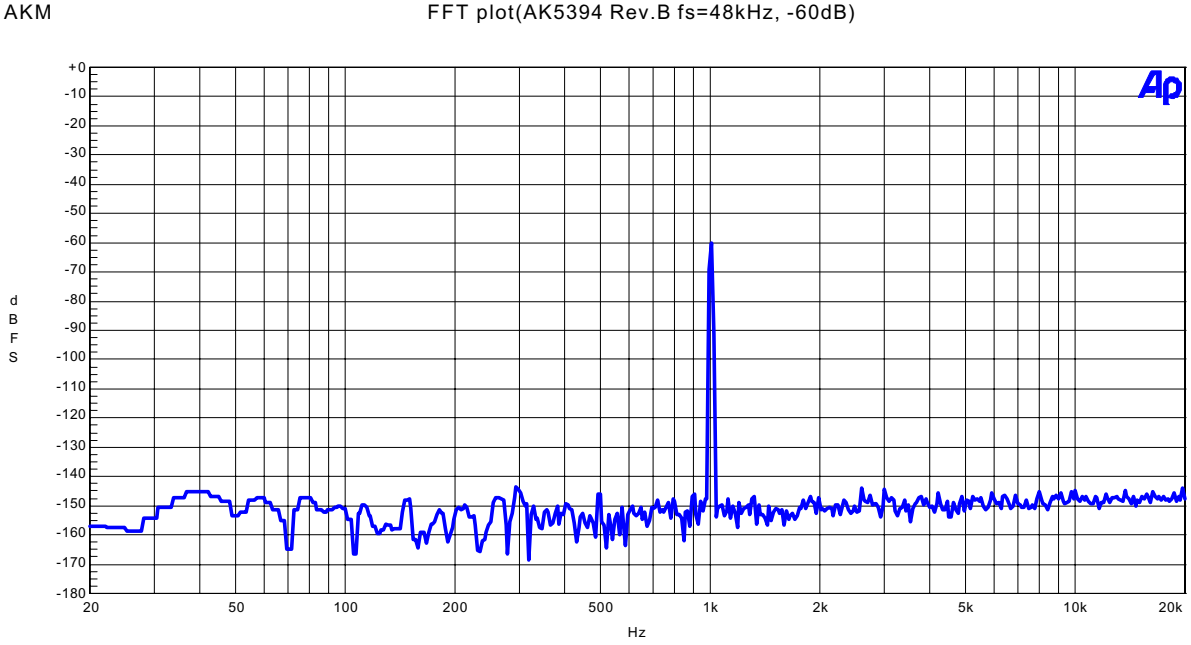


Figure 1-1-2. FFT (1kHz, –60dB input)

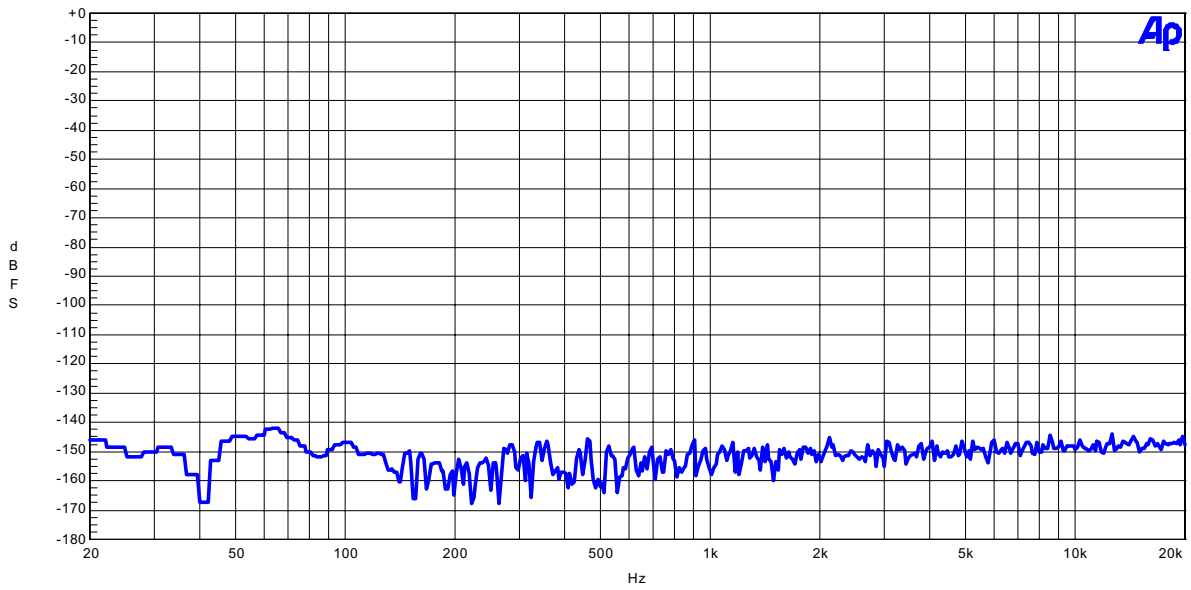


Figure 1-1-3. FFT (off the input)

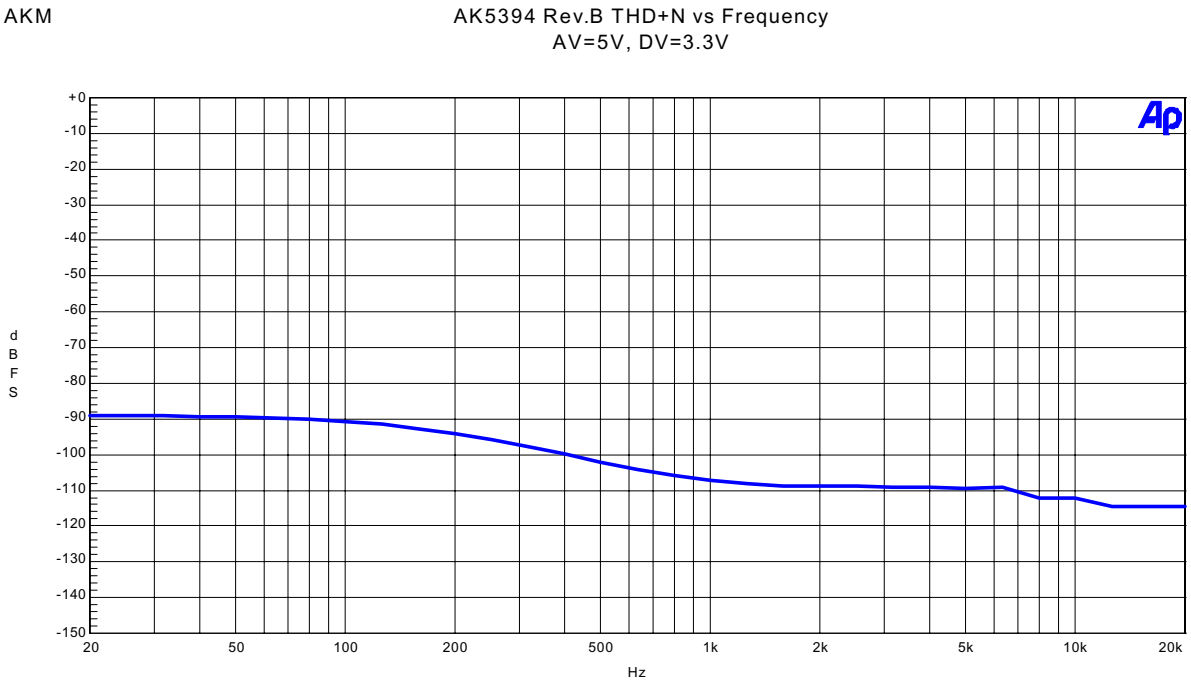


Figure 1-1-4. THD+N vs Input Frequency (-1dB input)

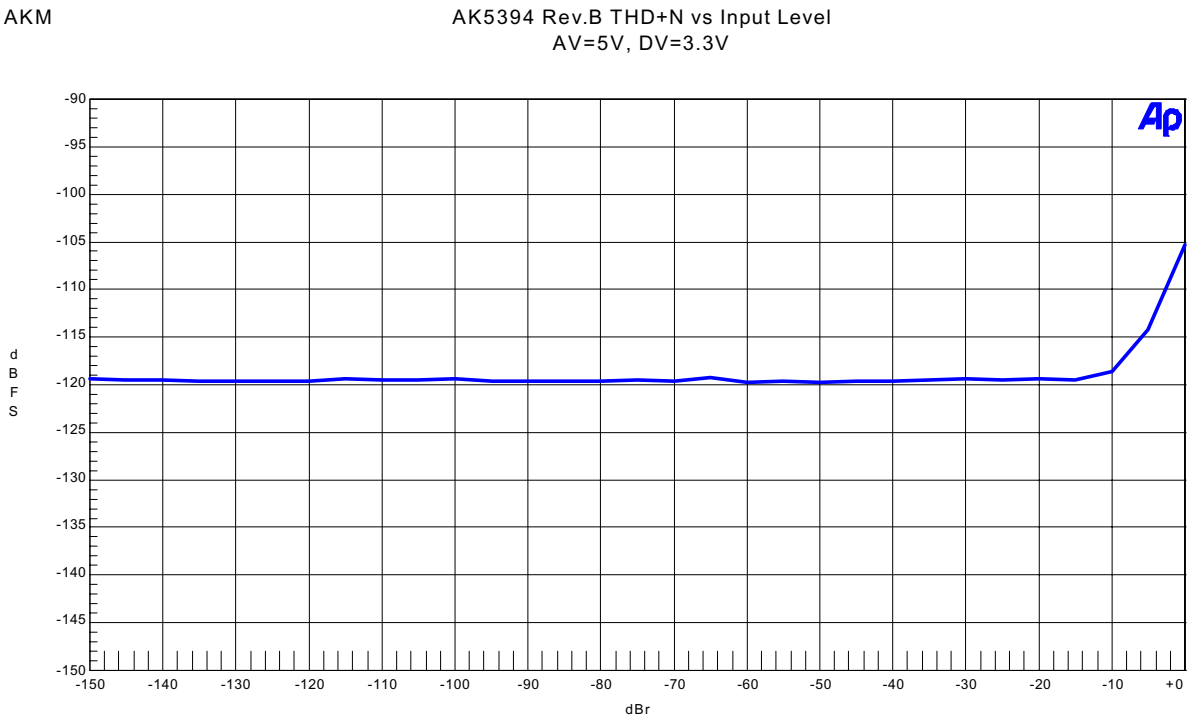


Figure 1-1-5. THD+N vs Input Level (1kHz input)

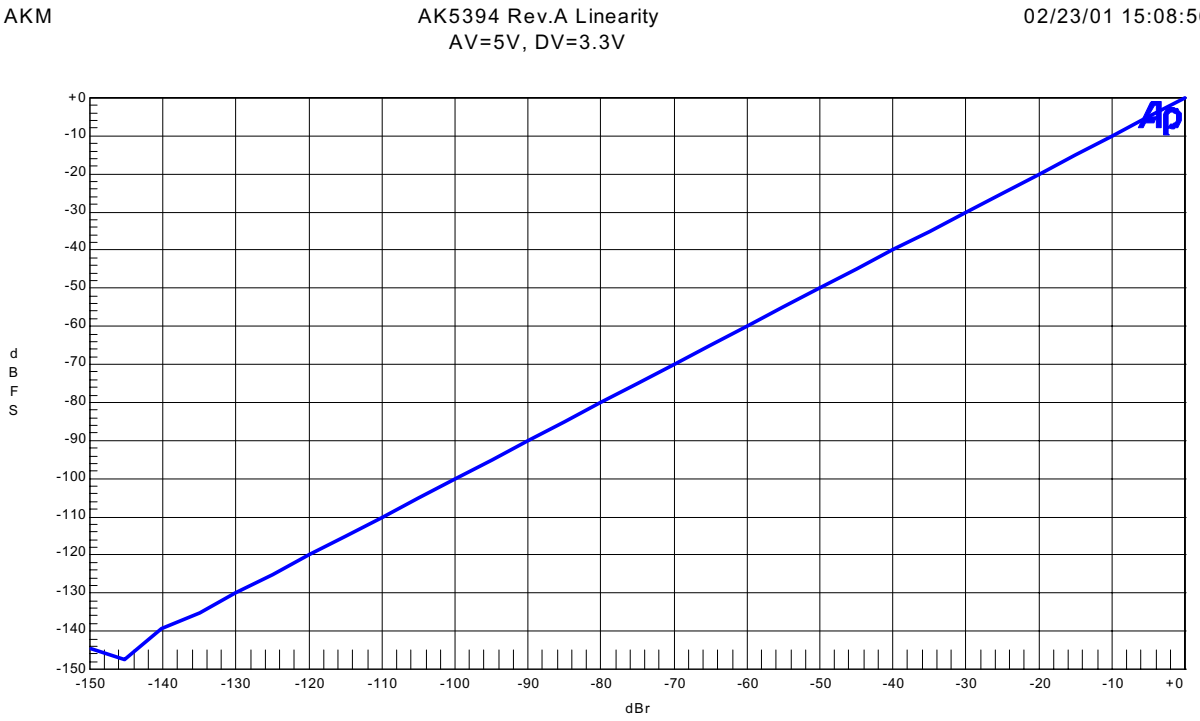


Figure 1-1-6. Linearity (fin=1kHz)

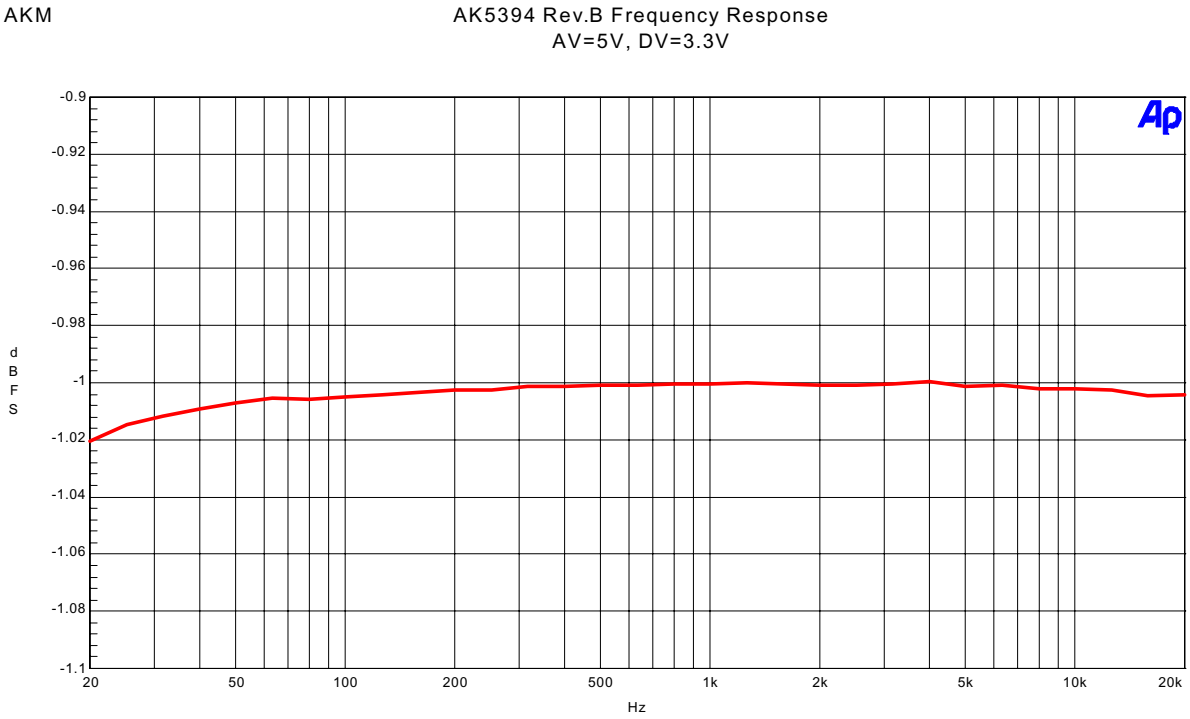


Figure 1-1-7. Frequency Response (-1dB input)

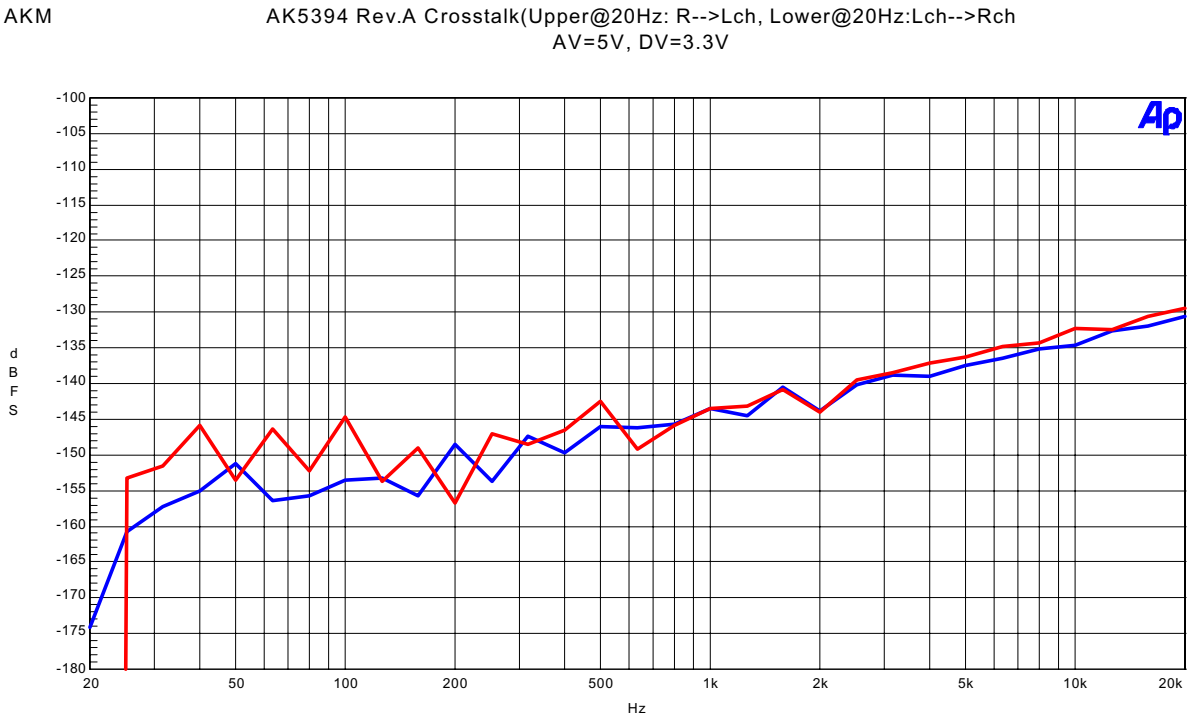


Figure 1-1-8. Cross-talk (-1dB input)

1-2. fs=96kHz

AKM FFT plot(AK5394 Rev.A fs=96kHz)

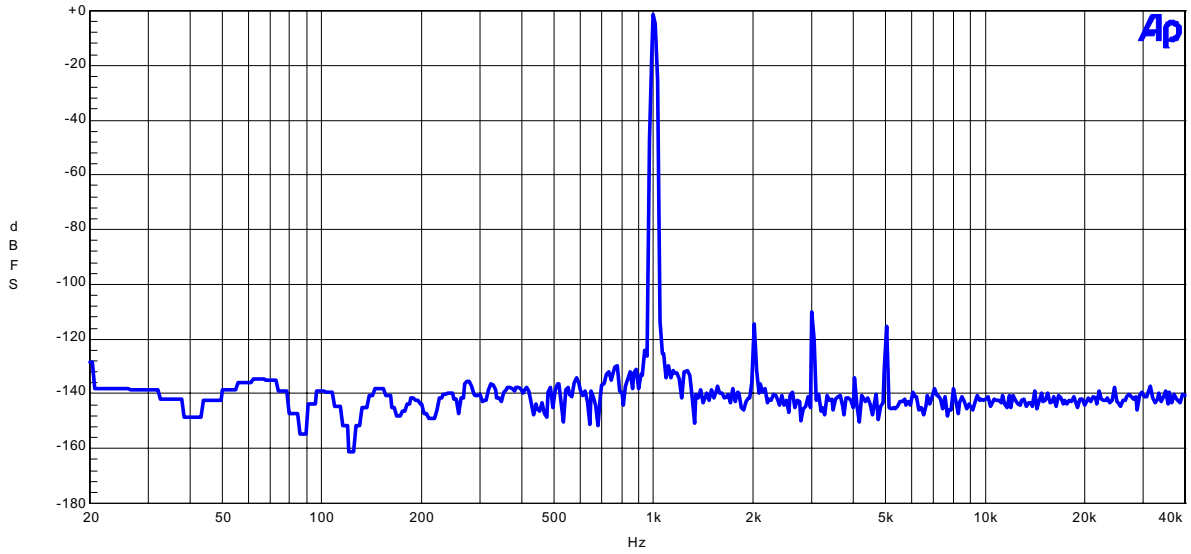


Figure 1-2-1. FFT (1kHz, –1dB input)

AKM FFT plot(AK5394 Rev.A fs=96kHz)

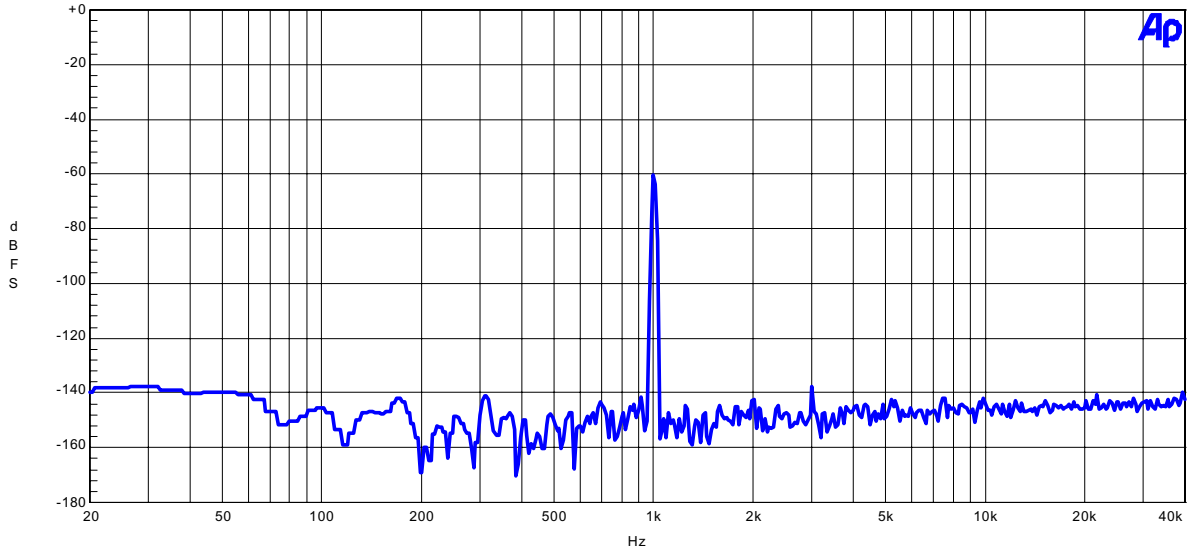


Figure 1-2-2. FFT (1kHz, –60dB input)

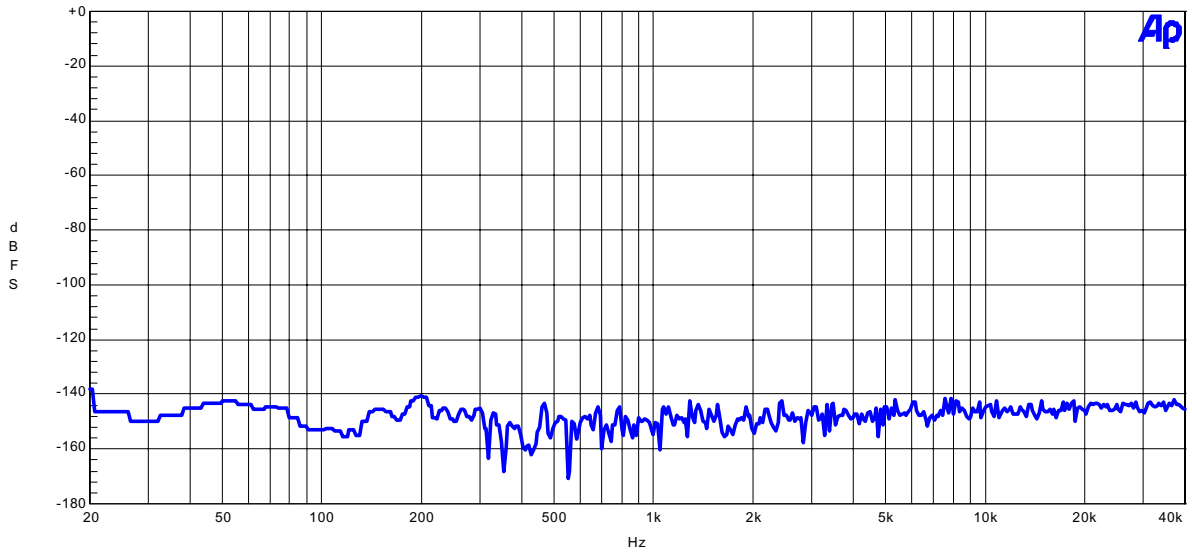


Figure 1-2-3. FFT (1kHz, –60dB input)

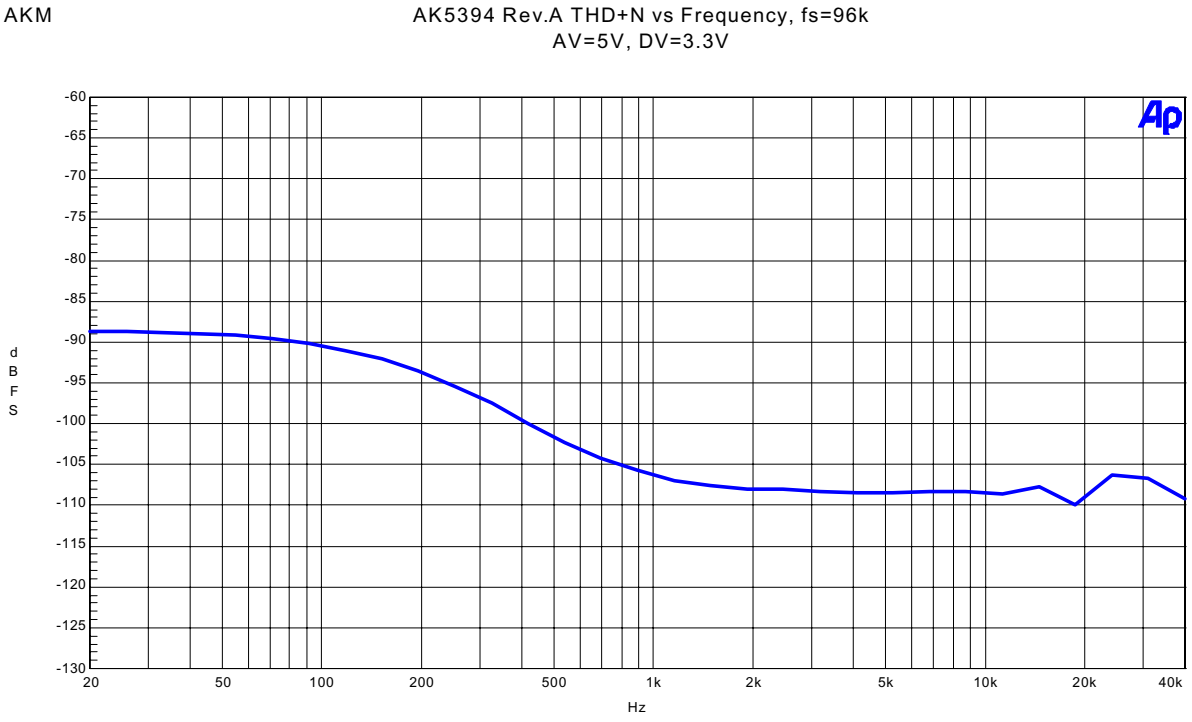


Figure 1-2-4. FFT (off the input)

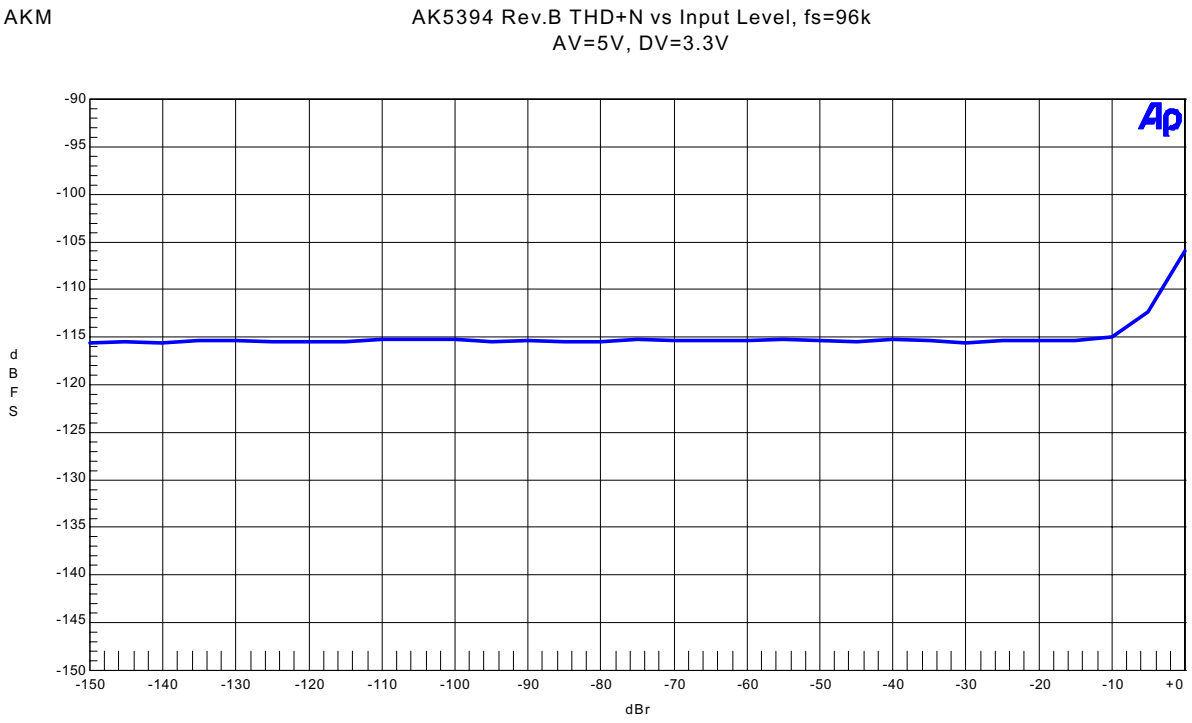


Figure 1-2-5. THD+N vs Input Level (1kHz input)

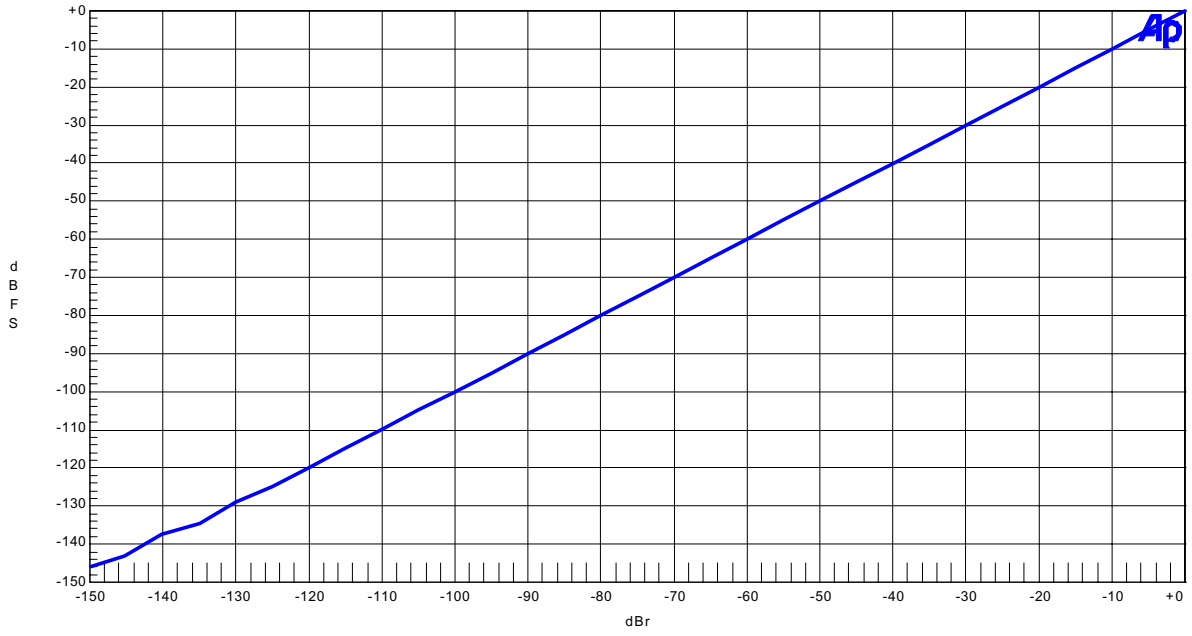


Figure 1-2-6. Linearity (fin=1kHz)

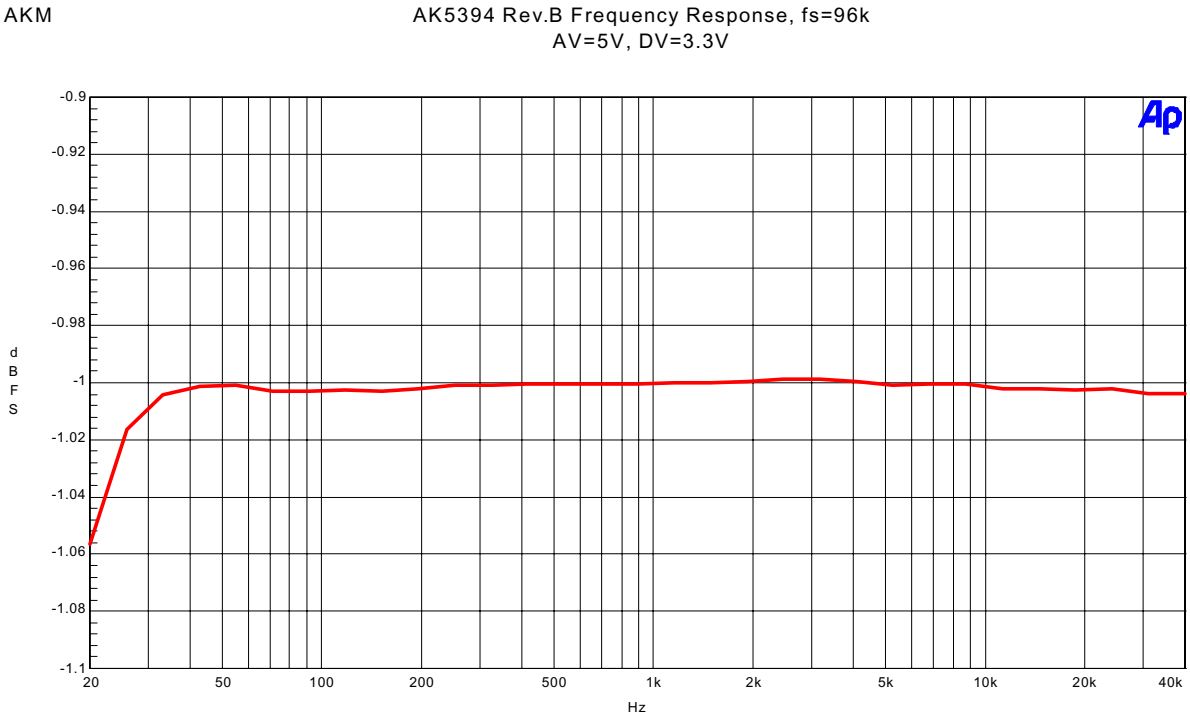


Figure 1-2-7. Frequency Response (-1dB input)

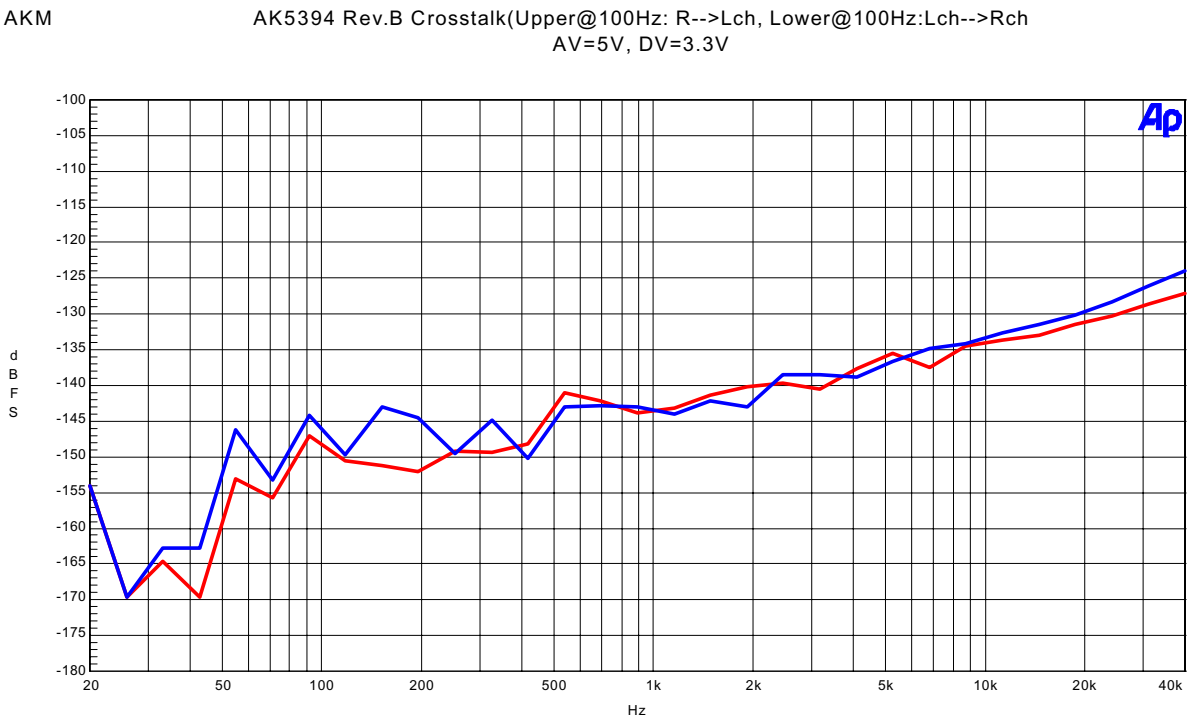


Figure 1-2-8. Cross-talk (-1dB input)

2-3. fs=192kHz

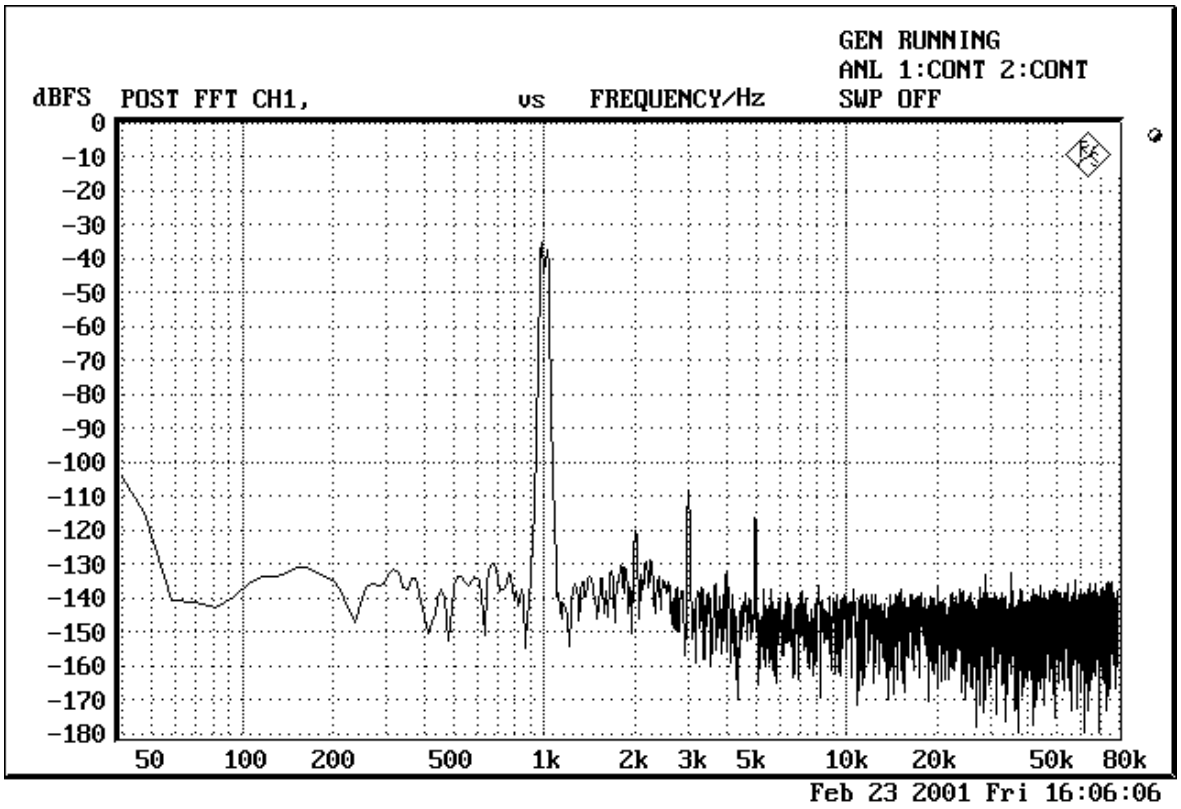


Figure 2-1-1. FFT (1kHz, –1dB input)

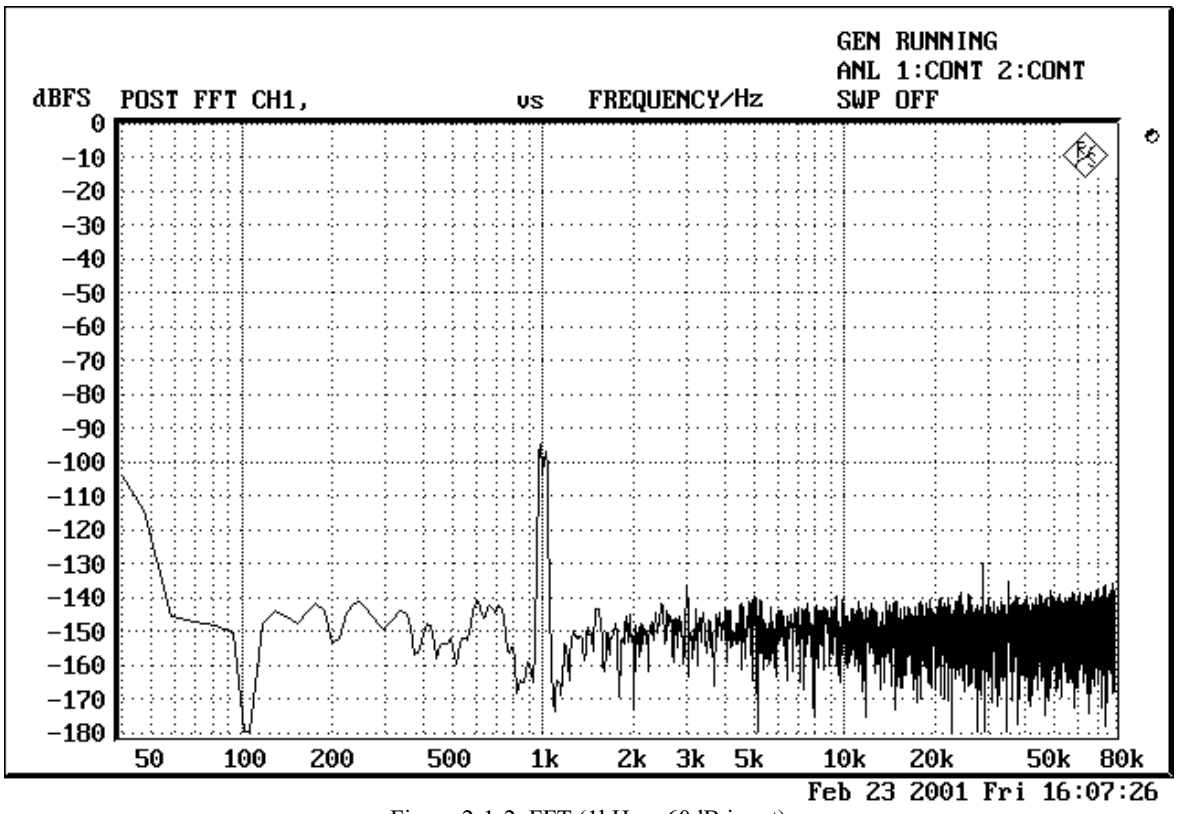


Figure 2-1-2. FFT (1kHz, –60dB input)

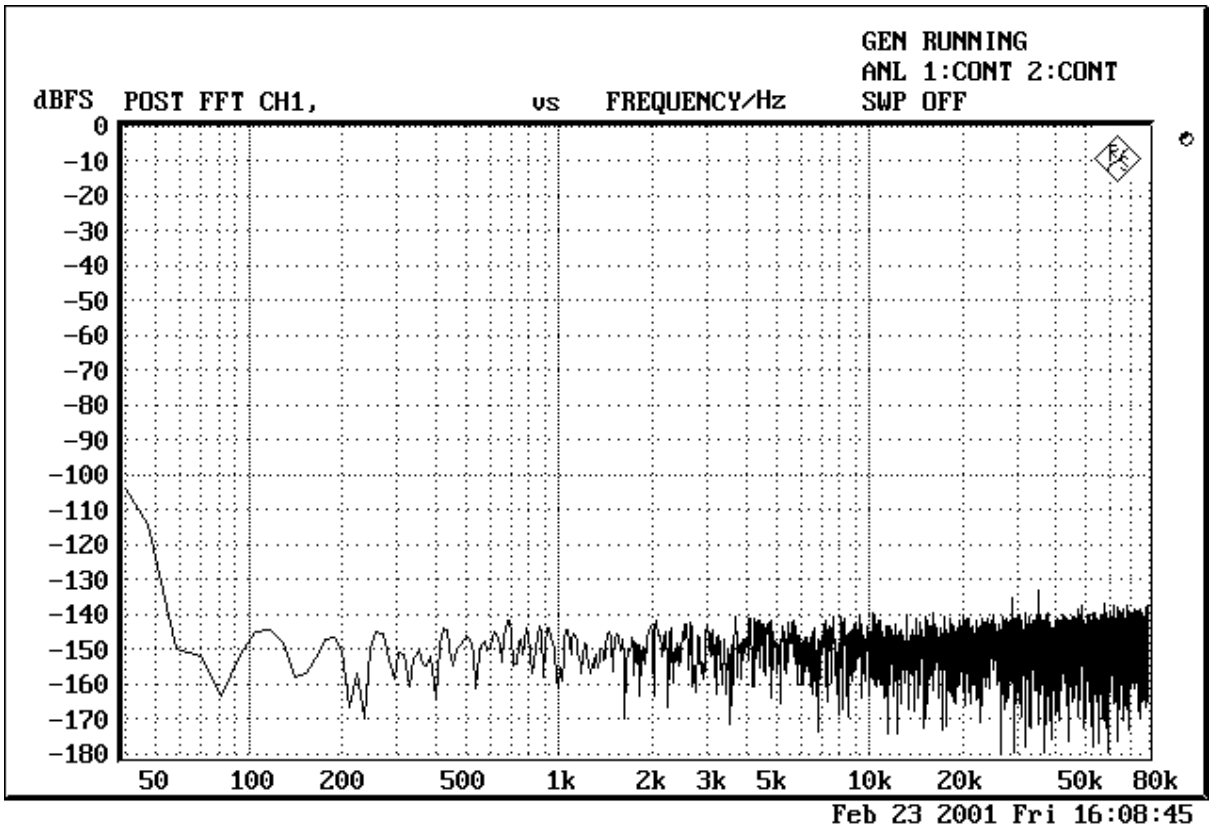


Figure 2-1-3. FFT (off the input)

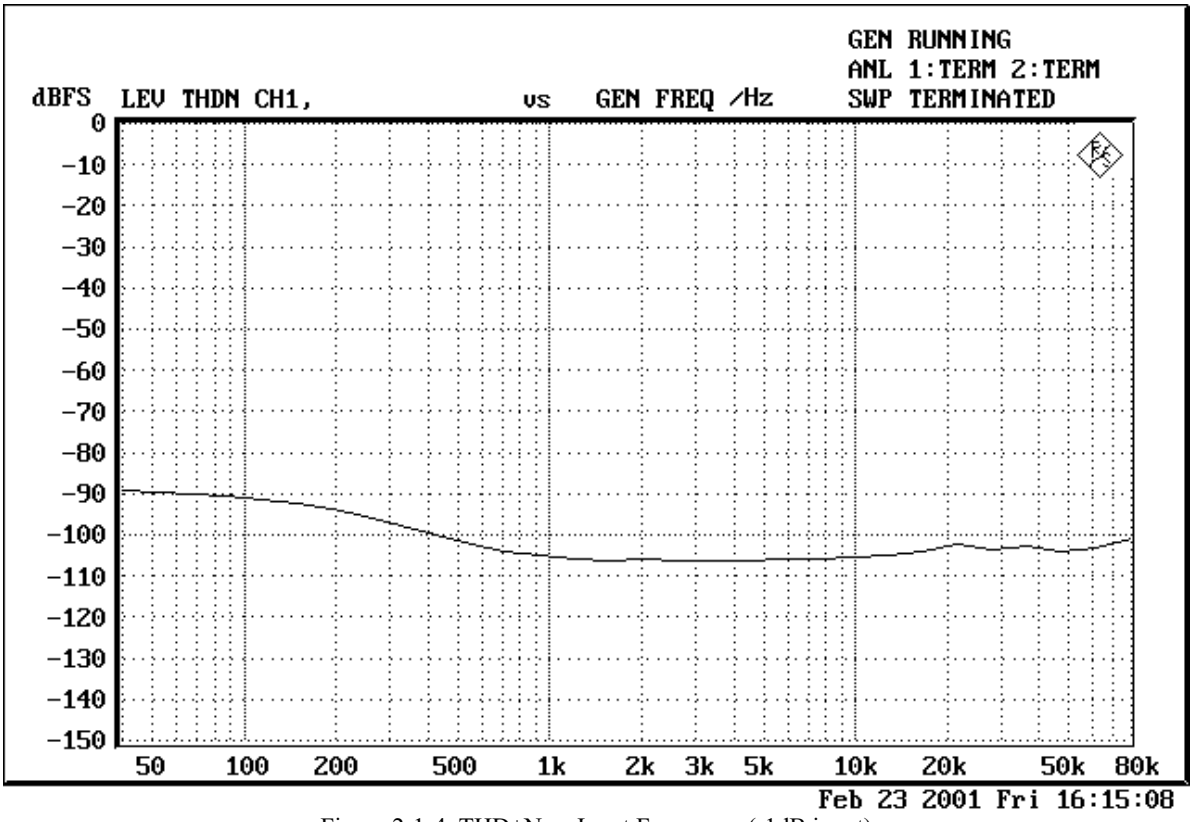


Figure 2-1-4. THD+N vs Input Frequency (-1dB input)

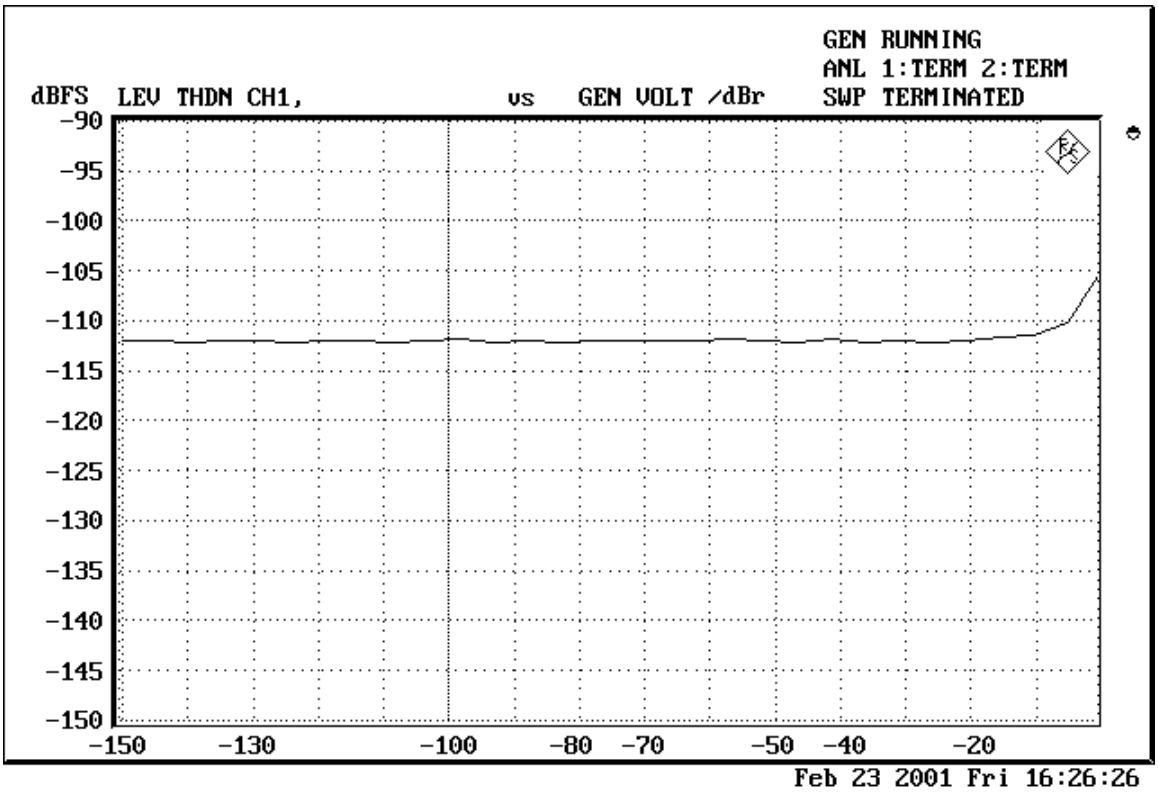


Figure 2-1-5. THD+N vs Input Level (1kHz input)

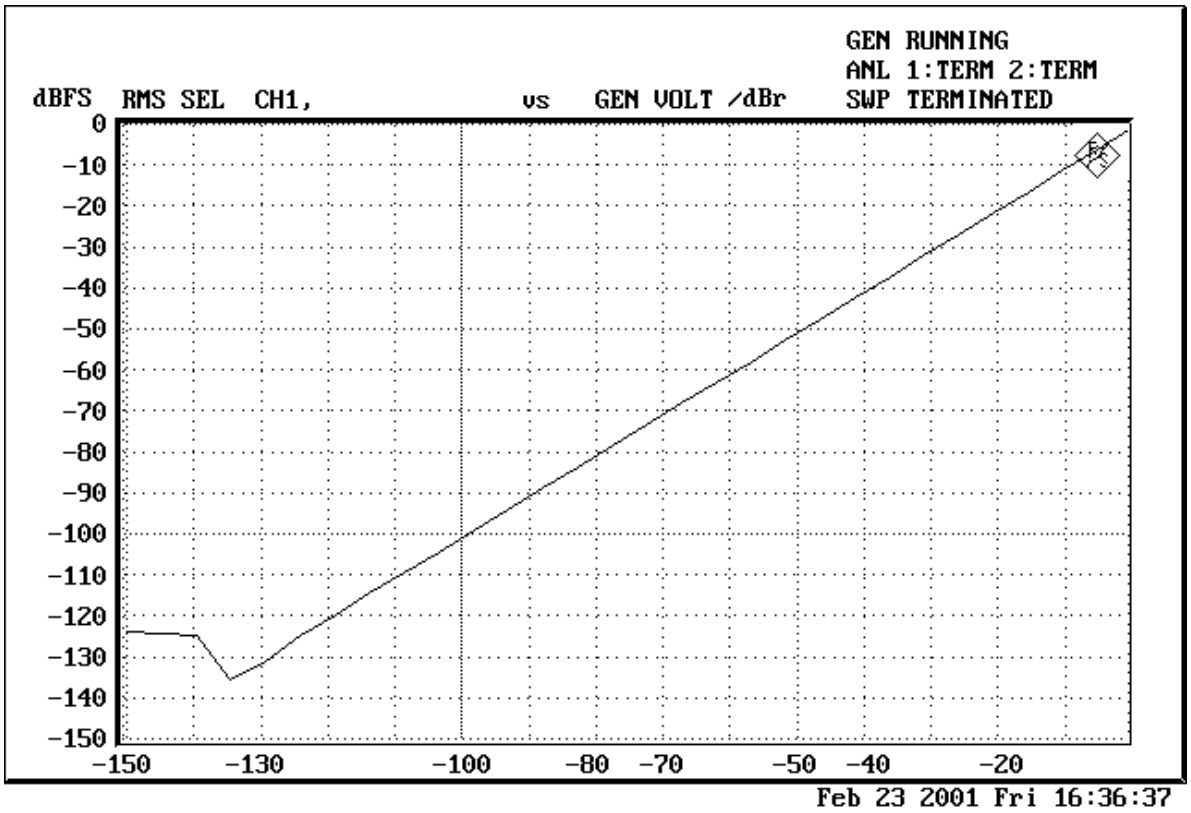


Figure 2-1-6. Linearity (fin=1kHz)

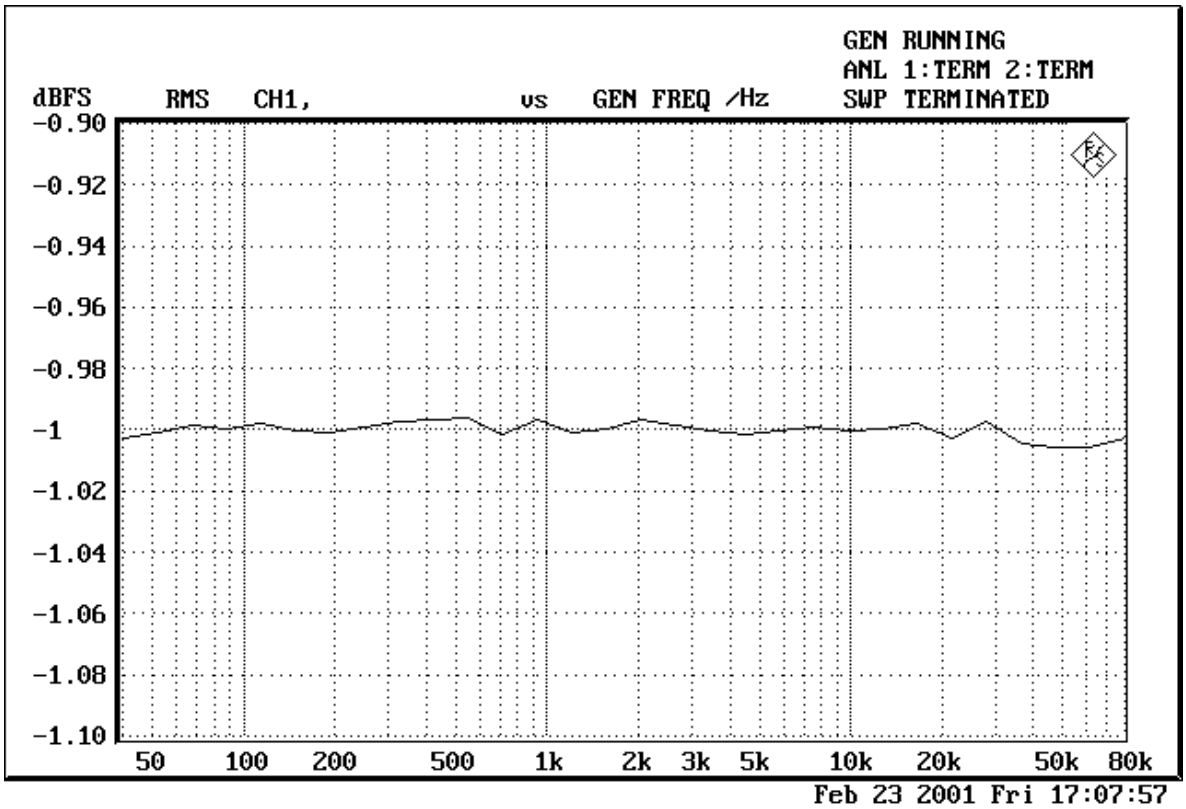
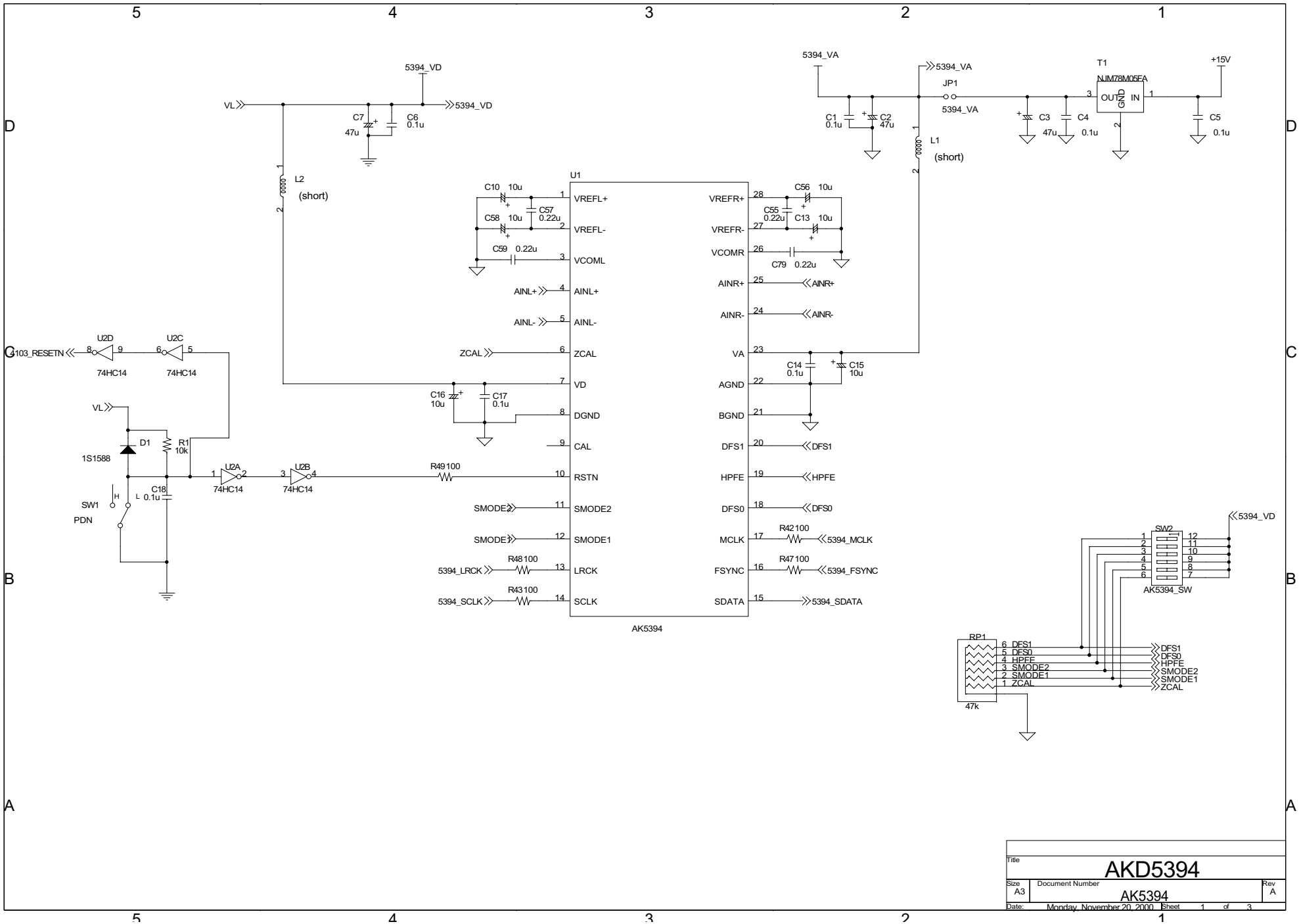


Figure 2-1-7. Frequency Response (-1dB input)



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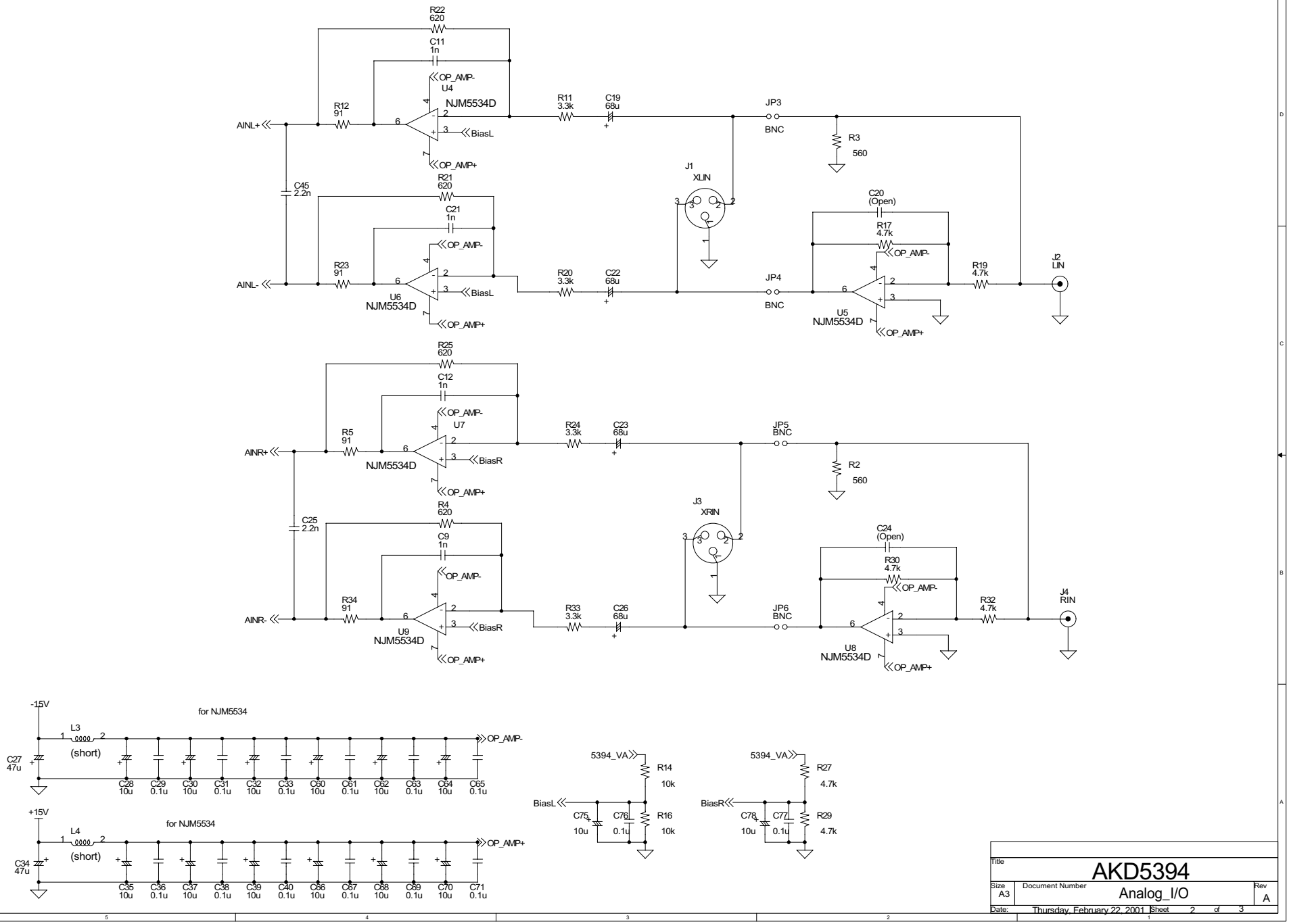

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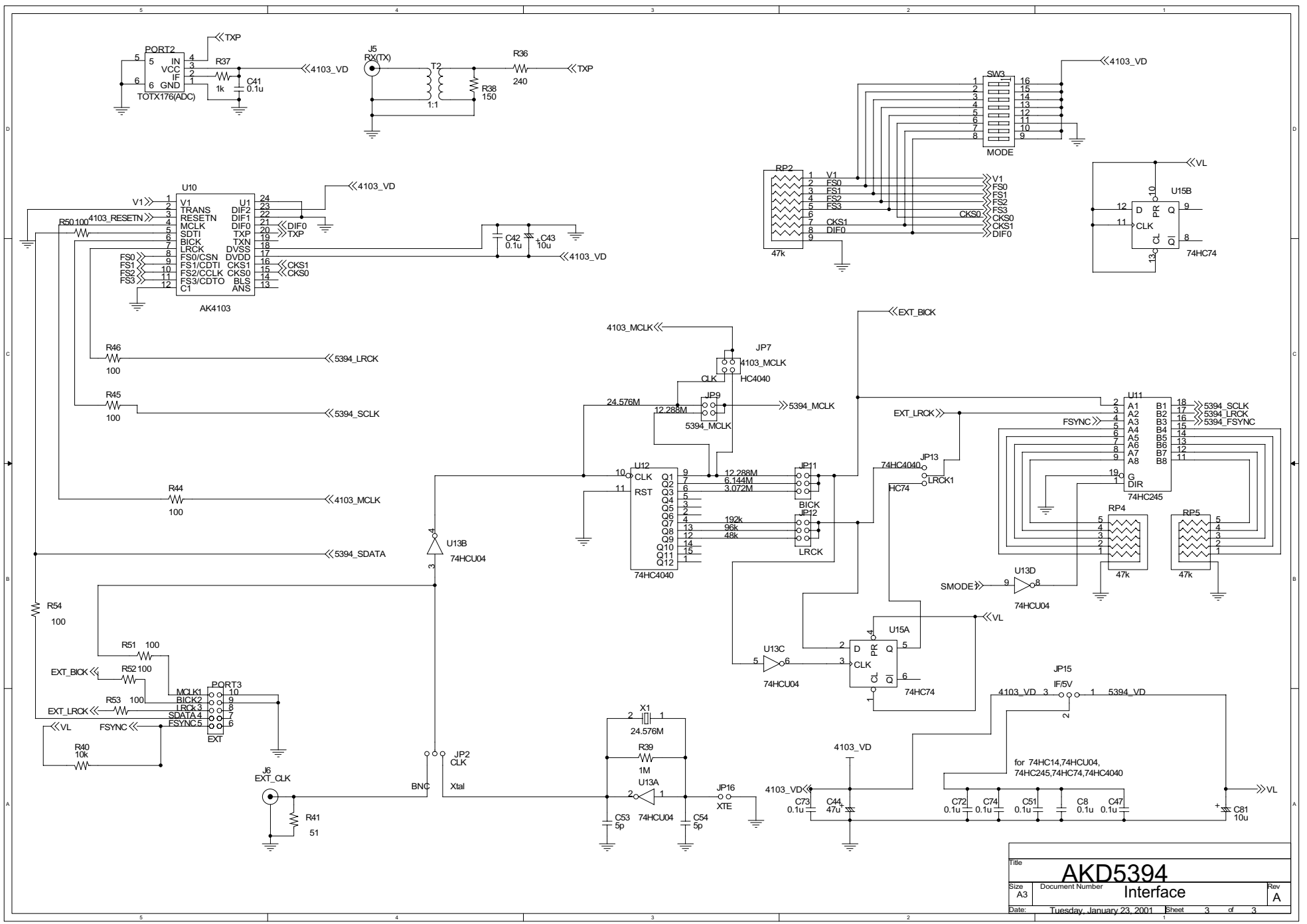
PORT2
TOTX176(ADC)
TXP
R37
1k
C41
0.1u
4103_VD
J5
RX(TX)
T2
1:1
R36
240
R38
150
TXP
SW3
MODE
4103_VD
RP2
47k
V1
FS0
FS1
FS2
FS3
CKS0
CKS1
DIF0
VL
U15B
74HC74
U10
AK4103
4103_RESETN
R50 100
C42
0.1u
C43
10u
4103_VD
DIF0
TXP
CKS1
CKS0
R46
100
5394_LRCK
R45
100
5394_SCLK
R44
100
4103_MCLK
5394_SDATA
4103_MCLK
JP7
CLK
HC4040
JP9
24.576M
12.288M
5394_MCLK
5394_MCLK
U12
74HC4040
RST
12.288M
6.144M
3.072M
192k
96k
48k
JP11
BICK
JP12
LRCK
EXT_BICK
JP13
74HC4040
LRCK1
HC74
U11
74HC245
5394_SCLK
5394_LRCK
5394_FSYNC
FSYNC
EXT_LRCK
RP4
RP5
47k
47k
U13B
74HCU04
U13D
74HCU04
SMODE
R54
100
R51 100
R52 100
R53 100
EXT_BICK
EXT_LRCK
VL
FSYNC
R40
10k
PORT3
MCLK1
BICK2
LRCK3
SDATA4
FSYNC5
EXT
U13C
74HCU04
U15A
74HC74
VL
JP15
IF/5V
4103_VD
5394_VD
J6
EXT_CLK
R41
51
BNC
JP2
CLK
Xtal
X1
24.576M
R39
1M
U13A
JP16
XTE
C53
5p
74HCU04
C54
5p
4103_VD
4103_VD
C73
0.1u
C44
47u
for 74HC14,74HCU04,
74HC245,74HC74,74HC4040
C72
0.1u
C74
0.1u
C51
0.1u
C8
0.1u
C47
0.1u
VL
C81
10u
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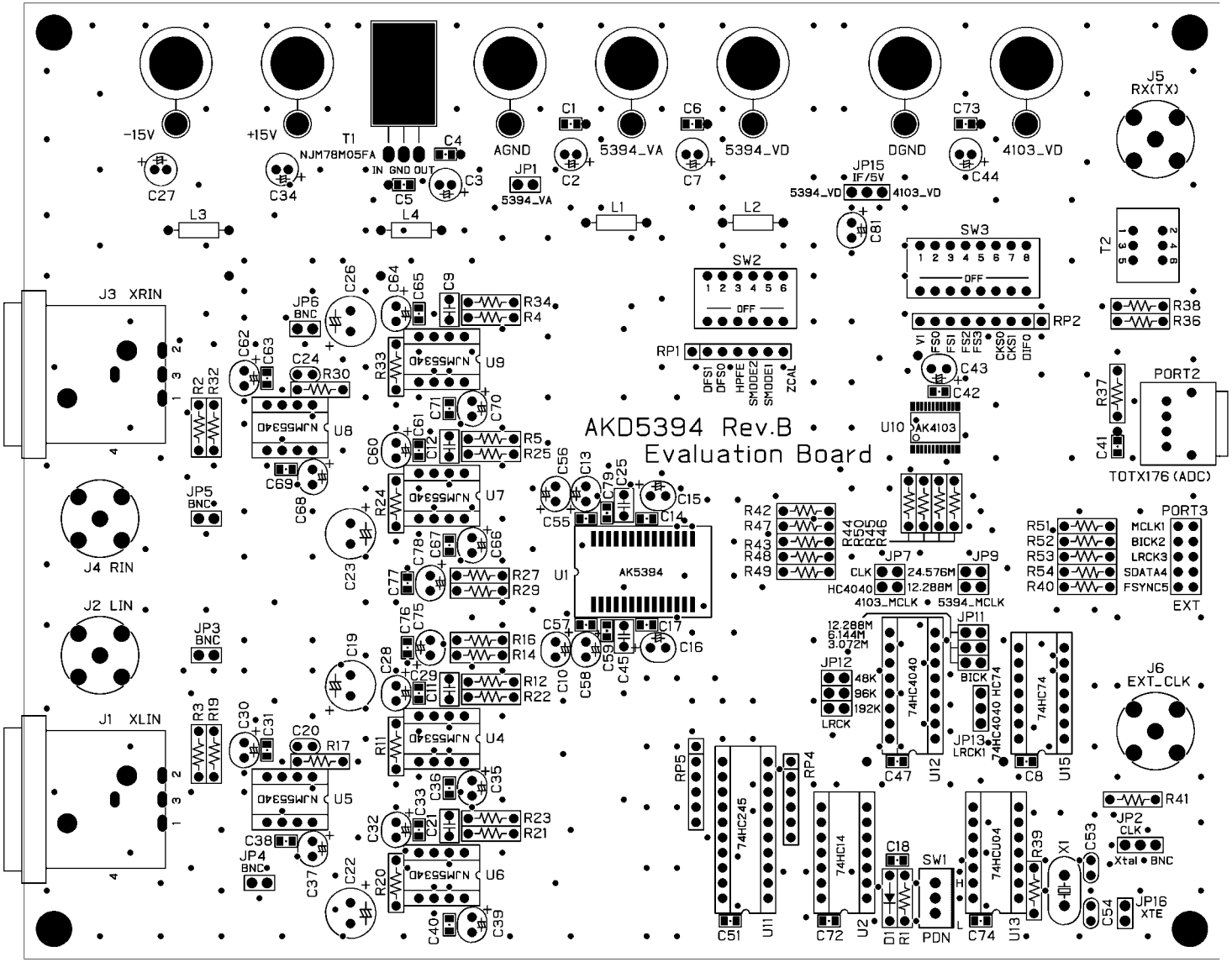

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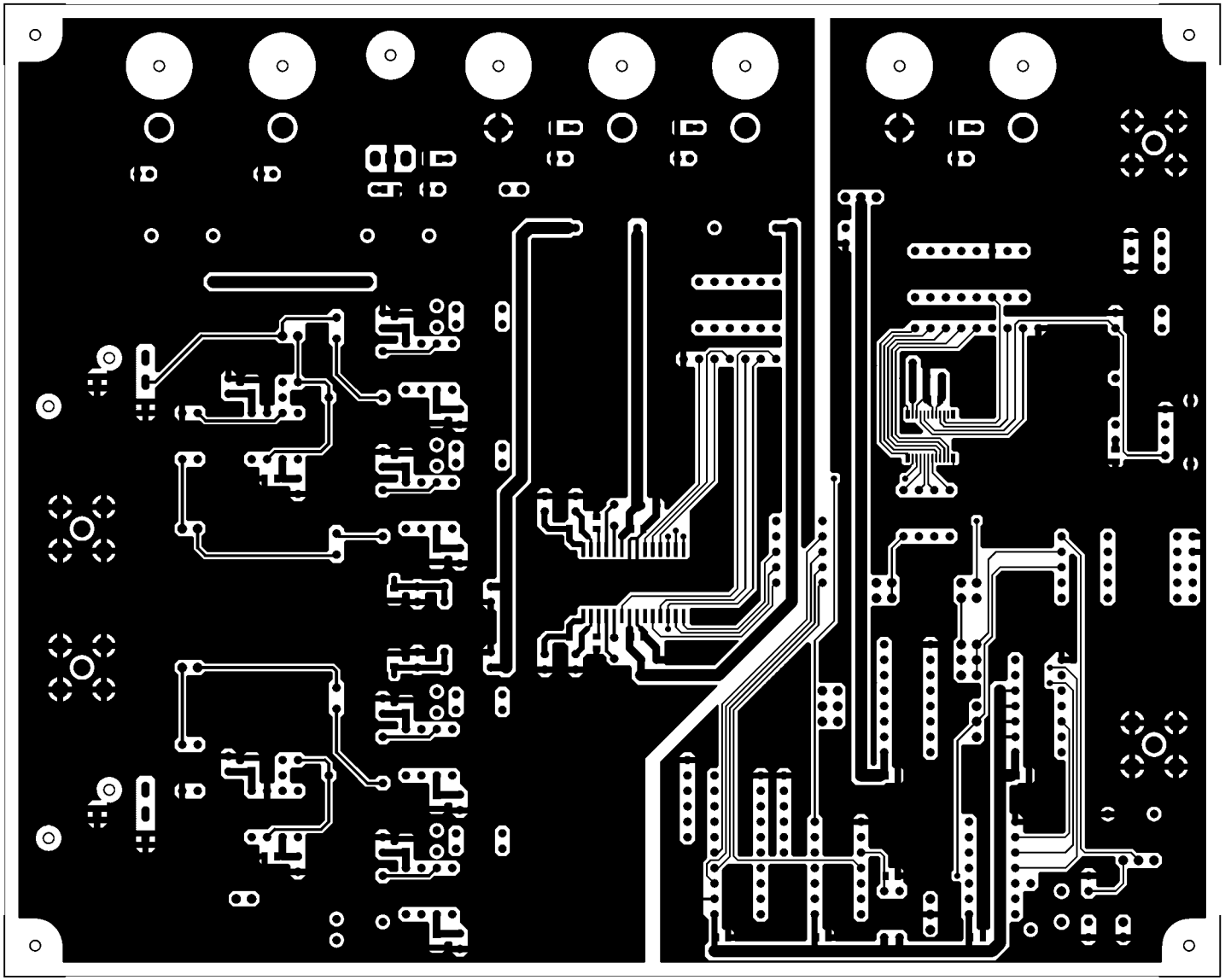

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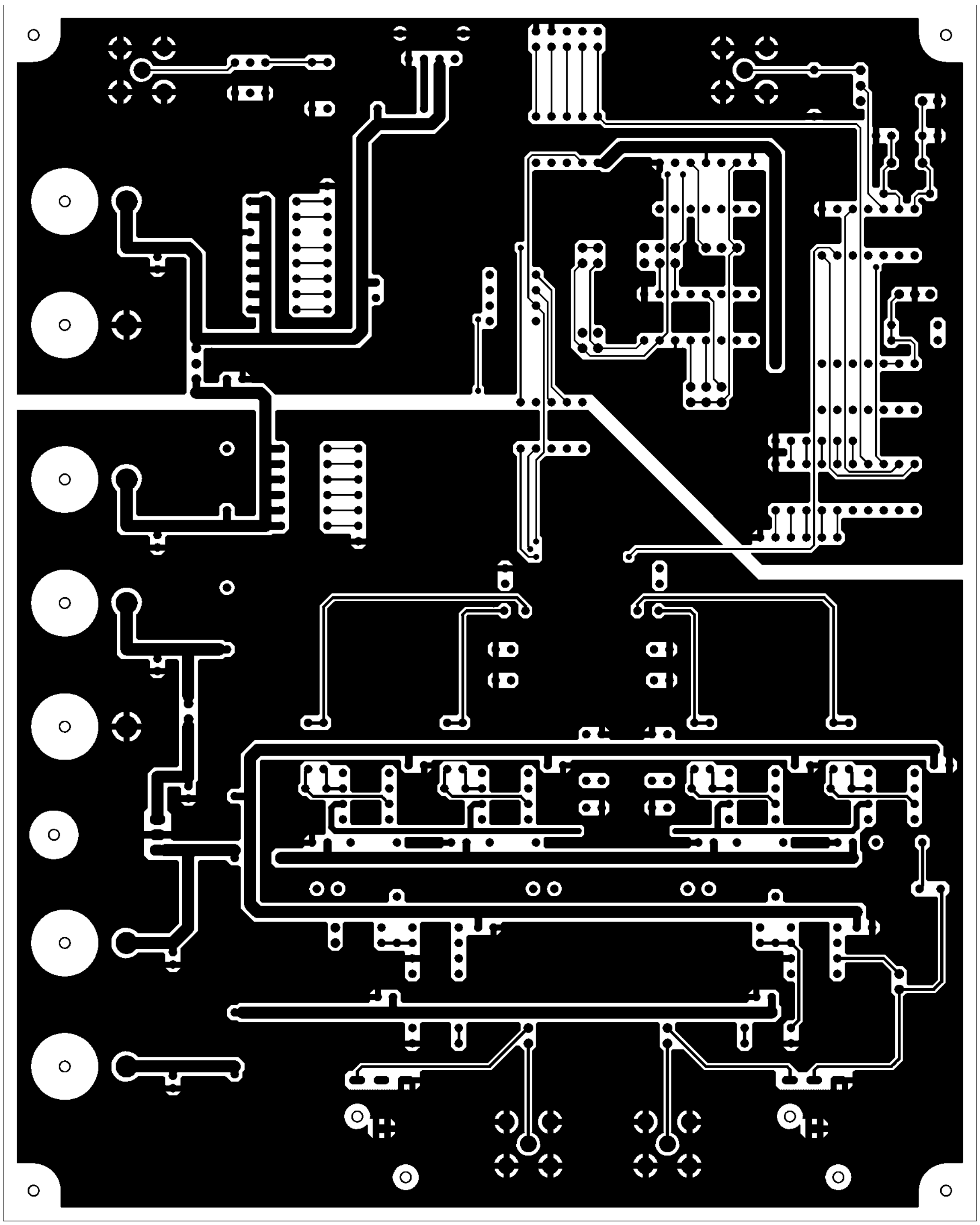

AKD5394 Rev.B L2