

Clock sources: PLL synthesizer vs. XO modules

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Should the new circuit board design or redesign use a crystal oscillator (XO) module or a phase locked loop (PLL) synthesizer as its clock source? Whether a system is a control board within a rack of boards (e.g. multiple line cards), a single board router with switches, a server farm or a site area network, clocks will certainly be required. Could a PLL save board space and lower cost?

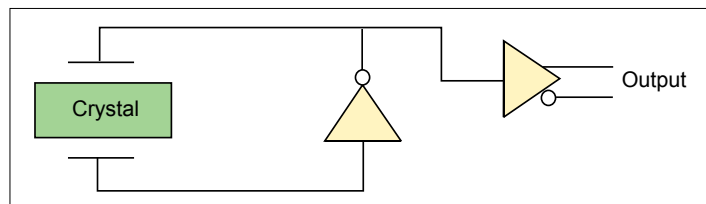


Figure1: A typical crystal oscillator clock must be in a dynamic signal loop with a gain amplifier to compensate for crystal losses.

Generation and distribution of a typical system-timing clock signal comprises functions such as an oscillator source driving a gain amplifier, a translation section to a standard logic level and a clock distribution network. These functions may be accomplished by component chipsets or a highly integrated single package.

The source of a system-timing clock will require a reliable, precision-timing reference, usually a crystal. This article compares two crystal sources—the XO module and the PLL synthesizer—for a system-timing clock. Key characteristics to focus on are cost, board real estate, frequency accuracy and edge jitter or phase noise.

Classic XO

A classic system XO source typically uses a quartz crystal resonator. For oscillator operation, the quartz crystal must properly consider phase shift. It must be in a dynamic signal loop with a gain

amplifier to compensate for crystal losses. The gain amplifier must also drive translation of the signal into standard logic output levels for use by a system clock distribution network, and eventually by clock receivers.

An XO clock is usually available as a hermetically sealed or “canned” module with an internal crystal and integrated circuitry for the translator and output buffer. The XO clock is generally operated at a single frequency and often has only one single-ended logic output pin, or a single com-

plementary differential output pair. Oscillation operation may be done at a crystal fundamental mode or at harmonic overtone modes. For the XO clock, device pin count and package outline footprints are minimized.

XO frequency accuracy (to a spec datasheet target) is typically expressed as a mean with a \pm ppm range of deviation. More accurate XOs tend to be more costly, as do higher-frequency XOs.

A separate characteristic, frequency precision, is expressed by

the number of significant digits and an uncertain deviation range, usually given in ppm. XO clock modules of various levels of accuracy and precision are currently available.

The edge jitter or phase noise of an XO is an independent measure of accuracy and precision. An XO clock module's total clock jitter should be given in picoseconds, while phase noise is only valid when specified over a sideband frequency range.

PLL synthesizer

A more sophisticated system clock oscillator source is the PLL synthesizer clock generator, which offers greater design flexibility and potential cost reduction. Generic PLL synthesizer clock devices usually require an external crystal and offer additional features such as more than one output and output frequencies that are multiples of the singular crystal frequency. By “up-multiplying” crystal oscillation, much higher harmonic frequency signals become available to a system. With additional internal “down-divider” circuitry, chains of lower frequencies are made available as outputs. Furthermore, selectable inputs could switch the wide range of outputs to active (enabled) or inactive (disabled) in banks.

Advanced chip circuit integration allows a PLL synthesizer device to offer wide fan-out ca-

pability for distribution of clock signal copies. For example, a PLL synthesizer could offer 20 complementary differential output pairs, or run up to 40 single-ended clock receivers. Selectable bank fan-out Enable capability can be combined with selectable up-multiplying and down-dividing for extensive output flexibility in a single package.

Common to all PLL outputs, the VCO output phase delay error approaches zero with respect to the input (crystal) reference signal (zero phase delay buffering). When the PLL feedback loop is externally accessible, the output edge phase error is adjustable. This allows selected phase-edge placement within a given range, including zero delay.

During operation, the PLL synthesizer's quartz crystal must also be in a loop with a gain amplifier to compensate for crystal losses and to translate impedance, similar to an XO. Since the PLL frequency synthesizer is locked in phase and frequency on the crystal signal, it retains the crystal's specified frequency accuracy and precision range at the crystal input frequency. When up-multiplied in frequency in a PLL synthesizer, the accuracy deviation expressed in ppm remains a constant, while the absolute range values are also multiplied. A 10MHz \pm 20ppm source can be up-multiplied by 10x in a PLL to

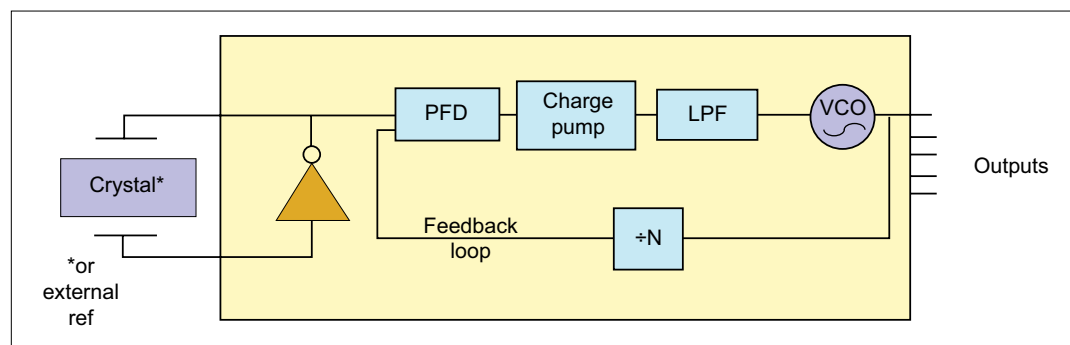


Figure 2: PLL synthesizer clock devices usually require an external crystal and offer additional features such as more than one output and output frequencies that are multiples of the singular crystal frequency.

become a 100MHz ± 20 ppm signal. Frequency up-multiplying or down-dividing in the PLL has little effect on frequency precision.

Similar to the crystal oscillator module, the PLL synthesizer output edge jitter or phase noise is an independent parameter of output accuracy and precision. The PLL synthesizer output will present an additive total jitter compared to the crystal input reference signal and jitter.

PLL input phase noise with a lower frequency than the PLL loop bandwidth (-3dB rolloff point) will transfer to the PLL with little attenuation, whereas PLL input phase noise with a higher frequency than the loop bandwidth will typically be at-

tenuated at -20dB/decade or steeper. This may allow a PLL synthesizer to reject input jitter, and reduce total jitter and phase noise. Phase noise may significantly shift across the various feedback divider values, thus altering the PLL loop bandwidth. The PLL low-pass filter may be externally available to adjust the loop bandwidth.

PLL's edge

For the same clock application, the PLL synthesizer clock offers the use of a less costly crystal that can operate at lower harmonic frequency compared to an XO module. Typically, higher-frequency crystals are considerably more expensive and may require long

lead times for delivery. Replacing an XO module with a PLL synthesizer could shorten lead times and reduce BOMs.

A design using several XO modules can be analyzed for a common higher harmonic frequency. If this higher harmonic frequency were to be generated instead by a PLL synthesizer and then divided down, the required signal frequencies could be made available to each clock receiver from the PLL synthesizer device, eliminating one or several XO modules. This eliminates the cost of multiple XO modules while freeing up board space.

Next in line for potential elimination would be the various fan-out buffer devices. Depending

on the PLL synthesizer's features, any design formerly using XO modules and a fan-out buffer might benefit from the fan-out integrated into the synthesizer device. Component count and cost go down, while board real estate is reduced.

PLL synthesizer circuitry could also include frequency spectrum, spreading circuitry to reduce EMI. A PLL synthesizer could provide multiple harmonic copies of lower-frequency clock signals with reduced EMI across a system or backplane. Subsequent daughter-card receivers would use a second PLL synthesizer that would generate and distribute local pure, clean signals at higher clock frequencies.