EE-313
Digital MOS Integrated Circuits
INFORMATION SHEET

http://eeclass.stanford.edu/ee313

TIME:	MWF 10:00 – 10:50AM, Gates Building room B03 Delayed broadcast: SITN channel 4, 5:45PM – 6:35PM Review Session: Monday 4:15 – 5:05PM, Skilling Aud (live on E4)
INSTRUCTOR:	Mark Johnson
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Office Hours:	Sunday 14:30 – 16:30 Monday 17:00 – 19:00 Tuesday 14:30 – 18:00
ADMIN:	Ann Guerra
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GRADING:		
	Homework	25% (Due on Wednesdays, no credit for late HW)
	Project	20%
	Midterm exam	25%
	Final exam	30%

REQUIRED TEXTBOOK:	David A. Hodges, H. G. Jackson, R. Saleh, *Analysis and Design of Digital Integrated Circuits*, Third edition, McGraw Hill, 2003
OPTIONAL REFERENCES	Rabey, Chandrakasan, and Nicolic: *Digital Integrated Circuits*, 2nd edition Sutherland, Sproull, and Harris: *Logical Effort, Designing Fast CMOS* Weste and Eshraghian, *Principles of VLSI Design*, 2nd edition
CLASS WEBSITE	http://eeclass.stanford.edu/ee313

BULLETIN BOARD

We encourage the use of the bulletin board located on the eeclass website. It will serve as an important tool for communication. However, the teaching staff will definitely NOT support the usenet newsgroup named " su.class.ee313 "

PREREQUISITES

EE-101A, EE-101B, EE-108A

You are assumed to have been exposed to poles and zeroes, basic bipolar and MOS device physics, large-signal and small-signal circuit models, linear systems analysis using the Laplace transform, Boolean algebra, digital logic design (both combinational and sequential circuits), and CMOS logic gates. If you are unsure about whether your background is adequate, look through the textbook. If it appears that the text assumes a significantly deeper background than you possess, you may wish to defer EE-313.

ANSWERS TO FREQUENTLY ASKED QUESTIONS

See attached.

COURSE CALENDAR

(subject to minor changes)

05 Jan	1	Course introduction; review of CMOS gates		HW1 out
07 Jan	2	RC Trees; Pass Transistor Logic		
10 Jan	3	RC Trees; Parameter Extraction; Delay Optimization		
12 Jan	4	More on Delay Optimization; the method of Logical Effort		HW2 out
14 Jan	5	Introduction to Semiconductor Memories		
		(MLK Jr. holiday on Monday)		
19 Jan	6	Logical Effort for memories; Ratioed logic; Power in CMOS		HW3 out
21 Jan	7	Gates with lower Logical Effort		
24 Jan	8	Long Channel MOS model		
26 Jan	9	Short Channel MOS model		HW 4 out
28 Jan	10	Using MOS Models: improved delay analysis		
31 Jan	11	Improved Capacitance Modeling		
02 Feb	12	What makes a gate Digital; transfer functions/noise margins		
04 Feb	---	MIDTERM EXAM in Terman Auditorium from 10:00 till 10:50		
07 Feb	13	SRAM design: Bitline capacitance and delay		
09 Feb	14	SRAM design: Column I/O circuitry		HW 5 out
11 Feb	15	SRAM design: static sense amplifiers		Project out
14 Feb	16	SRAM design: Cell margins, a closer look at "noise"		
16 Feb	17	Discussion of Project I		
18 Feb	18	SRAM design: Low Power techniques		
		(President's Day holiday on Monday)		
23 Feb	19	SRAM design: timing generators	Project I due	Project II out
25 Feb	20	SRAM design: lower power using low-swing gates		
28 Feb	21	Advanced clocked circuits		
02 Mar	22	Threshold voltage and subthreshold conduction	Project II due	Project III out
04 Mar	23	Voltage and technology scaling		
07 Mar	24	DRAM overview		
09 Mar	25	Memory evolution and structure; ROM and EEPROM		
11 Mar	26	Class summary, project discussion. Last day of classes.		Project III due
17 Mar	---	(Thursday): Final exam, 8:30 to 11:30, Terman Auditorium		

EE-313 ANSWERS TO FREQUENTLY ASKED QUESTIONS

Q1: *What is the homework policy?*

A1: Homework assignments will be handed out in class (10:00AM) on Wednesday and are due in class (10:45AM) the following Wednesday. Homework is considered "late" if it is handed in any time after 10:46AM on Wednesday. No credit will be awarded for late homework. That means zero. Solutions will be provided within ($\leq$ 3 days), after the homework is due.

Q2: *What is the homework policy for SCPD students?*

A2: Homework is "on time" (not late) if it gets picked up and shipped out in Wednesday's SCPD courier pouch. It must be picked up on Wednesday. Or, if your courier pickup occurs very early in the day, SCPD students are allowed to FAX their homework to SCPD and it will be "on time" (not late) if sent before 2:59PM Pacific Standard Time on Wednesday. No credit will be awarded for late homework. That means zero. Please DO NOT submit your assignments twice.

Q3: *I'm having trouble doing the homework, what can I do?*

A3: Attend the review session. We have arranged it to be on Monday afternoon which is an optimum time. You've recently worked on the problem set (over the weekend) and you still have 2 nights + 1 day left before the homework is due on Wednesday.

Q4: *I'm taking the quals; can I turn in the homework late, or do some different assignment ?*

A4: No. No credit will be awarded for late homework. No extensions will be granted. Compared to the rest of the homework assignments for EE-313, homework #1 is (intentionally) quite easy.

Q5: *It's inconvenient / unpleasant / difficult / impossible for me to use HSPICE and Sue, can some other arrangements be made?*

A5: No. You can remotely login to Stanford computers and use HSPICE + Sue. The SCPD TA's and the EE-313 CA's can show you how.

Q6: *I am an SCPD student and I must get a grade of B or higher, otherwise I have to pay. Can you guarantee that I won't have to pay?*

A6: No, of course not. You will receive the grade that you earn. You might earn a low grade and in that case, you will have to pay. No extensions or exceptions will be granted, not even for unexpected customer visits, tape-outs, design reviews, or unforseen demands at work.