Global negative feedback and error correction topologies

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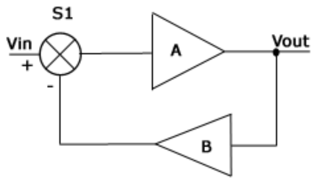

Fig. 1 Cannonical feedback topology

Gain and sensitivity to plant equations for conventional negative feedback and error correction corresponding respectively to fig. 1 and 3. are:

Global negative feedback:

$$G = \frac{A}{1+AB} \qquad S_A = \frac{dG/G}{dA/A} = \frac{dG}{dA}.\frac{A}{G} = \frac{1}{1+AB} \qquad [1]$$

So $S_A \to 0$ with $AB \to \infty$

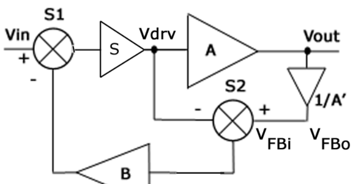

Fig. 3 Alternate topology including real active element models

Error correction:

$$G = \frac{AS}{1+ASB(1/A'-1/A)} \qquad S_A = \frac{dG/G}{dA/A} = \frac{A'}{A}.\frac{1/S-B}{B+\frac{A'}{A}(1/S-B)} \qquad [2]$$

So $S_A \to 0$ with $1/S - B \to 0$

From [2] it can be seen $S_A \cong 1/S - B$ to a good approximation, and this is what we seek to minimize.

In Fig. 3 we have included block *S* to denote some form of active network must be present in order to be able to adjust for near cancellation. We also included a plant *A* of arbitrary gain for generality. It can be seen there is a positive feedback loop formed by S1-S-S2-B, while if we abstract the dual summing nodes and consider a regular feedback topology breaking the loop between 1/A’ and S2, then the equivalent loop gain is given by:

$$G_{OL} = V_{FBo}/V_{FBi} = -\frac{1}{A'}\frac{AB}{(1/S-B)} \qquad [3]$$

So as expected the same cancellation condition $1/S - B \to 0$ leads equivalently to an infinite loop gain.

Why error correction is conceptually different from negative feedback?

Negative feedback accepts an error and seeks to null it only asymptotically with infinite loop gain.

Error correction actively seeks to null error by comparing plant input and output, and feeding back only the error. If the plant were perfect and *A=A’* there should be no output at S2.

In actual practice, both approaches of course do not accomplish full correction. For negative feedback simply there are no means of achieving infinite gain. For error correction, there is also no way of nulling $1/S - B$, both because of practical adjustment constraints, and more fundamentally because at least one of the terms is complex, meaning the difference cannot be made 0 for any frequency except DC.

Though the circuit complexity as derived from Fig. 3 may seem overwhelming as compared to Fig. 1, in actual implementations the differences are almost insignificant.