R5, R6 to recover loss in open-loop gain due to the lower Yfs. Examples of such devices are 2SK117, 2SK209 (SMD version), or 2SK332E (dual version). The latter is also already obsolete, but still can be found in small quantities, and saves the trouble of matching. The 2SK209 is in active production and widely available. The SOT23 SMD package does make matching more difficult, even with a suitable test socket.

Borbely used a pair of J508 current regulating diodes to make up a 4.8mA CCS. The closest equivalent today would be 2x Semitech E202 in parallel, or a single E452, or a 1N5314 from Central. All three are rather expensive, but they guarantee a known tolerance of the constant current, and save the need to measure and trim. However, there are no noise specification on these. So there is no reason why an experience builder cannot replace them with a pair of 2SK209s, each with a source resistor to trim the current of each JFET to 2.4mA. One can then be sure then the resulting CCS is low noise. It is a choice between performance and convenience.

Output Stage – Lateral MOSFETs vs Vertical MOSFETs

Borbely said in his interview with Jan Didden,
"For me these (Hitachi lateral MOSFETs) sound the best of all MOSFET types. At low bias, they sound kind of soft, and come very close to tubes. They have relatively low Gm but the negative tempco is a plus. Vertical types such as the Toshibas have higher Gm but a positive tempco, which makes it more difficult to stabilize the quiescent conditions. They can sound quite good as well, especially in the bass department, although for full-range I would always prefer the Hitachi's. And the Hitachi's can sound good with only 100mA, while the Toshibas would need at least double that.

I don't like the IR-type power MOSFETs, although they have a very high Gm. When I used them, I had an extra identical device on the heatsink as the bias regulator to keep the positive tempco under control. They measure well but they are not my favourite for sound quality, unless you go to very high bias currents or other topologies ….."

You hear similar comments from other prominent audio designers, such as Charles Hansen, and Thorsten Loesch [12]. The claim of better linearity of the laterals has been discussed controversially for decades, but it is a fact that that they have much lower capacitances. And more importantly the capacitances are constant with varying Vds. The net result : while the distortion level of those variants using V-MOS rises almost proportionally with frequency, that for the original Borbely is more constant over the audio band,.

One can argue that the same constant capacitances can be achieved by cascading vertical MOSFETs. Which is true to an extent, but the penalty is loss of voltage headroom. On top of that, the capacitances of vertical FETs at low cascode voltage (~5V) increase significantly, even though now more constant with cascode.

The Output Stage Current Source

As it would become obvious later, we have to look at the output stage first before the current mirror.

Let's start off with the output stage current source. There are many ways to make a high power CCS, as explained in great detail by Walt Jung [13]. You can also find them back in [5, 6, 7]. And it appears that the complication in the EB602 may not be justified. But if one is to follow Borbely's design philosophy and stick to (lateral) FETs, then one would either have to accept some trimming to set up the correct bias current, or one would use a form of current sensing control loop.

This is precisely what is employed in the EB602. The gate bias voltage of the n-MOS (Q4) is set by the NPN (Q5) loaded by R11. The bias current is sensed by R13, which is then fed to the base of Q5. As soon as the base voltage exceeds 0.6V, Q5 is turned on, reducing the gate bias voltage to maintain the MOSFET current to that constant value, irrespective of any variations in Vgs of the n-MOS. Again, plug and play, no adjustments.

Q5 is designed to have a bias current of approximately 1mA, and a Vce of about < 2V. So its temperature is likely to remain stable at room temperature. In addition, the Vbe drift is about -2mV/°C. This works out to be about 0.3%/°C, which is sufficiently low for the purpose.

One can argue that a LED biased BJT CCS would achieve the same. Which would be the case if the LED is thermally coupled to the power NPN. No such requirement in the Borbely solution.

The Output Driver

When driven by a fixed drain resistor of the input stage LTP, the gate voltage of the p-MOS is pre-determined by the value of the resistor and the LTP bias. Any variations of Vgs between devices or with working temperature will therefore affect the bias current, which when loaded by a stabilised CCS discussed above will lead to output DC offset.

This is not the case when the LTP is loaded with a current source or a current mirror. In this case, the drain voltage of the LTP positive leg is essentially floating. The output CCS will then determine the bias of the driver p-MOS, and the Vgs of the p-MOS at bias, plus the voltage drop across its source resistor, will determine collector voltage of the current mirror Q2. Plug and play yet again.

The Current Mirror

In reference [8], John Broskie suggested a hybrid version where the current mirror is replaced by a single resistor. Apart from that the single resistor will affect bias current and hence DC offset of the output driver, there are certain things that make the current mirror advantageous :

1) The current mirror loaded LTP outputs a current which equals the difference of the signal current of both legs of the LTP. This means that even harmonic distortion of the LTP cancels out, if the two devices are well matched.

2) The current mirror has a much higher dynamic impedance than the single fixed resistor. This increases open loop gain significantly.

As Borbely mentioned in [8],
"….I tried to make a very simple circuit, which I think worked very well with the current mirror. I think this was the simplest way of generating enough current to drive the input cap of the MOSFET. I left the generation of the second harmonics to the SE common source second stage, which also worked well, :-)) I guess I prefer a controlled/acceptable amount of harmonics, even of the second harmonic variety. ….."

There are other current mirrors, using 2~4 transistors, with even better performance than the single BJT+Diode as used by Borbely. They do require matched devices to realise their full performance advantage. Nowadays, matched PNP duals such as the PMP5201 (matched to 2% hfe, 2mV Vbe) become available in a single chip at very reasonable costs. Again if one wish to go for bets performance, then 4x hfe-matched 2SA1312 will guarantee lower noise. This is perhaps the one single area where one might consider deviating from the original circuit. The use of a 4-transistor

Wilson Mirror not only reduces distortion noticeably, but also, as a by-product, the output DC offset due to balancing of base currents on both arms.

Overall performance

Load Dependence

As Nelson Pass has pointed out in [10], the performance of this topology is load dependent. This is because both the first and second stage are purely transconductance. The open-loop voltage gain is therefore dependent on the load impedance, which in turn determines the amount of negative feedback and also the output impedance. For example, the open loop gain with a 100R load is in the order of 80dB, whereas it drops to 70dB with a 30R load. Luckily, most low impedance headphones also require less voltage for the same SPL, and one can still take this load variation into account. That is also why Borbely suggested a low-voltage, high bias version for phones with low impedances.

Minimum Voltage Headroom for the Current Mirror

For the current mirror of the front-end to work properly, it has to have a minimum voltage drop. This is equal to the bias current x R3, plus some minimum Vce for Q2. In order that Q2 functions in its linear region, Vce should not be less than 1V. Adding another 1V drop across R3 at normal bias, the gate voltage of the p-MOS should be 2~3V below the top rail. Thus, knowing the Vgs of the p-MOS at output bias current (~1.6V), one has to make sure that the source resistor R10 is large enough to make up the required voltage deficit.

Current Clipping on Negative Swing

When a negative signal is applied, the output will want to swing negative, and will have to sink current from the load at the same time. Since the output stage is single ended and not push-pull, sinking current can only be attained by switching off the driver p-MOS. The maximum theoretical current sink is then that by the n-MOS CCS.

To switch off the p-MOS completely, the gate voltage applied to the p-MOS gate has to be less than its Threshold voltage from the top rail, and no current will flow through its source resistor. However, the highest possible output voltage of the current mirror (from Gnd) is limited by the required voltage drop of the current mirror. Especially in the 4-transistor Wilson mirror, this minimum voltage is > 0.8V even if we take out R3, 4 altogether, whereas the Threshold voltage of the p-MOS can be as low as 0.2V. Even in the original schematics, the p-MOS cannot be completely switched off, as there will be some current flowing through R3 via the BE junction of Q2 into the opposite of the LTP. In case of the original schematics, the maximum current sink is around 120mA, with a bias of 160mA for the n-MOS CCS, i.e. some 75%. To be able to make use of the CCS bias 100%, the only solution is to reduce R3, 4 to zero, and use the 2-transistor current mirror only.

Frequency Response

Because of the load dependence mentioned above, the closed loop frequency response is also load dependent. With 30R load, There is only a slight overshoot of 2dB at 4 MHz even without bandwidth limiting of C4, and the Zobel network of R14, C5. This overshoot however increases rapidly with load impedance, becoming +9dB with a 60R load, and +18dB above 100R. For the same amplifier to be able to work with a variety of headphones, those stability enhancing components cannot be saved. Even with bandwidth limiting, -3dB bandwidth is still over 1MHz at 30R load.