

DSP ADAU142+AD1938 Testing Report

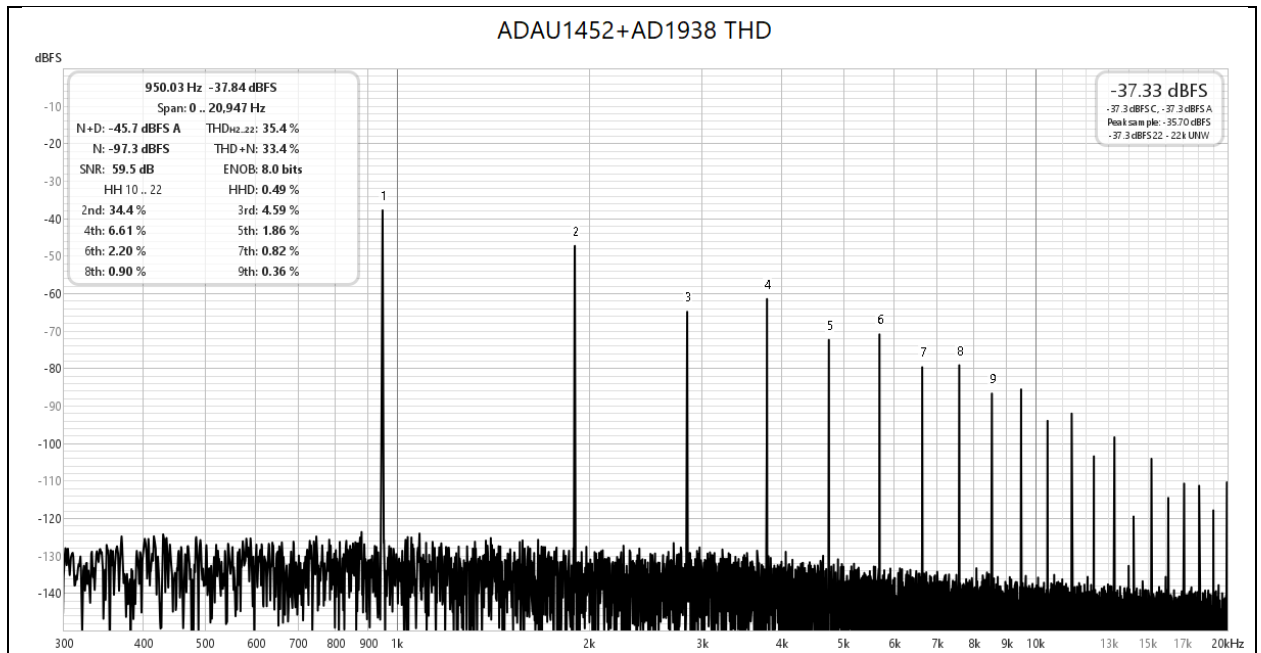


Fig. 1. 950Hz sine wave spectrum at the DSP output. DSP shows very high THD level reaching tens of percents. The sine wave was generated using SigmaStudio's built-in plugin (see. Fig. 7)



Fig. 2. Oscillogram at the DSP output which should be pure 950Hz sine wave. However, the waveform is very distorted because of high THD level. **Any DSP registry settings (Fig. 8 and 9), different sampling rates etc. didn't help to fix the problem. The same THD problem is inherent in the output of all 8 DSP channels.**

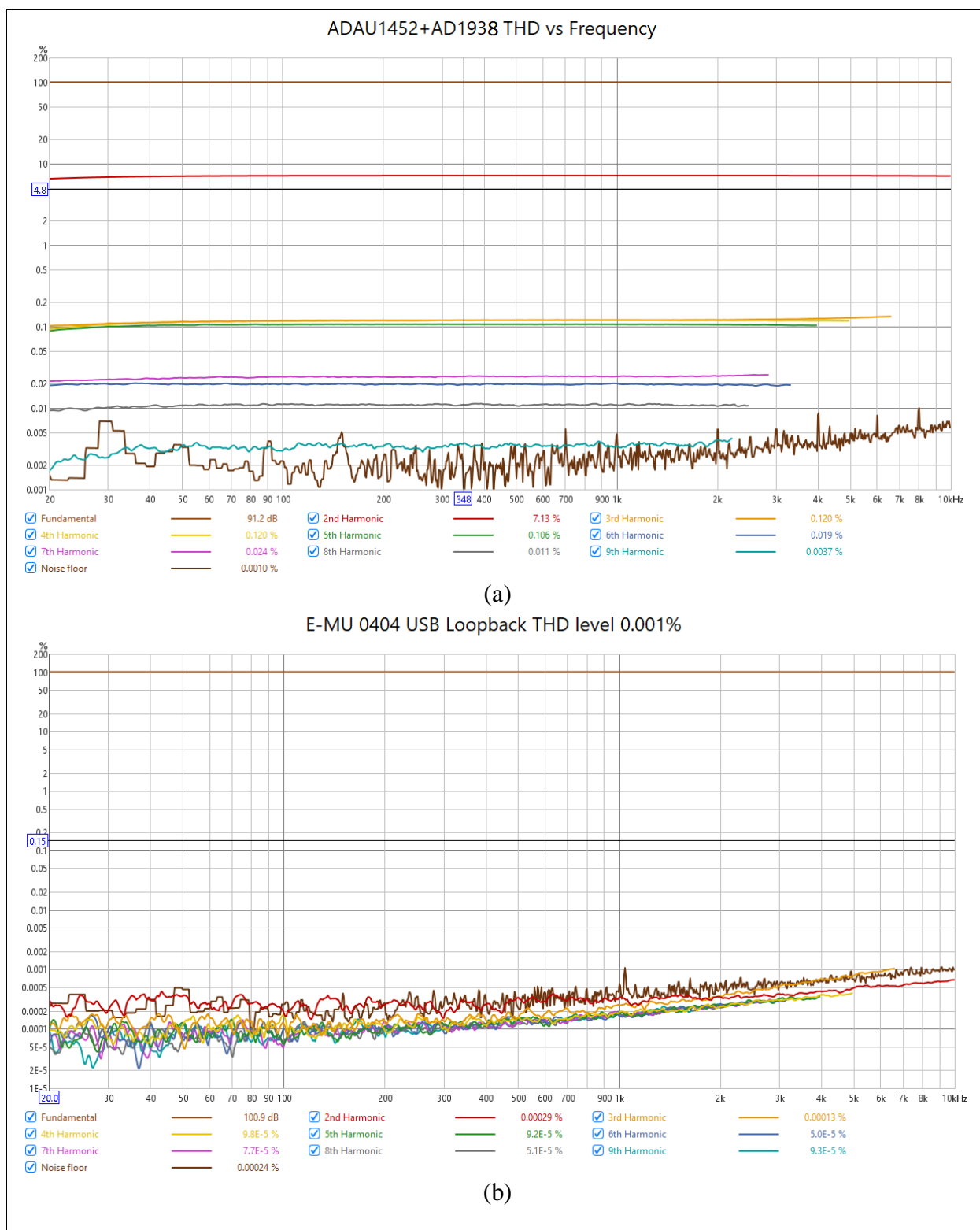


Fig. 3. THD vs Frequency at the DSP output (a) and loop-back THD of the testing bench (sound card E-MU 0404 USB + REW). THD level of the test bench is below 0.001%.

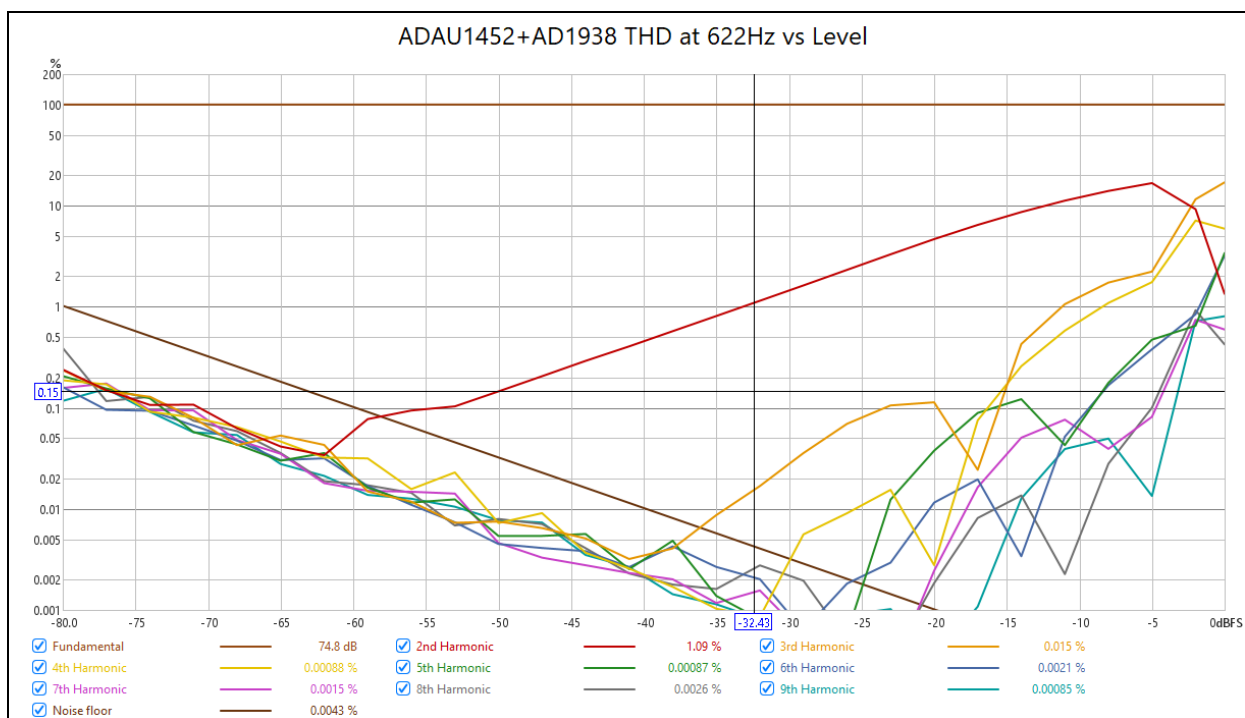


Fig. 4. THD vs input signal level. THD start rise from very low input signal levels (-62 dBFS), which indicates **the DSP operates incorrectly**.

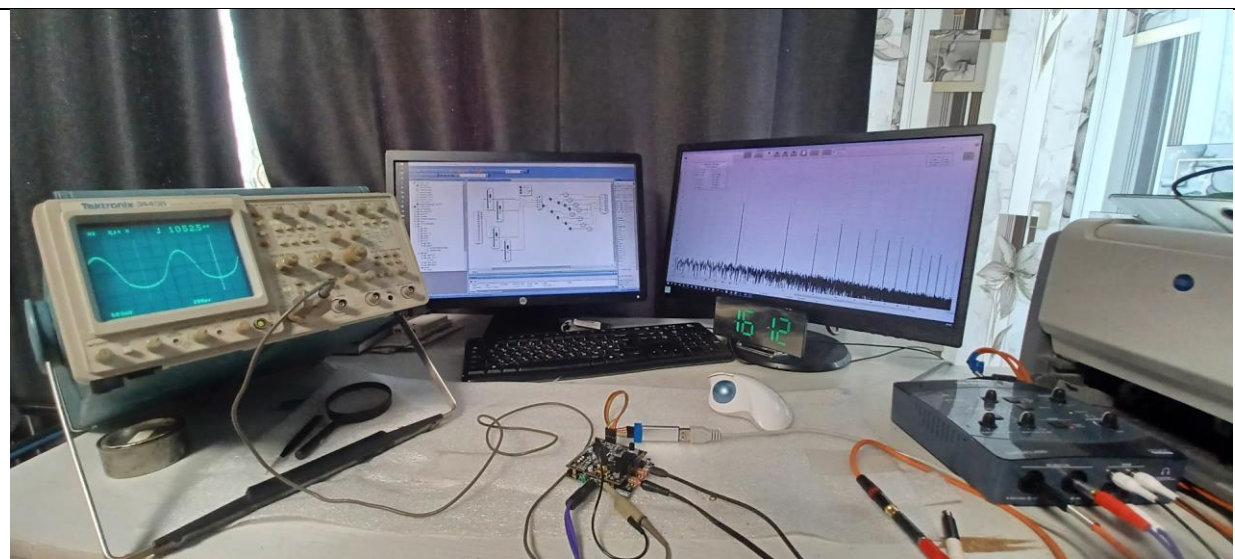


Fig. 5. The testing bench (Tektronix 2445B oscilloscope + Spectrum analyzer REW+EMU 0404 USB sound card).



Fig. 6. DSP ADAU1452 + AD1938 under test

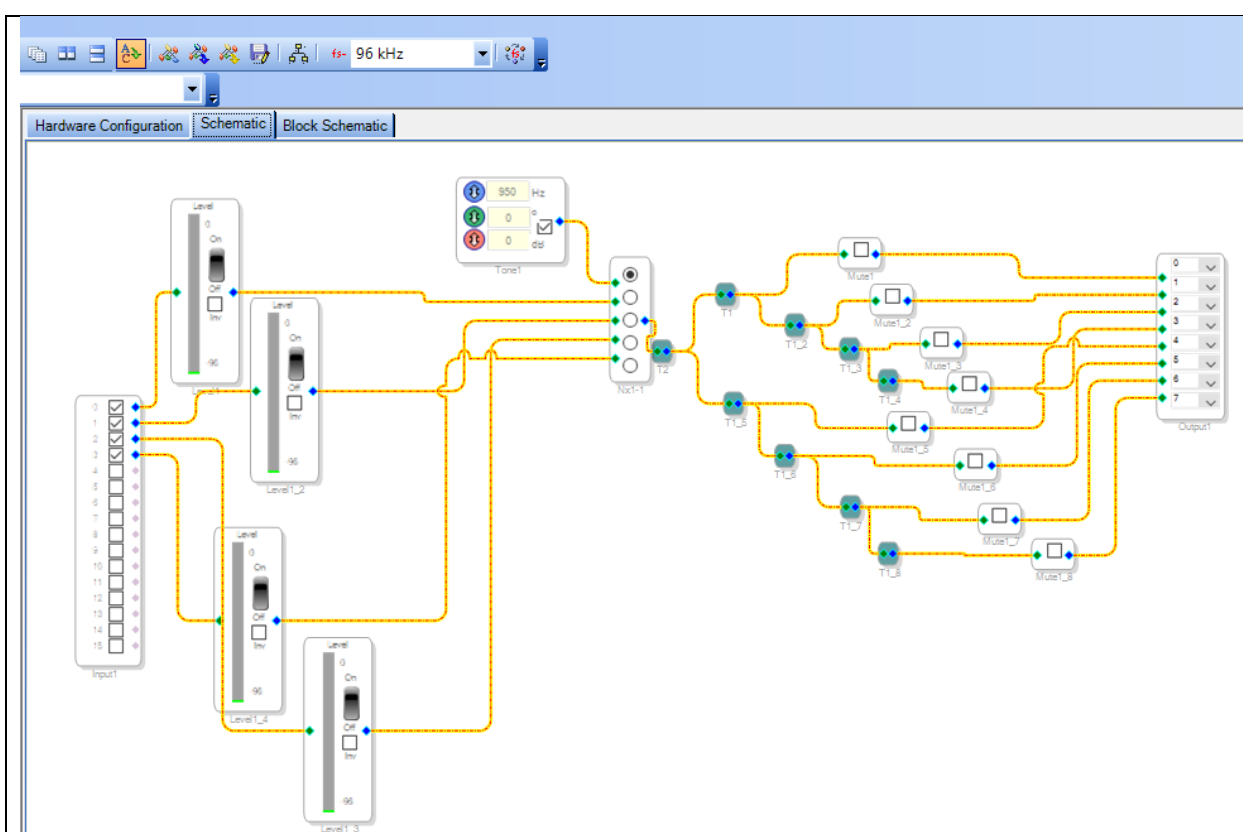


Fig. 7. Sigma Studio's diagram showing testing procedure of the DAC outputs.

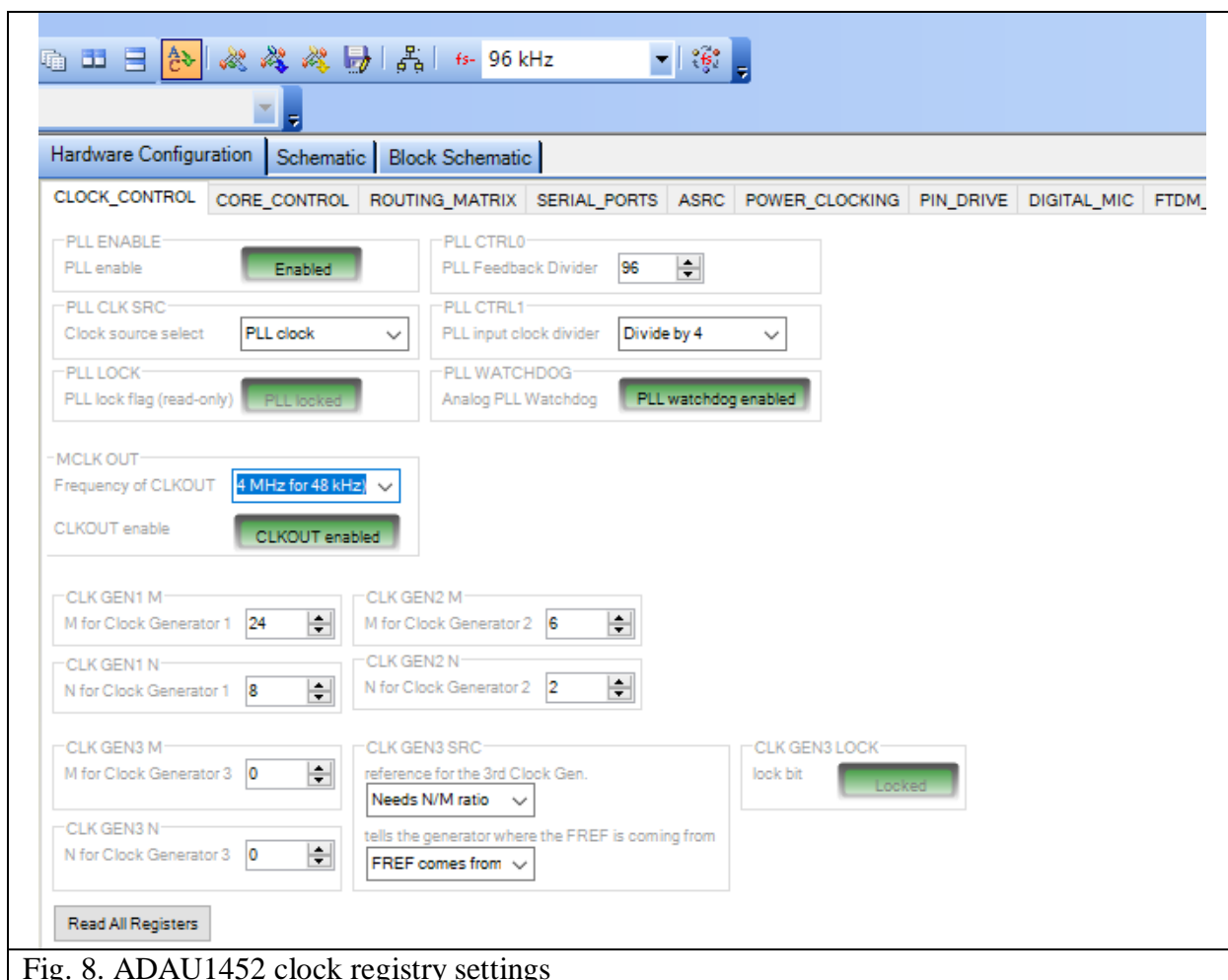


Fig. 8. ADAU1452 clock registry settings

Hardware Configuration | Schematic | Block Schematic

CLOCK_CONTROL | CORE_CONTROL | ROUTING_MATRIX | SERIAL_PORTS | ASRC | POWER_CLOCKING | PIN_DRIVE | DIGITAL_MIC | FTDM_IN | FTDM_OUT | MUL

SERIAL INPUT PORTS

SDATA_IN0				SDATA_IN1			
LRCLK Source	LRCLK is master	LRCLK type	50/50 duty cycle clock	LRCLK Source	LRCLK is master	LRCLK type	50/50 duty cycle clock
BCLK Source	BCLK is master	LRCLK Polarity	Positive polarity	BCLK Source	BCLK is master	LRCLK Polarity	Negative polarity
Word Length	32 bits	BCLK Polarity	Negative polarity	Word Length	24 bits	BCLK Polarity	Negative polarity
MSB Position	I2S - BCLK delay t	Clock Generator	Clock generator 1	MSB Position	I2S - BCLK delay t	Clock Generator	Clock generator 1
TDM Mode	4 channels, 32 bit	Sample Rate	Fs	TDM Mode	2 channels, 32 bit	Sampling Rate	Fs

SDATA_IN2				SDATA_IN3			
LRCLK Source	LRCLK is master	LRCLK type	50/50 duty cycle clock	LRCLK Source	LRCLK is master	LRCLK type	50/50 duty cycle clock
BCLK Source	BCLK is master	LRCLK Polarity	Negative polarity	BCLK Source	BCLK is master	LRCLK Polarity	Negative polarity
Word Length	24 bits	BCLK Polarity	Negative polarity	Word Length	24 bits	BCLK Polarity	Negative polarity
MSB Position	I2S - BCLK delay t	Clock Generator	Clock generator 1	MSB Position	I2S - BCLK delay t	Clock Generator	Clock generator 1
TDM Mode	2 channels, 32 bit	Sampling Rate	Fs	TDM Mode	2 channels, 32 bit	Sampling Rate	Fs

SERIAL OUTPUT PORTS

SDATA_OUT0				SDATA_OUT1			
LRCLK Source	LRCLK is master	LRCLK type	50/50 duty cycle clock	LRCLK Source	LRCLK is master	LRCLK type	50/50 duty cycle clock
BCLK Source	BCLK is master	LRCLK Polarity	Negative polarity	BCLK Source	BCLK is master	LRCLK Polarity	Negative polarity
Word Length	32 bits	BCLK Polarity	Negative polarity	Word Length	24 bits	BCLK Polarity	Negative polarity
MSB Position	I2S - BCLK delay t	Clock Generator	Clock generator 1	MSB Position	I2S - BCLK delay t	Clock Generator	Clock generator 1
TDM Mode	8 channels, 32 bit	Sampling Rate	Fs	TDM Mode	2 channels, 32 bit	Sampling Rate	Fs/2
Unused Output Channels	Drive every output channel			Unused Output Channels	Tristate unused output channels		

Fig. 9. ADAU1452 serial ports registry settings