

	Reg	Value	Binary	Name	Settings
1-2-3 open 48kHz TDM	00	BE	10111110	PLL0	PLL normal, Input 768, MCLK XO Off, PLL input DLRCLK, ADC and DAC active
	01	F8	11111000	PLL1	DAC source PLL, ADC source PLL, on-chip voltage off, PLL locked,
	02	40	01000000	DAC Cti0	Power on, 48kHz rate, SDATA delay=1, serial format=TDM
	03	0C	00001100	DAC Cti1	Latch in mid cycle, BCLK per frame=256 (8 channels), LRCLK left=high, LRCLK slave, BCLK=slave, BCLK source=DBCLK, BCLK polarity normal
	04	C0	11000000	DAC Cti2	Unmute, de-emphasis flat, 24 bit word width, output polarity noninverted
	05	00	00000000	DAC Ch Mute	All unmuted
	06	00	00000000	DAC L1 Vol	No attenuation
	07	00	00000000	DAC R1 Vol	No attenuation
	08	00	00000000	DAC L2 Vol	No attenuation
	09	00	00000000	DAC R2 Vol	No attenuation
	0A	00	00000000	DAC L3 Vol	No attenuation
	0B	00	00000000	DAC R3 Vol	No attenuation
	0C	00	00000000	DAC L4 Vol	No attenuation
	0D	00	00000000	DAC R4 Vol	No attenuation
	0E	00	00000000	ADC Cti0	Power on, high pass off, all unmuted, output rate 48kHz
	0F	A0	10100000	ADC Cti1	24 bit word width, SDATA delay=1, serial format=TDM, BCLK latch in mid cycle
	10	26	00100110	ADC Cti2	LRCLK=50/50, BCLK out on rising edge, LRCLK left=high, LRCLK slave, 256 BCLK per frame, BCLK slave, BCLK source=ABCLK
1-2-3 close 48kHz I2S	00	BE	10111110	PLL0	PLL normal, Input 768, MCLK XO Off, PLL input DLRCLK, ADC and DAC active
	01	F8	11111000	PLL1	DAC source PLL, ADC source PLL, on-chip voltage off, PLL locked,
	02	02	00000010	DAC Cti0	Power on, 96kHz rate, SDATA delay=1, serial format=stereo
	03	8D	10001101	DAC Cti1	Latch at end of cycle, BCLK per frame=256 (8 channels), LRCLK left=high, LRCLK slave, BCLK=slave, BCLK source=DBCLK, BCLK polarity inverted
	04	E0	11100000	DAC Cti2	Unmute, de-emphasis flat, 24 bit word width, output polarity noninverted
	05	00	00000000	DAC Ch Mute	All unmuted
	06	00	00000000	DAC L1 Vol	No attenuation
	07	00	00000000	DAC R1 Vol	No attenuation
	08	00	00000000	DAC L2 Vol	No attenuation
	09	00	00000000	DAC R2 Vol	No attenuation
	0A	00	00000000	DAC L3 Vol	No attenuation
	0B	00	00000000	DAC R3 Vol	No attenuation
	0C	00	00000000	DAC L4 Vol	No attenuation
	0D	00	00000000	DAC R4 Vol	No attenuation
	0E	40	01000000	ADC Cti0	Power on, high pass off, all unmuted, output rate 96kHz
	0F	80	10000000	ADC Cti1	24 bit word width, SDATA delay=1, serial format=stereo, BCLK latch in mid cycle
	10	26	00100110	ADC Cti2	LRCLK=50/50, BCLK out on rising edge, LRCLK left=high, LRCLK slave, 256 BCLK per frame, BCLK slave, BCLK source=ABCLK
1-3 close 96kHz I2S	00	BE	10111110	PLL0	PLL normal, Input 768, MCLK XO Off, PLL input DLRCLK, ADC and DAC active
	01	F8	11111000	PLL1	DAC source PLL, ADC source PLL, on-chip voltage off, PLL locked,
	02	42	01000010	DAC Cti0	Power on, 96kHz rate, SDATA delay=1, serial format=TDM
	03	06	00000110	DAC Cti1	Latch in mid cycle, BCLK per frame=512 (16 channels), LRCLK left=low, LRCLK slave, BCLK=slave, BCLK source=DBCLK, BCLK polarity normal
	04	C0	11000000	DAC Cti2	Unmute, de-emphasis flat, 24 bit word width, output polarity noninverted
	05	00	00000000	DAC Ch Mute	All unmuted
	06	00	00000000	DAC L1 Vol	No attenuation
	07	00	00000000	DAC R1 Vol	No attenuation
	08	00	00000000	DAC L2 Vol	No attenuation
	09	00	00000000	DAC R2 Vol	No attenuation
	0A	00	00000000	DAC L3 Vol	No attenuation
	0B	00	00000000	DAC R3 Vol	No attenuation
	0C	00	00000000	DAC L4 Vol	No attenuation
	0D	00	00000000	DAC R4 Vol	No attenuation
	0E	40	01000000	ADC Cti0	Power on, high pass off, all unmuted, output rate 96kHz
	0F	A0	10100000	ADC Cti1	24 bit word width, SDATA delay=1, serial format=TDM, BCLK latch in mid cycle
	10	34	00110100	ADC Cti2	LRCLK=50/50, BCLK out on falling edge, LRCLK left=high, LRCLK slave, 512 BCLK per frame, BCLK slave, BCLK source=ABCLK
2-3 close 192kHz I2S 96kHz TDM 192kHz I2S	00	BE	10111110	PLL0	PLL normal, Input 768, MCLK XO Off, PLL input DLRCLK, ADC and DAC active
	01	F8	11111000	PLL1	DAC source PLL, ADC source PLL, on-chip voltage off, PLL locked,
	02	44	01000100	DAC Cti0	Power on, 192kHz rate, SDATA delay=1, serial format=TDM
	03	0E	00001110	DAC Cti1	Latch in mid cycle, BCLK per frame=512 (16 channels), LRCLK left=high, LRCLK slave, BCLK=slave, BCLK source=DBCLK, BCLK polarity normal
	04	C0	11000000	DAC Cti2	Unmute, de-emphasis flat, 24 bit word width, output polarity noninverted
	05	00	00000000	DAC Ch Mute	All unmuted
	06	00	00000000	DAC L1 Vol	No attenuation
	07	00	00000000	DAC R1 Vol	No attenuation
	08	00	00000000	DAC L2 Vol	No attenuation
	09	00	00000000	DAC R2 Vol	No attenuation
	0A	00	00000000	DAC L3 Vol	No attenuation
	0B	00	00000000	DAC R3 Vol	No attenuation
	0C	00	00000000	DAC L4 Vol	No attenuation
	0D	00	00000000	DAC R4 Vol	No attenuation
	0E	80	10000000	ADC Cti0	Power on, high pass off, all unmuted, output rate 192kHz
	0F	A0	10100000	ADC Cti1	24 bit word width, SDATA delay=1, serial format=TDM, BCLK latch in mid cycle
	10	36	00110110	ADC Cti2	LRCLK=50/50, BCLK out on rising edge, LRCLK left=high, LRCLK slave, 512 BCLK per frame, BCLK slave, BCLK source=ABCLK