Distortion Correction Circuits for Audio Amplifiers*

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Circuit topologies are introduced which should prove of use to the circuit designer of analog audio amplifiers. The objective is to produce circuits of modest complexity that overcome the nonlinearities inherent in single-transistor and long-tail pair circuits. This allows amplifiers with excellent linearity to be designed without resorting to overall negative feedback with high loop gains. To aid comparison of circuit nonlinear behavior, a parameter called the incremental distortion factor (IDF) is introduced and discussed.

0 INTRODUCTION

Most modern transistor amplifiers use either a single transistor or a pair of transistors in the input circuitry. It is argued that if this stage is cascaded with adequate gain, then by the expedience of overall negative feedback, the input devices will operate within the limits for small-signal operation and thus yield good overall linearity.

Often a consequence of this design philosophy is poor dynamic performance of the input circuitry, where modest input overload can result in gross distortion. There are simple circuit modifications that can be introduced: an increase in device operating current, though possibly at the expense of the noise factor; the introduction of local negative feedback (emitter degeneration) which reduces stage gain but enhances linearity and overload performance, again at the expense of the noise factor.

The aim of this paper is to introduce circuit topologies that enhance the nonlinear performance of amplifier gain cells without recourse to high overall negative feedback. It is considered by this author that the combination of high loop gain together with its inevitable dynamic performance (dominant pole) when compounded with nonlinear elements can result in poor transient distortion characteristics, especially when complex signals are being processed. Since the signals being amplified are rendered more complex due to these nonlinearities falling within a dynamic negative feedback loop, then intermodulation products result which are effectively time smeared. In the limit this must determine the ultimate resolution of an amplifier, which is its ability to transfer fine signal detail in the presence of complex signals.

The only rational methodology to minimize these attributes of nonlinear distortion is to use gain cells that are inherently linear over a wide range of their transfer characteristics and are essentially nondynamic with predictable gain characteristics. Such gain cells can then be used with amplifiers with overall negative feedback without detriment to the intermodulation performance. However, the use of linear circuitry may well render the need for high negative feedback unnecessary.

This paper investigates and catalogs examples of gain cells that generally exhibit good linearity and dynamic range. The circuits should prove of use to designers of both discrete and integrated circuitry, although some design examples which are particularly relevant to integrated-circuit fabrication are included.

In order to facilitate the comparison of various circuit topologies, a parameter called incremental distortion factor (IDF) is introduced. The IDF is related to the change in slope of the transfer characteristic with the input signal and is useful for quantifying nonlinearity under large-signal conditions.

1 PRINCIPLES OF DISTORTION CORRECTION

Three methods are identified in this section to enhance the linearity of gain cells that may already use either local or overall negative feedback within an amplifier structure. (See [1–5] for background.)

1.1 Complementary Nonlinear Stages in Cascade

If a stage has a predictable nonlinearity, then by using a nonlinear stage with a complementary transfer characteristic, overall linearity is possible (Fig. 1). This technique is, for example, used in translinear multiplier stages and in a modified form is the principle of complementary compandors.

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1.2 Device Linearization

This method involves matching device nonlinearities as with the long-tailed pair, where the transconductance is linearized approximately by keeping r_{ep} constant over a wider range of emitter current compared with a single transistor r_e over the same current range. Thus for single transistors,

$$r_{e1} = \frac{\partial V_{be1}}{\partial I_{e1}} \tag{1}$$

$$r_{e2} = \frac{\partial V_{be2}}{\partial I_{e2}} \tag{2}$$

and for a long-tail pair of transistors,

$$r_{ep} = \frac{\partial V_{be1}}{\partial I_{e1}} + \frac{\partial V_{be2}}{\partial I_{e2}} \tag{3}$$

Comparing r_{ep} with r_{e1} or r_{e2} for a given change in emitter current, r_{ep} exhibits greater linearity.

1.3 Error Feedforward and Feedback Distortion Correction

A technique [6] that was recently reported for linearizing near unity gain output stages in analog power amplifiers uses in general a combination of error feedforward and error feedback. Fig. 2 illustrates the method in schematic form.

Analysis shows that when

$$b = (1 - a) \tag{4}$$

then

$$S_{out} = S_{in} \tag{5}$$

where a and b are constrained to values between 0 and 1.

If $a = 1$ and $b = 0$, the system becomes pure error feedback, while if $a = 0$ and $b = 1$, pure feedforward error correction results.

When the balance equation (4) is satisfied, the effects of nonlinearity in the general network N are minimized, and the output parameters S_{out} and S_{in} become linearly related. Though it is inferred that these parameters are voltages, in general they may be any suitable combination of current and voltage, such as voltage in, current out, which is of particular importance for the input stage of an audio amplifier.

Although this principle can be applied to an overall amplifier, it is recommended that the technique be restricted to single stages (which in turn can be compounded to form a complete amplifier), as this permits near nondynamic stage performance and minimizes signal distortion that can be generated in cascaded high gain, low local-feedback amplifier stages.

In practical amplifier design it is possible to compound the techniques outlined in this section to produce amplifier stages of high linearity. It is also possible, within limits, to trade off circuit complexity against performance and to choose a technique that is best suited to a particular amplifier application. In the following sections, circuit examples will be discussed to indicate how predictable amplifiers can be designed and that by the careful choice of design techniques enhanced performance results.

2 INCREMENTAL DISTORTION FACTOR (IDF)

The prime nonlinearity of a transistor which is operated with near constant collector–base voltage is defined by the exponential relationship

$$I_e = I_0 \exp\left(\frac{qV_{be}}{KT}\right) \tag{6}$$

where

I_e = emitter current
I_0 = base-emitter diode saturation current
K = Boltzman's constant
q = charge on electron
T = junction temperature (degrees Kelvin)

Some deviation from this relationship will occur, but is of little consequence here.

Thus when a transistor is used as a transconductance amplifier, nonlinear distortion will result. In order to attempt to quantify the nonlinearity, we introduce the term *incremental distortion factor* (IDF). In essence this term is a measure of the change in incremental gain of a stage to the small-signal gain. In practical circuits the IDF can most simply be expressed as a function of one or more variables. Hence by observing the variation of IDF with these parameters, an accurate measure of nonlinear performance can be made.

To explain the IDF in more detail, we proceed by analyzing first the nonlinear behavior of a simple single-transistor stage with local emitter degeneration and second the performance of a two-transistor long-tail pair. These results are also of use as a reference to allow comparison with the more elaborate gain cell topologies presented in later sections.

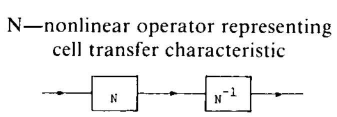

Fig. 1. Complementary linearization.

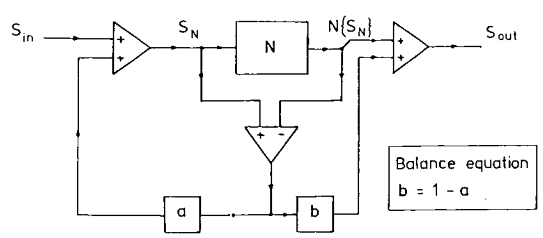

Fig. 2. Error feedforward and feedback distortion correction.

2.1 Distortion Characteristics of a Single-Transistor Cell

A single-transistor cell is shown in Fig. 3. We assume the base current to be negligible. Hence from Eq. (6),

$$V_{be} = \frac{KT}{q} \ln \left(\frac{I_e}{I_0}\right) . \tag{7}$$

Let $\alpha = KT/q$. Therefore

$$V_{be} = \alpha \ln \left[\frac{I_e}{I_0}\right] . \tag{8}$$

Applying Kirchhoff's law to the circuit shown in Fig. 3 and eliminating V_{be} [using Eq. (8)],

$$V_{in} = (i - I_x) R + \alpha \ln \left(\frac{I + i}{I_0}\right) \tag{9}$$

(bias currents I_x, I are shown in Fig. 3). In this simple example V_{in} is a function of a single variable i, that is,

$$V_{in} = f(i).$$

By differentiation we obtain

$$\mathrm{d}V_{in} = \left(\frac{\mathrm{d}V_{in}}{\mathrm{d}i}\right) \mathrm{d}i$$

therefore

$$\mathrm{d}V_{in} = R\,\mathrm{d}i + \frac{\alpha}{I + i}\,\mathrm{d}i.$$

Extracting linear and nonlinear components,

$$\underbrace{\mathrm{d}V_{in}}_{I/P \text{ voltage}} = \underbrace{\left(R + \frac{\alpha}{I}\right)\mathrm{d}i}_{\text{linear component}} - \underbrace{\left\{\frac{\alpha i}{I(I + i)}\right\}\mathrm{d}i}_{\text{nonlinear component}} . \tag{10}$$

Eq. (10) relates incremental changes in current and voltage expressed as a function of the bias current I and the present state of signal current i. It is essentially the tangent to the transfer characteristic for transconductance. For linearity, $\mathrm{d}V_{in}$ and $\mathrm{d}i$ must be related by a constant multiplier. However, Eq. (10) reveals that the incremental gain is a function of i, which represents a nonlinear process. We define the IDF $N(\ldots)$ as

$$N(x) = \left[\frac{\text{nonlinear incremental gain component}}{\text{linear incremental gain component}}\right] . \tag{11}$$

$N(\ldots)$ is shown here to be a function of a single variable x. However, in later sections the definition is extended to functions of several variables.

Defining x, the transistor loading factor, as the ratio of signal current i to bias current I for the single-stage transistor amplifier,

$$x = \frac{i}{I} . \tag{12}$$

Hence from Eqs. (10)–(12) we obtain

$$N(x) = \frac{-x}{1 + x} \left(\frac{\alpha}{\alpha + IR}\right) . \tag{13}$$

Eq. (13) reveals that the IDF is an asymmetric function of x, as would be anticipated for a single-transistor nonlinearity. The advantage of this format is that since x is a direct measure of the signal loading of a transistor, then if large values of x result in low values of IDF, this is an expression of near linear performance. In practice x can range from -1 to $+1$, though usually (except under overload) x will remain well within these limits.

The main advantage of the IDF is that it permits a comparison of circuits with respect to their nonlinear performance, even when complex multiple distorting mechanisms coexist.

2.2 Distortion Characteristic of the Long-Tail Pair Cell

A treatment similar to that presented in Section 2.1 is applied here to the long-tail pair circuit shown in Fig. 4. From Kirchhoff's law,

$$V_{in} = iR + (V_{be1} - V_{be2}) .$$

Applying Eq. (8) to each transistor,

$$V_{in} = iR + \alpha \ln \left[\frac{I + i}{I - i}\right] . \tag{14}$$

Differentiating and extracting linear and nonlinear components,

$$\mathrm{d}V_{in} = \left(R + \frac{2\alpha}{I}\right) \mathrm{d}i + \left\{\frac{2\alpha i^2}{I(I^2 - i^2)}\right\} \mathrm{d}i. \tag{15}$$

We obtain the IDF using the definition of Eq. (11):

$$N(x) = \frac{x^2}{(1 - x^2)} \left(\frac{2\alpha}{2\alpha + IR}\right) . \tag{16}$$

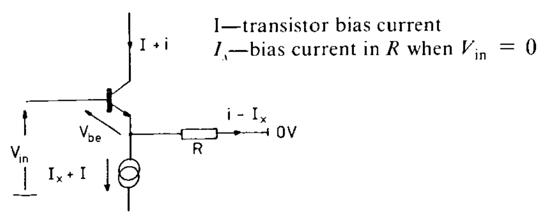

Fig. 3. Single-transistor cell.

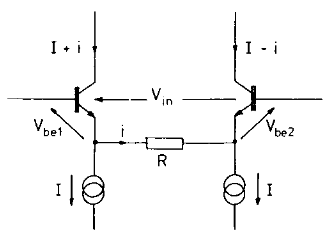

Fig. 4. Long-tail pair circuit.

Comparing Eq. (16) with Eq. (13), the differences in nonlinearity can be compared directly as a function of the transistor loading parameter x. These equations also form a reference for the circuits presented in the following sections.

3 GAIN CELL LINEARIZATION USING FEEDFORWARD ERROR CORRECTION

This section presents a series of circuit topologies that exploit error correction feedforward as outlined in Section 1. Where appropriate, the IDF is evaluated as a means of circuit comparison. All the circuits shown use bipolar transistors, though in most cases adaptation to FET devices should be feasible.

3.1 Single-Stage Feedforward Error Correction

The technique exploited in the circuit of Fig. 5 was derived from Fig. 2, where $a = 0$ and $b = 1$. Essentially when an input signal V_{in} is applied to the base of the input transistor, the resistor R_1 is used as a reference for converting V_{in} to a current. However, due to V_{be1} the voltage across R_1 is less than the input voltage. Hence by using a differential amplifier to measure the error voltage V_{be1}, a corrective current i_2 can be summed with i_1 to compensate almost exactly for the lost current. The transconductance is then almost independent of V_{be1}. Since $V_{be1} < V_{in}$, good linearity results. The main advantage of this circuit is that linearity can be achieved with only modest values of R_1, a fact that increases the transconductance of the cell, yet minimizes Johnson noise due to R_1.

The simplest method of adding the main current i_1 with the error correction current i_2 is to parallel the two collectors. However, if both collector currents of each half of the difference amplifier are used by introducing a current mirror, then either the value of R_2 can be increased, which improves linearity, or the value of R_1 can be reduced, which reduces Johnson noise and increases transconductance.

An example of a more practical amplifier is illustrated in Fig. 6, where biasing requirements and current mirror are shown.

We assume that the output signal current i_0 is derived as

$$i_0 = i_1 + \lambda i_2 \tag{17}$$

where generally λ has a value of 1 or 2 (Fig. 6 assumes $\lambda = 2$). The circuit equations are as follows:

$$V_{in} = (i_1 - I_x)R_1 + V_{be1} \tag{18}$$

$$V_{be1} = (i_2 + I_y)R_2 + (V_{be2} - V_{be3}) \tag{19}$$

$$V_{be1} = \alpha \ln\left[\frac{I_1 + i_1}{I_0}\right] \tag{20}$$

I_x, I_y—bias currents in R_1 and R_2 when $V_{in} = 0$

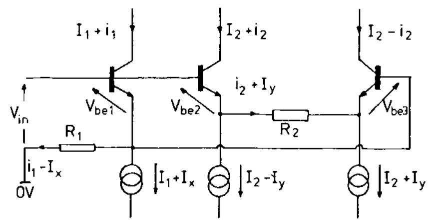

Fig. 5. Single-stage input device with feedforward error correction.

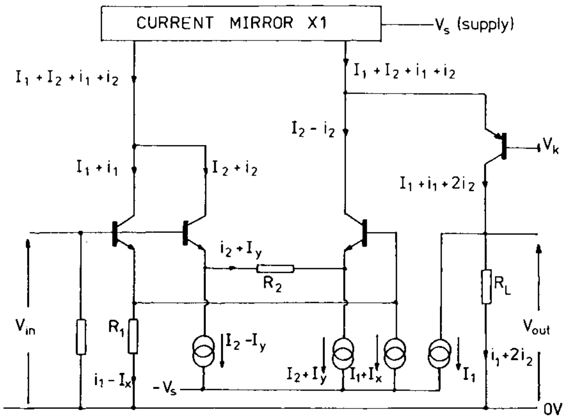

Fig. 6. Practical amplifier stage using a single input transistor with feedforward error correction.

$$V_{be2} - V_{be3} = \alpha \ln\left[\frac{I_2 + i_2}{I_2 - i_2}\right] . \tag{21}$$

Thus

$$V_{in} = (i_1 - I_x)R_1 + (i_2 + I_y)R_2 + \alpha \ln\left[\frac{I_2 + i_2}{I_2 - i_2}\right] .$$

Since

$$V_{in} = f(i_1, i_2)$$

then

$$dV_{in} = \frac{\partial V_{in}}{\partial i_1} di_1 + \frac{\partial V_{in}}{\partial i_2} di_2.$$

Therefore

$$dV_{in} = R_1 \left[di_1 + \left(\frac{I_2R_2 + 2\alpha}{R_1I_2}\right) di_2 \right] + \frac{2\alpha}{I_2}\left[\frac{i_2^2}{I_2^2 - i_2^2}\right] di_2.$$

By comparison with Eq. (17),

$$\lambda = \frac{I_2R_2 + 2\alpha}{I_2R_1} . \tag{22}$$

Expressing di_2 as a function of di_0, we then obtain the IDF

$$N(x, y) = \frac{2\alpha^2 y^2}{\lambda I_1 I_2 R_1^2[(1 - x)(1 - y^2 R_2/\lambda R_1) + (2\alpha/R_1 I_1)(1 - y^2)]} \tag{23}$$

where

$$x = \frac{i_1}{I_1} \quad \text{and} \quad y = \frac{i_2}{I_2} .$$

Since $|y| < |x|$ and $|x| < 1$, then Eq. (23) indicates that a substantial reduction in nonlinearity is possible.

3.2 Symmetrical Long-Tail Pair with Feedforward Error Correction

The primary distortion mechanism of a single transistor is the I_e/V_{be} relationship. If a long-tail pair is chosen, then the primary distortion is reduced, as discussed in Section 2.2, where it was also shown that the nonlinearity is symmetrical about the operating point.

This section investigates the use of feedforward error correction applied to a single long-tail pair. The IDF is stated in Eq. (24), the analysis being similar to that of Section 3.1:

$$N(x, y) = \frac{4\alpha^2 y^2}{\lambda I_1 I_2 R_1{}^2[(1 - x^2)(1 - y^2 R_2/\lambda R_1) + (2\alpha/I_1 R_1)(1 - y^2)]} \tag{24}$$

where λ, x, y, and i_0 are as defined in Section 3.1. The circuit is given in Fig. 7.

Eq. (24) reveals that the IDF is of a lower order due to the square-law dependence on x and that the nonlinearity is symmetrical about the quiescent operating point.

This particular configuration is applicable to amplifier input stages where offset cancellation of base–emitter junctions is useful in establishing dc biasing of the complete amplifier. Note, however, that there is no requirement for accurate device matching within either the long-tail pair or the error amplifier to achieve useful linearization. (Matching is necessary for accurate dc conditions, but this is a separate problem and may not be of importance in ac-coupled stages.)

3.3 Cascaded Gain Cells to Derive Differential Output Currents

A circuit application may require a differential output current from the gain cell. Since this feature is absent from the circuits presented in Figs. 5, 6 and 7, we consider here modifications that result in differential output currents.

The principle is illustrated in the basic schematic shown in Fig. 8, where identical gain cells are compounded within a cascade topology. This technique results in a fully complementary cell with enhanced IDF due to a reduction in primary distortion by sharing the input signal between cells.

Two circuits are presented in Figs. 9 and 10, which are formed by cascading the respective circuits of Figs. 5 and 7.

3.4 Nested Feedforward Error Correction Amplifier

To conclude this section on feedforward error correction, it should be noted that the error amplifier can be nested to yield even further distortion reduction, where effectively an error amplifier is used to compensate for the main error amplifier. However, in such circuits it is likely that other sources of distortion (other than the V_{be}/I_e nonlinearity) will then be dominant. Also, such circuits become somewhat complex, and the overall improvements are likely to be small. In fact for a given total current consumption in a gain cell, increasing the error amplifier current I_2 will produce a useful reduction in distortion, since the error amplifier loading factor is reduced as a function of y^2. Further enhancement can be obtained by using the modified amplifier cells to be presented in Section 5, in particular the cell shown in Figs. 15 and 16.

4 GAIN CELL LINEARIZATION USING FEEDBACK ERROR CORRECTION

Circuit topologies similar to that of Section 3 can be designed which rely upon the error signal being fed back to the gain cell input. This corresponds to the system

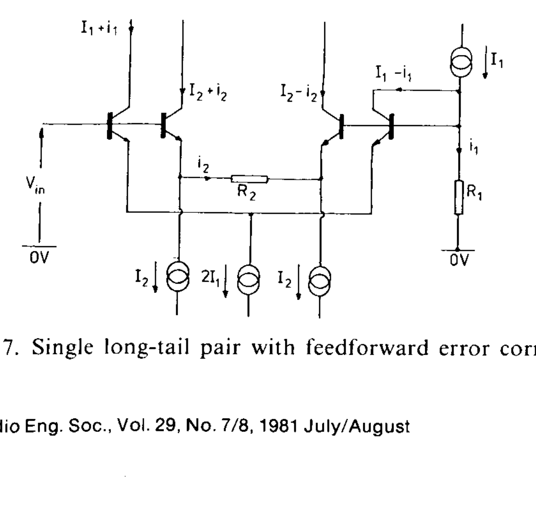

Fig. 7. Single long-tail pair with feedforward error correction.

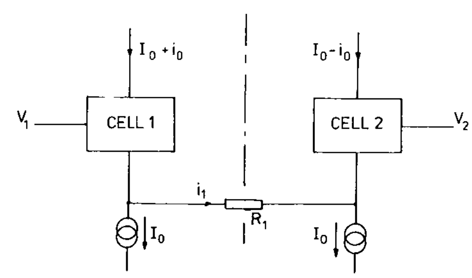

Fig. 8. Basic cascade of two identical gain cells.

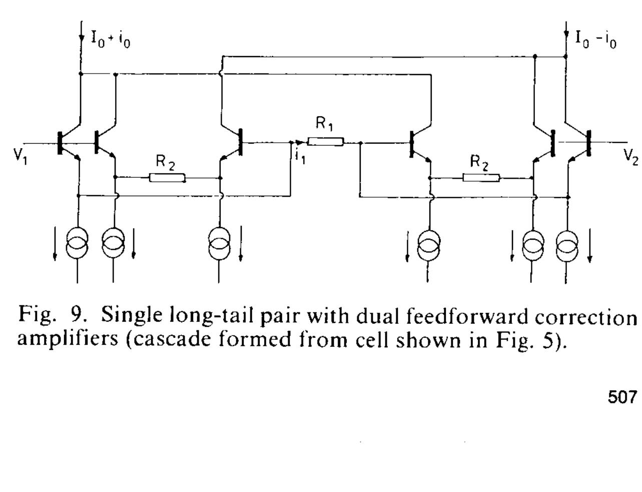

Fig. 9. Single long-tail pair with dual feedforward correction amplifiers (cascade formed from cell shown in Fig. 5).

diagram of Fig. 2, where $a = 1$ and $b = 0$. In these circuits the error signal is generally a current.

Figs. 11 and 12 show two examples which can be compared directly with the feedforward versions illustrated in Figs. 5 and 7.

Compound circuits similar to those described in Section 3.3 also can be derived by cascading gain cells with error correction feedback. These should be proven useful where differential output currents are required in fully symmetrical circuits (see Fig. 8).

The circuit equations are as follows. For the input transistor (Fig. 11),

$$V_{in} = V_{be} + (i_1 - i_2 + I_y)R_1$$

$$V_{be} = \alpha \ln\left[\frac{I_1 + i_1}{I_0}\right]$$

and for the error amplifier,

$$V_{be} = (I_x + i_2)R_2 + \alpha \ln\left[\frac{I_2 + i_2}{I_2 - i_2}\right] .$$

Let

$$R_2 = \frac{R_1 I_2 - 2\alpha}{I_2} . \tag{25}$$

Differentiating V_{in},

$$\mathrm{d}V_{in} = R_1\,\mathrm{d}i_1 - \left[\frac{2\alpha^2 i_2^2 \mathrm{d}i_1}{I_1 I_2^3 R_1(1 + i_1/I_1)(1 - i_2^2 R_2/I_2^2 R_1)}\right] . \tag{26}$$

Therefore

$$N(x, y) = \frac{-2\alpha^2 y^2}{I_1 I_2 R_1^2(1 + x)(1 - y^2 R_2/R_1)} . \tag{27}$$

Again the loading parameters x and y are defined as in Section 3.

It is interesting to note that Eq. (25) represents a balance equation which minimizes the output current i_1 dependence on i_2 and allows R_1^{-1} to determine the transconductance exactly.

A similar analysis for the circuit in Fig. 12 gives the IDF as

$$N(x, y) = \frac{-4\alpha^2 y^2}{I_1 I_2 R_1^2(1 - x^2)(1 - y^2 R_2/R_1)} , \tag{28}$$

where the balance is again determined by Eq. (25).

These results show that the feedback circuits give virtually the same performance as their feedforward counterparts, and for practical circuits the performance should be essentially identical.

5 INDIRECT DISTORTION CANCELLATION TOPOLOGIES

A significant improvement over the standard long-tail pair can be realized by using matched transistors. In these circuits it is assumed that the I_e/V_{be} characteristics are essentially identical. As examples Figs. 13 and 14 show indirect error correction.

In Figs. 13 and 14 transistors T_1, T_3, and T_2, T_4 are matched, and since they carry the same emitter current (excluding the small base current), the base–emitter voltages are identical. Thus an error-sensing difference am-

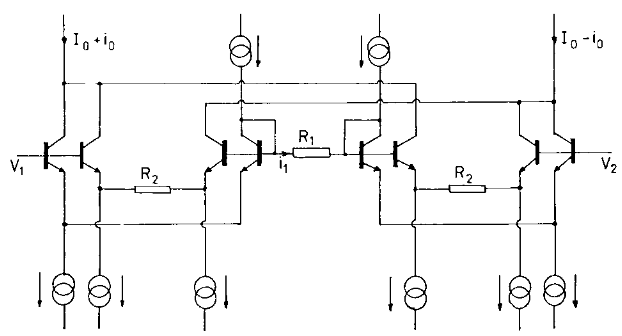

Fig. 10. Dual long-tail pair circuits with dual feedforward correction amplifiers (cascade formed from cell shown in Fig. 7).

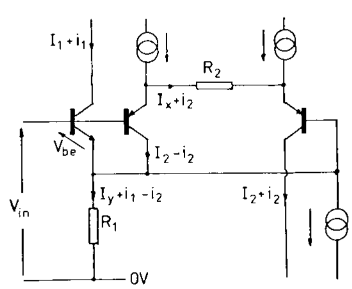

Fig. 11. Single input transistor with error correction feedback.

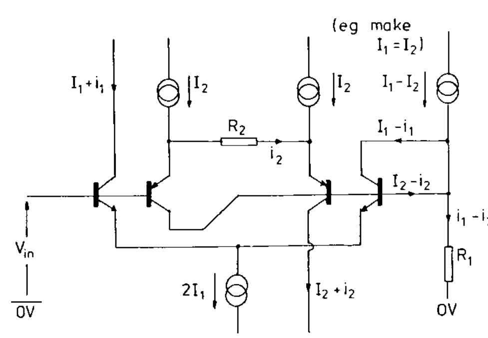

Fig. 12. Long-tail pair with error correction feedback.

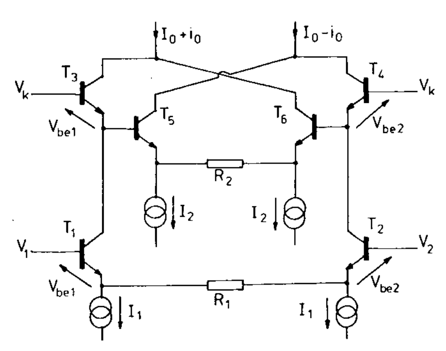

Fig. 13. Indirect error feedforward.

plifier can measure the error voltage ($V_{be1} - V_{be2}$) indirectly and compensate either by feedforward or by feedback.

The advantages of these circuits are that only a single error amplifier need be used, and transistors T_3, T_4 form a cascode configuration, which enhances bandwidth and linearity.

The IDFs for the error feedforward and error feedback circuits should compare with the circuits of Fig. 7 [Eq. (24)] and Fig. 12 [Eq. (28)], respectively, provided that there is accurate transistor matching, and base currents are neglected (i.e., high β transistors).

Finally a circuit is presented in Fig. 15 which combines the advantages of error feedforward with indirect error sensing to minimize nonlinearities.

We assume that all transistors are matched in terms of I_c/V_{be} nonlinearity and collector–base current gain β. The values of currents and voltages are shown in Fig. 15.

$$V_{in} = (V_1 - V_2) = (V_{be1} - V_{be2}) + (V_{be3} - V_{be4}) + i_1 R$$

where

$$(V_{be1} - V_{be2}) = \alpha \ln \left[\frac{I_1 - ki_1}{I_1 + ki_1} \right]$$

and

$$(V_{be3} - V_{be4}) = \alpha \ln \left[\frac{I_1 + i_1}{I_1 - i_1} \right] .$$

Differentiating V_{in} and substituting for base–emitter voltages,

$$\mathrm{d}V_{in} = R\,\mathrm{d}i_1 + \frac{2\alpha(1 - k^2)x^2\,\mathrm{d}i_1}{I_1(1 - x^2)(1 - k^2x^2)} \tag{29}$$

where

$$x = \frac{i_1}{I_1} \tag{30}$$

and

$$k = \frac{\beta - 1}{\beta + 1} . \tag{31}$$

Therefore

$$N(x) = \frac{2\alpha(1 - k^2)x^2}{I_1R\{(1 - x^2)(1 - k^2x^2)\}} . \tag{32}$$

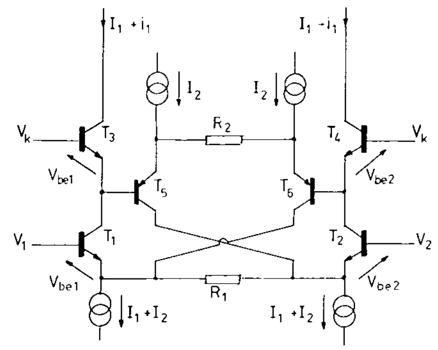

Fig. 14. Indirect error feedback.

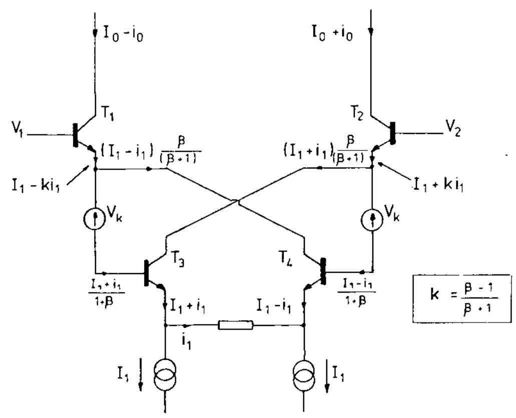

Fig. 15. Modified error feedforward with indirect V_{be} compensation.

This circuit topology reveals that if transistor matching is achieved, the nonlinearities are mainly dependent upon transistor β.

In order to obtain an adequate dynamic range without transistor saturation, constant offset voltages V_k are required (as shown in Fig. 15). However, in situations where the input signal is controlled and small, V_k can be set to zero. Such an application is to use this circuit as the error amplifier for a single long-tail pair, as shown in Fig. 7. This compound circuit is illustrated in Fig. 16.

Defining λ, x, and y as in Section 3.2, then if

$$\lambda = \frac{R_2}{R_1} \tag{33}$$

we have

$$\mathrm{d}V_{in} = R_1\,\mathrm{d}i_0 + \frac{4\alpha^2(1 - k^2)y^2\,\mathrm{d}i_0}{[I_1(1 - x^2)\{I_2R_2(1 - y^2)(1 - k^2y^2) + 2\alpha(1 - k^2)y^2\} + 2\alpha\lambda I_2(1 - y^2)(1 - k^2y^2)]} . \tag{34}$$

Therefore

$$N(x, y) = \frac{4\alpha^2(1 - k^2)y^2}{\lambda I_1I_2R_1{}^2[(1 - y^2)(1 - k^2y^2)(1 + 2\alpha/I_1R_1 - x^2) + (2\alpha/\lambda I_2R_1)(1 - k^2)y^2(1 - x^2)]} . \tag{35}$$

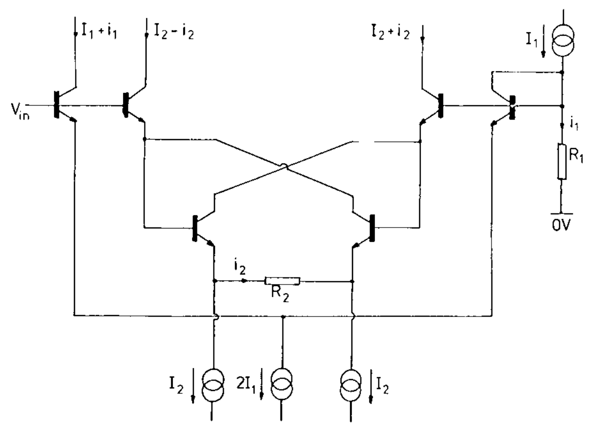

Fig. 16. Single long-tail pair using an error feedforward correction with indirect V_{be} compensation.

Hence comparing Eqs. (35) and (24), there is a further reduction of distortion of approximately $(1 - k^2)$, where k is just less than 1.

6 CONCLUSIONS

A series of circuit topologies were presented which are suitable for the input and subsequent stages of audio amplifiers. The aim has been to show that partial linearization can be achieved without recourse to excessive negative feedback. The circuits require the implementation of a balance condition which is essentially noncritical, provided that only moderate cell transconductance is required.

As an aid to circuit comparison the parameter IDF was introduced which readily expressed nonlinearities as a function of amplifier current loading factors. These expressions can be approximated still further by letting terms of the form $(1 - x^2) \rightarrow 1$ with the assumption of modest loading factors.

It is hoped that some of the circuits will prove useful to the designers of audio amplifiers and allow enhanced performance by minimizing both nonlinearity and loop-gain requirements, which have a strong correlation with transient distortion phenomena.

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