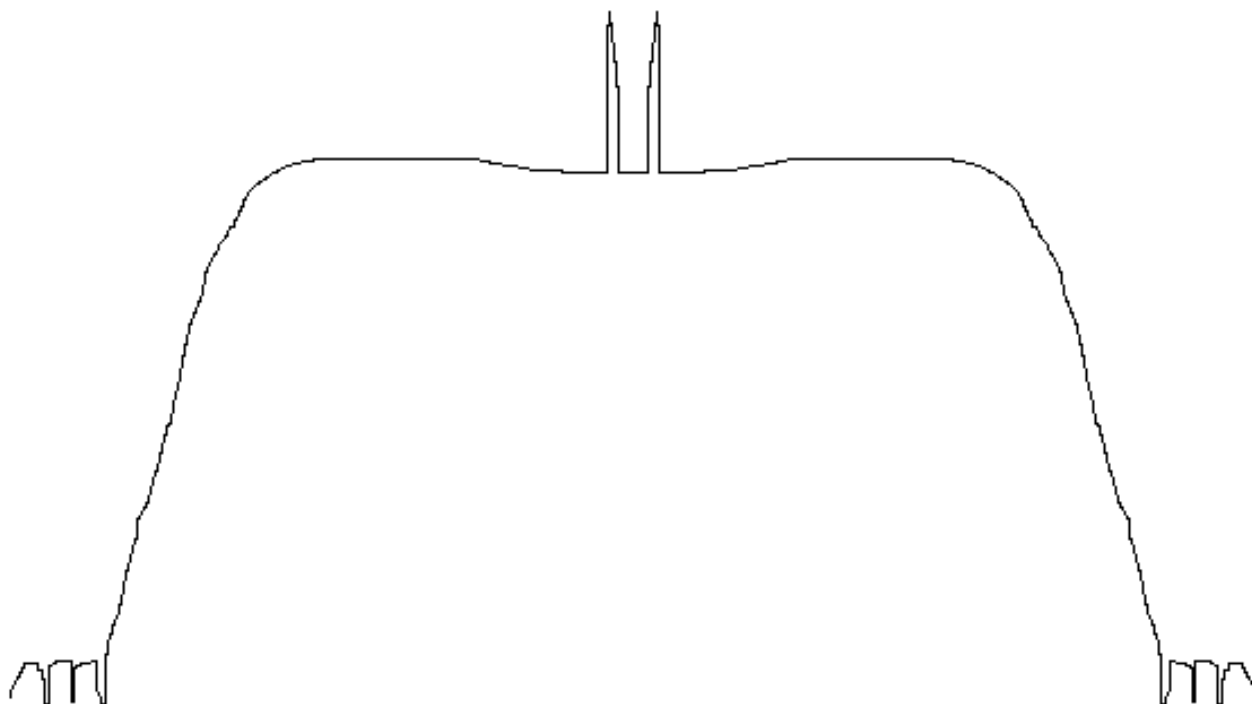


When you look at the quantization noise spectrum of a DSD signal, or any other sigma-delta modulate, it usually looks roughly like Figure 1.



*Figure 1: Sketch of a typical DSD/sigma-delta spectrum, drawn from 0 Hz to the sample rate.*

The noise shaping keeps the quantization noise quite low in the band of interest (audio band for an audio converter). Above the band of interest, the power spectral density of the quantization noise increases very quickly, and then becomes more or less flat.

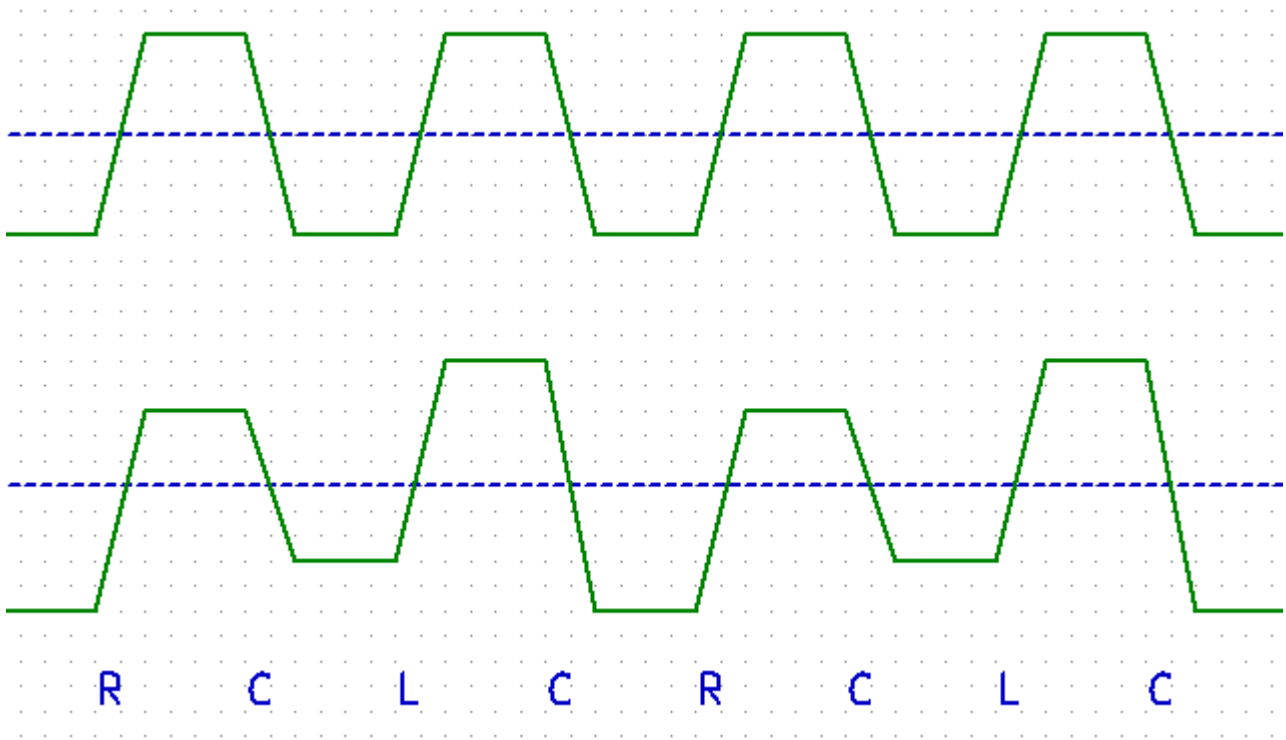
A straightforward single-bit converter will produce idle tones around half the sample rate, which I've drawn as the narrow peaks in the middle. That is, when playing silence with 0 DC offset, there is just an idle tone at exactly half the sample rate, but the sketch shows what happens when there is a small DC offset. You then get a tone just below half the sample rate, and its alias will then lie just above half the sample rate. When playing music, the frequencies of these tones get modulated by the music.

When you amplitude- or phase-modulate this signal with something having spectral content in the frequency range where the quantization noise spectrum is high, it will mix some of the quantization noise down to low frequencies, which will affect the audio noise floor. If you modulate it with a tone at or near half the sample rate, the idle tones can be mixed down into the audio band, so you get tones that are frequency-modulated by the music added to the audio signal.

The DSD signal itself obviously has spectral content at the frequencies that the DSD signal shouldn't mix with. Hence, when some of the DSD signal crosstalks to the voltage reference, amplitude-modulating the DAC output signal, or to the clock, phase-modulating the output signal, it can disturb the audio spectrum.

If the data signal switched exactly at the falling edges of the bit clock and if the crosstalk were a simple weighted addition, Figure 2 would show how this would lead to jitter at the rising clock edges. The dashed blue line is supposed to be the switching threshold of the level converter for the bit clock at the DAC input, the upper green signal is an undisturbed clock and the lower green signal a bit clock that has a data signal added to it that shifts the signal down, up, down, up... (The

amount of added data signal is grossly exaggerated to make it visible.) The crossings of the switching threshold shift due to this, the letter indicates whether it has shifted left, right or remained at the correct place.



*Figure 2: Oversimplified sketch showing how a data signal added to the clock shifts the crossings of the switching threshold*

Besides the exaggerated amount of crosstalk, there is another difference with reality. In reality, the crosstalk will normally be inductive or capacitive, and will therefore consist of spikes that occur when the data signal switches. If the spikes have damped out sufficiently by the time the clock switches, they won't do any harm. The degradation will therefore depend in a complicated way on the timing of the data with respect to the clock. When the data and clock signals pass through a relatively long cable, you also have to take reflections of the switching data signals into account.

There is not much shift of the clock necessary to mess up the noise floor. I haven't calculated how much is allowed for a given noise floor degradation for this specific DAC, but the last time I did such a calculation (and verified it with simulations), it was a matter of picoseconds.