

## Lynx30 DAC Module

This design owes its existence in many respects to a coincidence of random events that occurred in the second half of the last (2005) year, which led to the fact that I had at my disposal a D20400 hybrid DAC from UltraAnalog. Having heard a lot about the unique properties of this product, I could not help but use the given opportunity to test in practice this already legendary and now not produced DAC.

A few words about the design basis - D20400 DAC. The appearance of this device is shown in Fig. 1:



Figure: 10 Exterior view of one of the instances of assembly D20400

A printed circuit board with elements of a DAC itself, a generator of all service signals on a custom masked PLM, a sampling-storage device and a reference voltage source are placed in a polypropylene case with dimensions of 76 x 50 mm. The functional diagram of the D20400 is shown in Fig. 2:

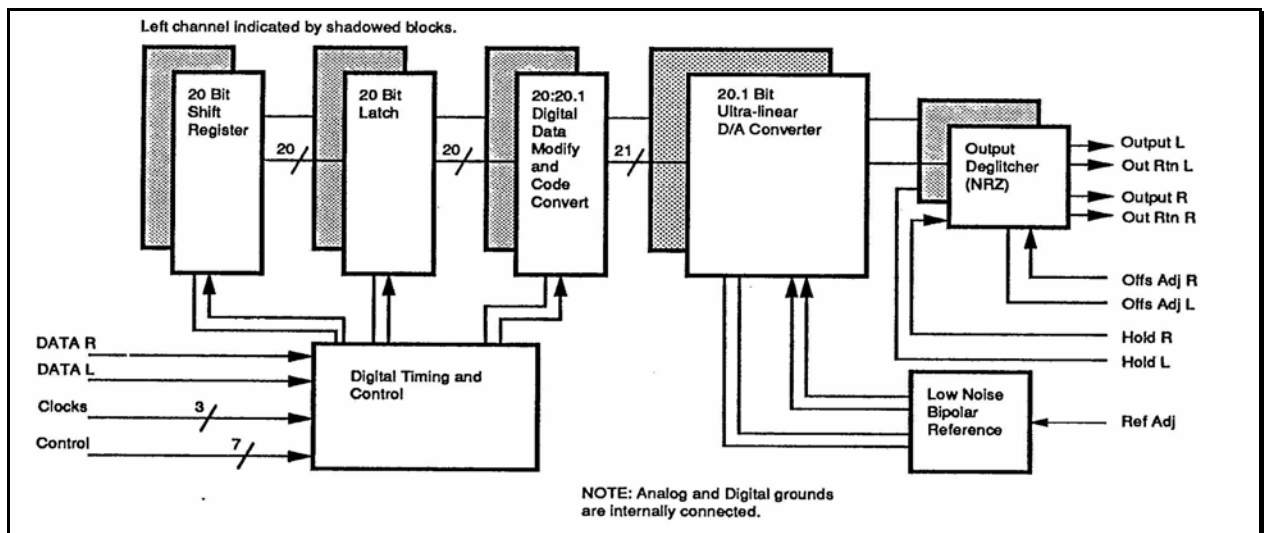


Fig. 2

The converter is built according to the so-called. "Hybrid compound" scheme. It is based on high-linearity conversion of low-order bits using a monolithic digital-to-analog converter with a small bit depth, guaranteed monotonicity on the entire scale and differential nonlinearity no worse than  $\frac{1}{2} \dots \frac{1}{4}$  LSM, and conversion of high-order bits in a discrete digital-to-analog converter performed on CMOS switches and a precision resistor matrix. The D20400 uses a monolithic CMOS device DAC7541 (AD7541A) as a DAC for the least significant twelve bits, which provides 14-bit monotonicity and differential nonlinearity no worse than  $\frac{1}{2}$  LSB. The most significant 6 bits are converted by a discrete DAC based on 4051 CMOS switches and a resistor array calibrated at the factory.

All control signals, both low-order DAC and high-order keys, are generated by a custom PLM. It also converts input data formats, inverts the signal independently by channels (for example, for differential switching on the module), etc. secondary functions.

The analog output signal scale is set by a precision low-noise reference, one for both channels, which guarantees a high degree of output voltage identity. Moreover, for the same purpose, both channels use a single resistor matrix that sets the weights of the most significant bits. These measures made it possible to minimize the mutual drift of the channels, both from temperature changes and from natural aging of elements.

Unfortunately, with all the advantages at low conversion frequencies, such a structure does not allow direct operation at conversion periods of less than 1 ... 2ms, due to the fact that even with careful selection and coordination of timing diagrams for the operation of the SZR and DAC keys, the glitch energy will be sufficient is large and the EDD will not exceed 10 ... 12 digits. To solve this problem at the DAC output, the D20400 developers used a sample-store device, and the sample time can be set arbitrarily, since UVX keys have separate independent control inputs. Since the value of the equivalent conversion jitter depends on the quality of the keys, mainly on their aperture uncertainty, the value of the equivalent jitter of the conversion depends, then the MIS keys SD540x from Calogic are used in the UVC. providing signal propagation time in the channel of the key transistor less than 600 ps and its own aperture uncertainty less than 0.8 ps and precision op amps. Power supply of both D20400 channels is combined, while the isolation between the channels is more than 98dB at a frequency of 10kHz. The device has a voltage output, and the full conversion scale corresponds to the voltage amplitude at the output  $\pm 5V$ . The D20400 consumes a total power of about 1.7 ... 1.8W from all power supplies.

To implement a functionally complete digital-to-analog converter module, a well-known and well-proven block diagram was chosen, shown in Fig. 3:

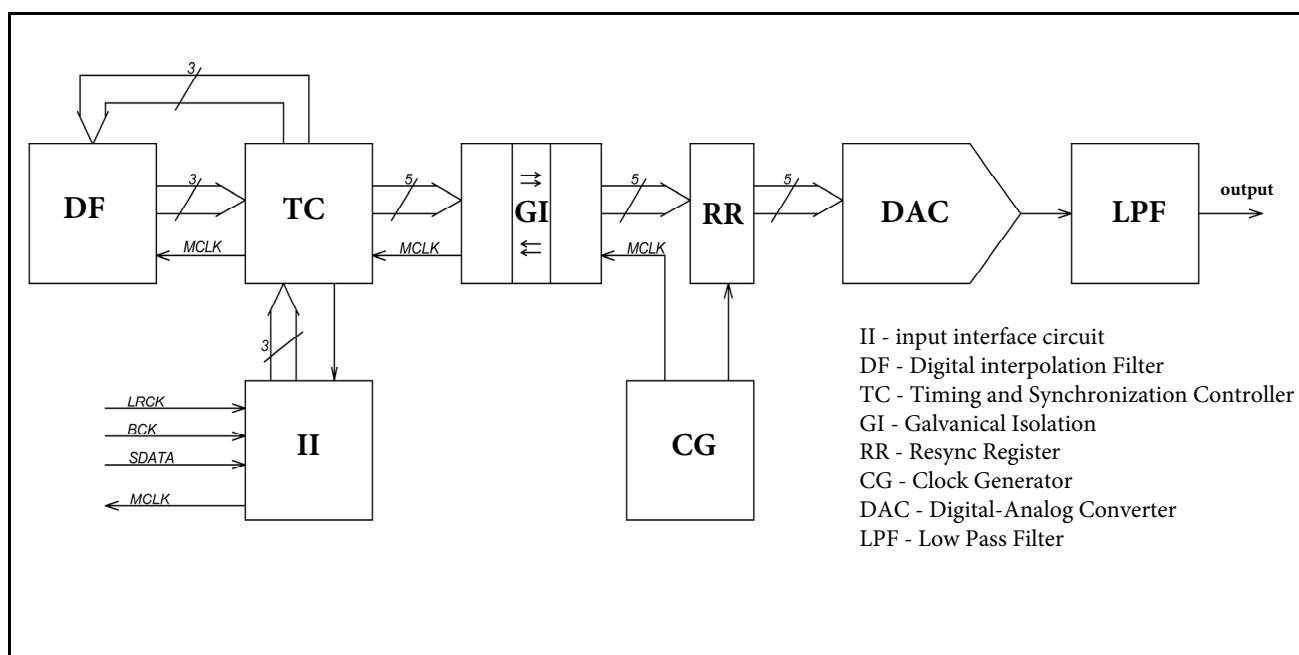


Fig. 3

The II (input interface) circuit matches the logic levels of the digital devices of the module with the logic levels of external devices and provides the specified level of noise immunity of the DAC module interface and the source of the audio stream. When transmitting data over short distances (up to 20 ... 30cm), the interface can be standard TTL / CMOS, for long transmission distances it is desirable, and often mandatory, to use differential interfaces such as RS422 / RS485, LVDS, ECL.

DF (digital interpolation filter) is a mandatory device for audio D / A converters when working with sampling frequencies close to the doubled upper frequency of the audio spectrum, i.e. 44.1 and 48kHz. The use of a digital filter with multiple (4-fold or 8-fold) oversampling shifts the spectrum of sampling products to the frequency range above 100 kHz and makes it possible to significantly reduce the requirements for the reconstruction analog filter both in terms of the squareness factor and the amount of attenuation in the suppression band, at least, in the region close to the cutoff frequency of the LPF. The quality of the DF, i.e. its order, the number of taps, the digit capacity of the calculations, the algorithm for rounding the output data to the digit capacity of the DAC largely determine the final sound quality of a device equipped with a digital converter.

The timing and synchronization controller (TC) provides optimal, from the point of view of noise immunity, temporal relationships of the signals fed to the DF and the control DACs. This device is very convenient to implement using programmable logic, since the physical dimensions of the systems for generating grids of clock signals and resynchronization of receiving / issuing data according to such grids can be very significant, in addition, FPGAs make it possible to change the project "on the fly" and thus select the optimal modes data transmission in the time domain.

Galvanic isolation (GI) allows many times to reduce the level of asynchronous interference that penetrates from digital devices into the analog part along the common wire ("ground"). In fact, it is the GI that determines the division of the device into digital and analog parts. Everything to the right of the GI belongs to the analog part.

The clock generator (CG) generates the main clock signal, from which all other clock signals are generated in the synchronous system. It also clocks the resynchronization register (RR) - a device designed to eliminate instantaneous time instabilities of the edges of the DAC control signals, i.e. jitter suppression. After RR, the value of instantaneous temporal instability is determined only by the phase noise of the clock generator and the aperture uncertainty of the register triggers. All instabilities present in the signals at the inputs of the RR, if their value does not exceed  $\frac{1}{4}$  of the clock frequency period, are completely eliminated by resynchronization.

A digital-to-analog converter (DAC) converts a digital data stream into an analog signal, and a low-pass filter (LPF) ensures, to a greater or lesser extent, the fulfillment of the conditions of the Kotelnikov-Shannon theorem. Conversion of digital data into an analog signal can be carried out in several ways, the most common of which is parallel, by summing the weight signals in the amplitude domain (so-called multibit or parallel DACs), by changing the distribution of calibrated single samples in the time domain (PWM, PFM transformation) and, as a kind of the latter, by changing the distribution in the time domain of the signal increment in relation to the previous sample, the so-called. delta transformation. The latter method and its varieties provide very high static accuracy and accuracy of transformation of deterministic signals, but due to the presence of interdependence of neighboring samples due to the nature of such transformation, they distort the statistical characteristics of random signals. In particular, the ACP of the converted signal will be a convolution of the ACP of the converted signal and the DF of the converter.

Parallel DACs provide lower static accuracy, are subject to various kinds of TC (transfer characteristic) defects (for example, non-monotonicity) and are very complex and expensive to manufacture with the required accuracy higher than 16 ... 17 bits (when the weight of the least significant bit becomes comparable to the values of leakage signals in semiconductor structures and on the surface of substrates and boards), but at the same time the length of their CP is always less than or equal to the sampling period, the conversion of neighboring samples occurs statistically independently, and the probabilistic characteristics of random signals, to which, according to many criteria, sound can also be attributed, are not distorted. Perhaps this explains the subjective advantage of sounding parallel DACs over delta converters.

The schematic electrical diagram of the DAC module, based on the block diagram discussed above, is shown in Fig. 4:

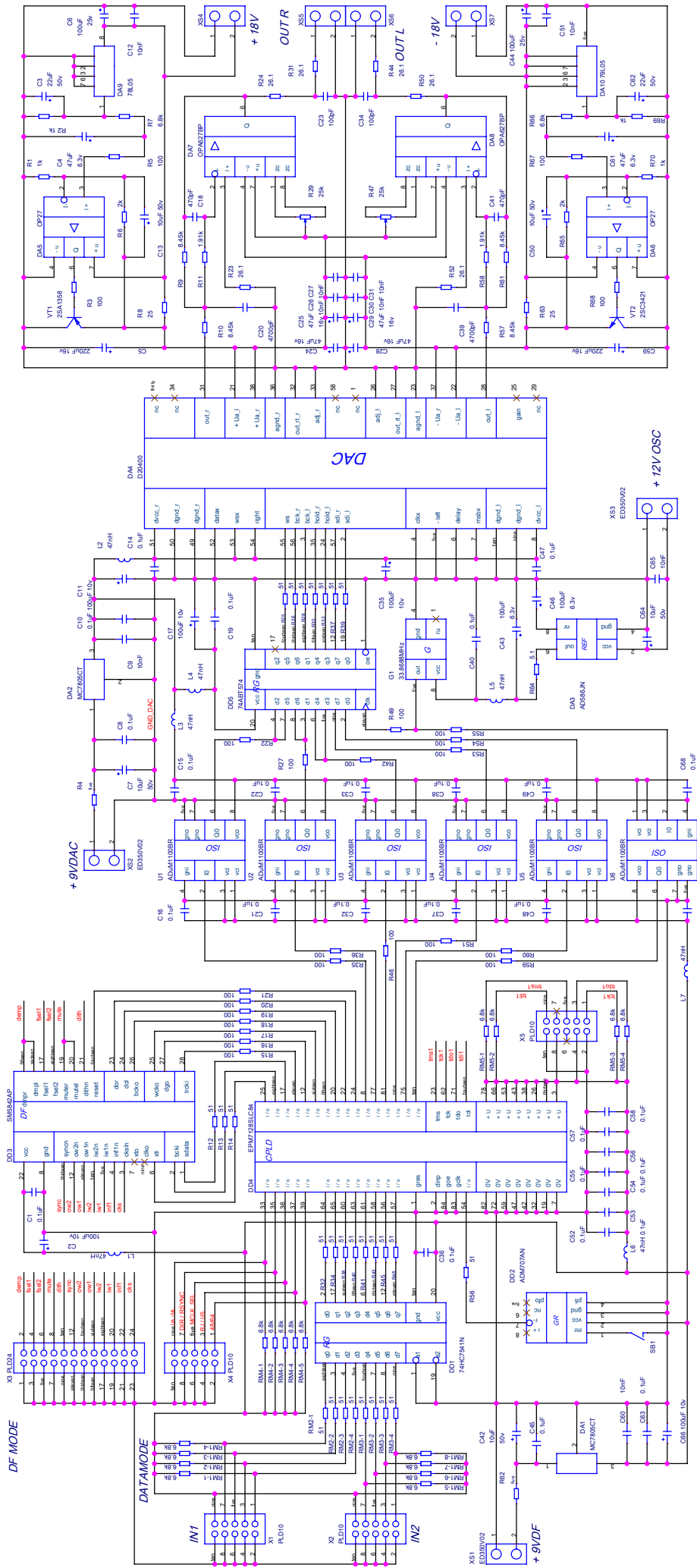


Figure: 4

The input interface of the device is provided by a specialized microcircuit DD1 of type 74HC7541, containing 8 Schmitt triggers with high load capacity, which allows, on the one hand, due to the hysteresis of the switching characteristics, to increase the noise immunity of the inputs, and, on the other hand, to ensure reliable transmission of clock frequency up to 20 MHz over a distance to 30cm without additional measures. The primary resynchronization of the input signals, their reduction to the form perceived by the DF, the formation of the necessary clock frequencies, as well as the formation of the most favorable timings for the DAC control signals, is performed in the FPGA DD4 of the EPM7128SLC84-15 type manufactured by Altera. The use of the slowest device in the rather old MAX7000S series is primarily due to the low electromagnetic interference generated by these FPGAs.

Since this DAC module was developed to work exclusively with the CDDA format, as with the only real high-quality playback format to date, the well-known NPC SM5842 filter was used as a digital filter, operating up to an input signal sampling frequency of 50 kHz. Compared to the more modern filter SM5847, which has a completely identical structure, but allows operation up to sampling rates of 200 kHz, the SM5842, as a device based on slower LEs, provides a lower level of interference radiated into the air and induced in the supply circuits by 3 ... 6 dB.

The initial power-on reset of all digital ICs is provided by a dedicated DD2 reset generator, type ADM707.

The digital part is powered by a typical 7805 regulator, which provides the required level of stability and noise in the digital power supply.

Galvanic isolation of digital and analog circuits is provided using high-speed digital isolators U1... U6 type ADuM1100BR.

The clock generator and resynchronization register are located on the "analog" side of the circuit. These devices are completely similar to those in previous DAC designs. As a resynchronization register, an 8-bit DD5 register of type 74ABT574 is used, which has the lowest level of intrinsic jitter of all TTL / CMOS microcircuits known to me. The clock generator is a sealed integral GXO-U100H from Golledge, which has excellent characteristics at a relatively low price. Alternatively, TENT Labs generators with similar or slightly better performance can be recommended. Since the parameters of the generator, in particular the phase noise level, strongly depend on the quality of the power supply, the generator is powered from an AD586 type DA3 integrated reference, structured ION - noise filter - regulating element. With external noise filter capacitors, this device allows you to get the noise level at the output voltage below -117 ... 120dB.

The resynchronization register and the digital part of the DAC itself are powered by a standard DA2 stabilizer of the 7805 type. Perhaps the use of the 7805 will cause confusion among many, but this is a completely deliberate step based on both measurements and subjective comparisons. In the course of preliminary experiments, it turned out that the power supply of the resynchronization register and the digital part of the DAC from the 7805 subjectively and objectively does not deteriorate the properties of the device in comparison with the power supply from a discrete stabilizer. True, the origin of the stabilizer was fundamental. Russian-made devices, as well as SGS Thomson, ROHM, Philips and Texas Instruments have about twice - three more noise and 10 ... 12 dB worse input noise suppression at frequencies of 10 ... 100 kHz than similar stabilizer chips manufactured by ONS, TS, JRC and Mitsubishi. The noise level of the 7805 stabilizers of the last three companies did not exceed 22 ... 25  $\mu$ V (RMS) in the frequency band up to 80 kHz, and the cutoff frequency of excess noise for ONS products was only 1.4 kHz, which is two times lower than that of TI microcircuits and 2.5 times lower. than Thomson stabilizers. Therefore, in this stabilizer, only microcircuits of these companies should be used.

The actual conversion of the digital stream into an analog signal is carried out in the module type D20400 from UltraAnalog. The assembly is included according to a typical scheme for operation in two-channel mode. In the study of its properties, it was found that the level of distortion and the realized dynamic range significantly depend on the temporal position of the resolution pulse for the built-in IHCs in relation to the pulse of the conversion command. The use of FPGAs to build a timing generator made it possible to quickly change the position of the deglitching pulse (starting the UVC into storage mode) with a discreteness of about 30 ns during the DAC tuning process and select its optimal location on the time axis for this D20400 instance. Besides

Moreover, a positive effect was observed from a decrease (compared to the typical) in the duration of the deglitching pulse. After a series of experiments, the optimal location and duration of the control pulses of the IHR were selected, which were reflected in the FPGA design for the available D20400 instance.

The output signal of the DAC goes to the recovery LPF with a cutoff frequency of about 40 kHz. I chose this frequency value as a result of many years of experiments with various types of DACs. According to my observations, for parallel DACs with 8x oversampling, the use of a 2nd order low-pass filter with a Butterworth characteristic and a cutoff frequency of 38 ... 42 kHz is optimal from the point of view of the subjective sound of these devices. The second order filter itself is made according to the scheme with a multiloop OS. Compared to the Salen - Kelly circuit, such a circuit has an advantage when operating under conditions of a high level of RF components (which is exactly the case when working in the DAC post - filter) due to the fact that in the first filter link the capacitor is grounded and not included in op-amp output circuit. This significantly reduces the level of HF components in the OOS circuit of the op-amp and excludes its input overload and the growth of intermodulation distortion. Well-known OPA627 devices are used as an op-amp, which are distinguished by a low level of distortion and noise. The signal from the outputs of the op-amp low-pass filter through the RC T - filter that prevents the ingress of external noise induced on the connecting cable into the OA circuit of the op amp is fed to the analog signal output connectors.

The power supply of the analog part of the D20400, the UVH circuits and the output low-pass filter is carried out from discrete parallel stabilizers of the "ION - filter - OA" type. The stabilizer circuit is quite trivial, with the exception of one peculiarity. Low-power stabilizers 78L05 and 79L05 are used as a reference. Their relatively high noise level (20 ... 25  $\mu\text{V}$ ) is very effectively reduced by means of a noise filter, as a result of which the noise at the output of  $\pm 15\text{V}$  stabilizers is only 2 ... 3  $\mu\text{V}$  in the frequency band 100Hz ... 80kHz. Since the current of the useful signal does not flow through these stabilizers, their own linearity and response to a pulsed load is absolutely unimportant. This solution made it possible to create symmetrical stabilizer circuits independent of each other and with the op-amp powered only from its own input voltage without using the voltage of the other arm.

The appearance of the assembled Lynx30 DAC module is shown in Fig. 5:

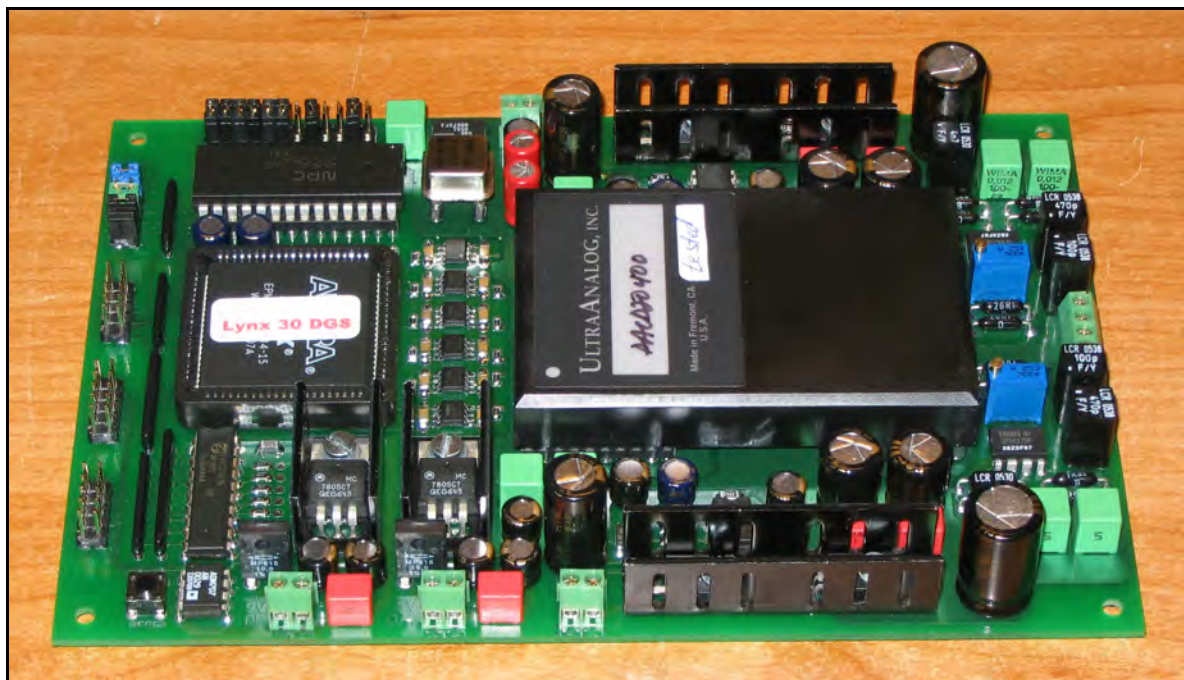


Figure: 5 Lynx30 DAC board layout

The Lynx30 DAC element base is in many respects similar to that of previous devices. In the digital part, SMD resistors of standard sizes 0805 and 1206 from Koa are used, SMD capacitors of size 1206 from Kemet. Electrolytic capacitors bypassing the power supply of the digital microcircuits of the module - Black Gate PK. The power supply regulator of the generator uses Black Gate NX as the blocking capacitor and the RC noise filter capacitor, which have very low "capacitive" noise. The same capacitors are used in the filter.



noise ION of power stabilizers of the analog part. In addition, to minimize the noise of analog stabilizers, their circuits use metal-film SMD resistors of the MELF type, which have less noise and better temperature stability compared to standard SMD resistors based on ruthenium oxide. The outputs of the analog power supply stabilizers are shunted by Black Gate FK capacitors, which are distinguished by their high intrinsic linearity and very low dependence of the capacitance on the applied voltage and AC component. To reduce the impedance of the supply rails at high frequencies, Wima FKP2 foil polypropylene series are installed in parallel to the electrolytic capacitors.

The analog signal circuits (low-pass reconstruction filters) use precision (0.1%) metal film resistors of the RC55 series manufactured by Welwyn, which are characterized by very high thermal stability and extremely low levels of both excess and current noise. In addition, resistors in this series have extremely low intrinsic distortion. Precision polystyrene tanks of the EXFS / HR series manufactured by LCR Components are used as low-pass filter capacitors. In addition to high stability, such capacitors have very low dielectric losses, which is beneficial in terms of the distortion introduced by the filter capacitors into the signal.

The Lynx30 DAC module has the following specifications (at 44.1kHz sampling rate):

1) rated output voltage, corresponding to full scale conversion, V (RMS)	3.53
2) the relative level of noise at the output (at zero input signal), dB	below -110
3) the relative level of harmonic distortion and interference in the 45 kHz frequency band for the test 16-bit signal (at the DF input) with a frequency of 918 Hz full scale, dB	- 104
4) the relative level of harmonic distortion and interference in the frequency band of 45 kHz for a test 16-bit signal with a frequency of 918 Hz with a level of -80 dB, dB	- 27
5) Noise level in the 100 MHz band at analog outputs, dB	below -76
6) RMS jitter of the clock generator signal, ps	less than 4.5

The spectrum of the test signal with a level of -80dB is shown in Fig. 6:

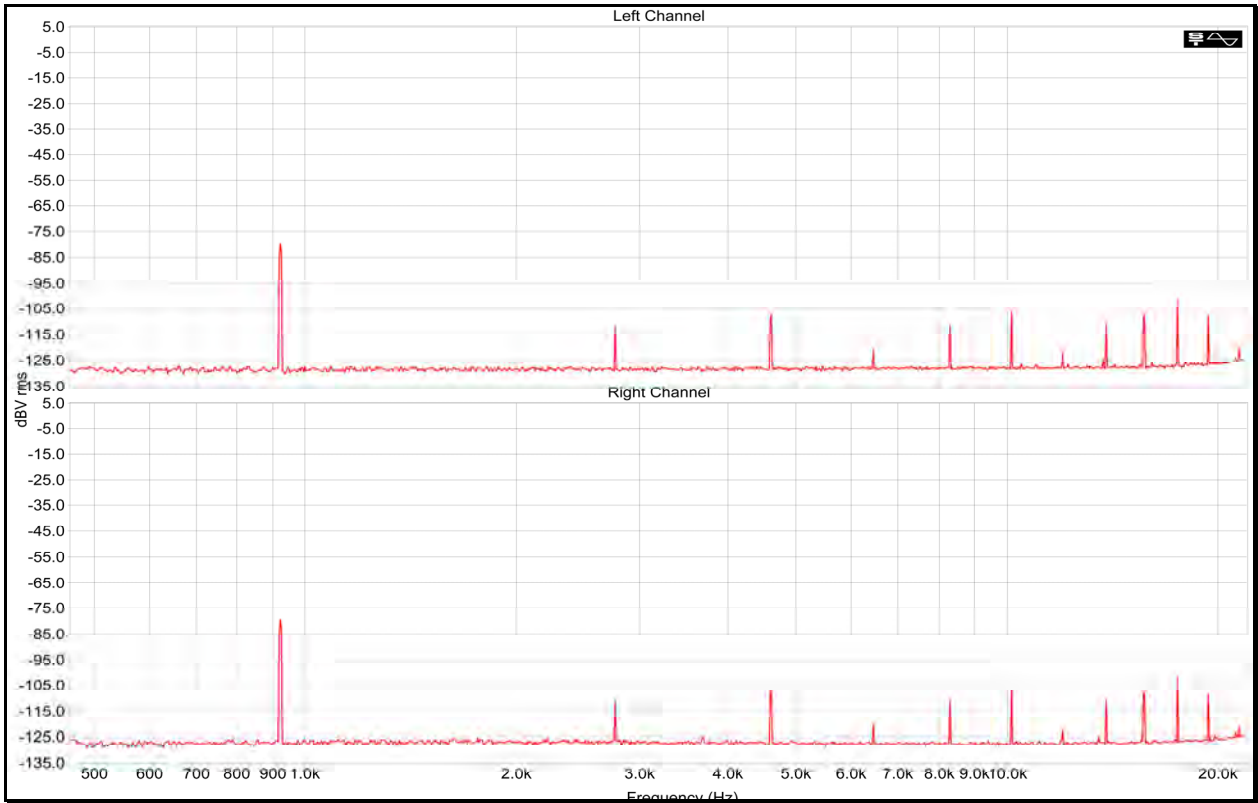


Figure: 10 Spectrum of 918Hz signal with -80dB level at the output of Lynx30 DAC

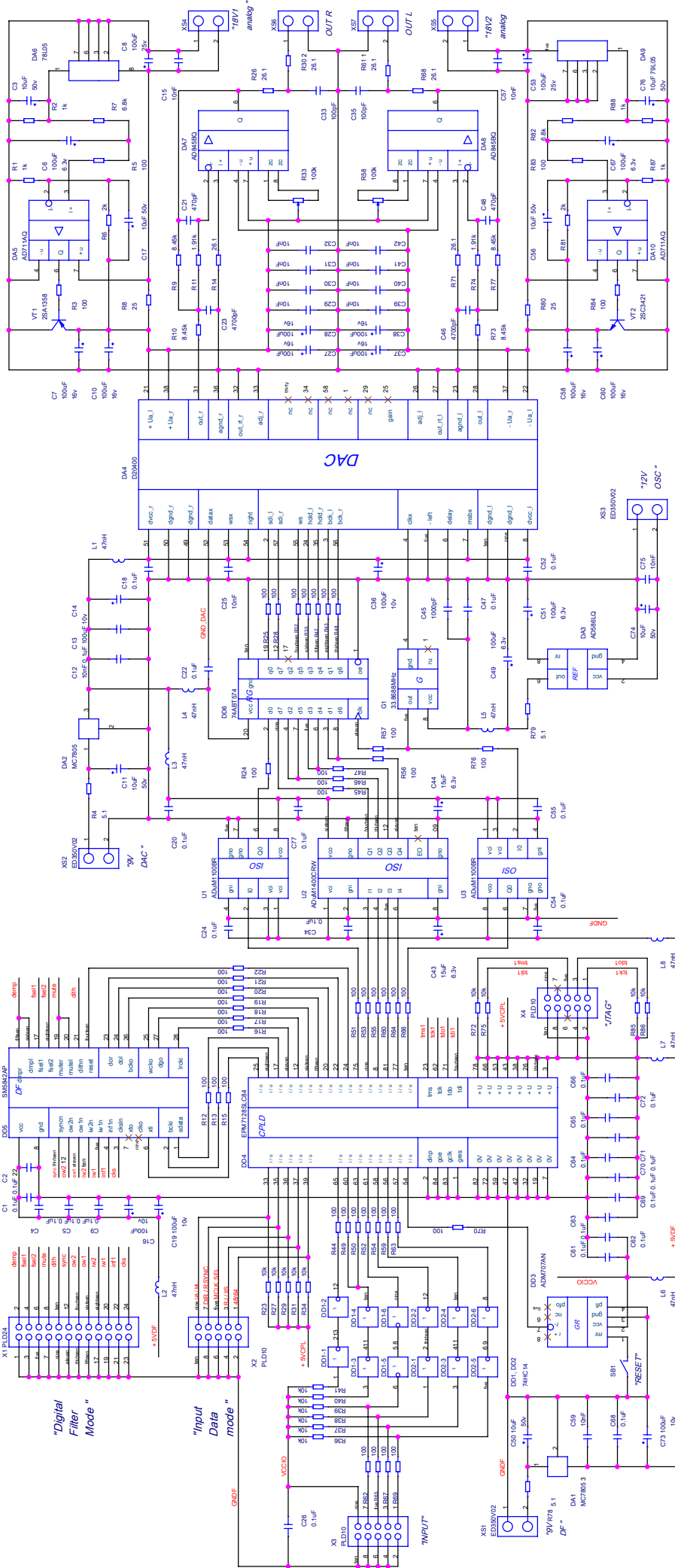


Figure: 7

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The spectra of signals of high levels are not indicative, since they mainly reflect the level of distortion of the measuring ADC. To obtain a real spectrum of the signal with a level of -80dB, an additional linear instrumentation amplifier with a transfer coefficient of 40dB based on an OPA637 op amp with a bandwidth of 30 kHz limited by an additional low-pass filter of the first order was used. Thus, the signal acting on the ADC input had a level of -40dBfs. The scale of the spectrogram amplitudes is calibrated in the true values of the signal level. Components with frequencies of 17, 18 and 19 kHz are increased against the true values by 4 dB due to ADC distortion.

Subjectively, the sound of the Lynx30 DAC can be described as crystal-clear, airy, but at the same time alive, natural and full.

The operation of the first copy of the device revealed a number of design flaws that were eliminated in the next version of the DAC - Lynx30V1. The main difference is the use of not separate ADuM1100 isolators for galvanic isolation of the digital and analog parts, but the use of the quad ADuM1400, the use of buffering on the Schmitt triggers on the digital inputs, and the use of the AD845 instead of the OPA627 in the output filter. The schematic diagram of the Lynx30V1 DAC is shown in Fig. 7, and the appearance of the assembled board is shown in Fig. 8:



Figure: 8 Lynx30v1 DAC board layout

The analysis of the work and functions of the first versions of the DAC allowed us to continue the development of the project in order to maximize the potential of the D20400 DAC. As a result, a new Lynx30v3 module was developed, significantly different from the first two. The digital part of the new module implements the reception of data from two inputs - one in TTL levels, the second - differential RS485 for DAC communication with remote sources of stream. FPGAs, digital filters and input receivers are powered from separate stabilizers in order to reduce possible mutual influence along the supply circuits. ISO150 is used instead of ADuM as galvanic isolators, since they generate less microwave interference. On the analog side, separate regulators are also used to supply the decouples, the resynchronization register and the D20400 input part.

Parallel analog stabilizers +/- 15V are made with the use of powerful MIS transistors in the regulating elements.

The reconstruction filter uses op-amps of the OP42 type, which have extremely high sound qualities, while the op-amp outputs are buffered by repeaters BUF04. This allowed the DAC to operate on a relatively low-impedance load without increasing distortion. A schematic diagram of the Lynx30v3 is shown in Fig. 9, and the appearance of the assembled device board is shown in Fig. ten:

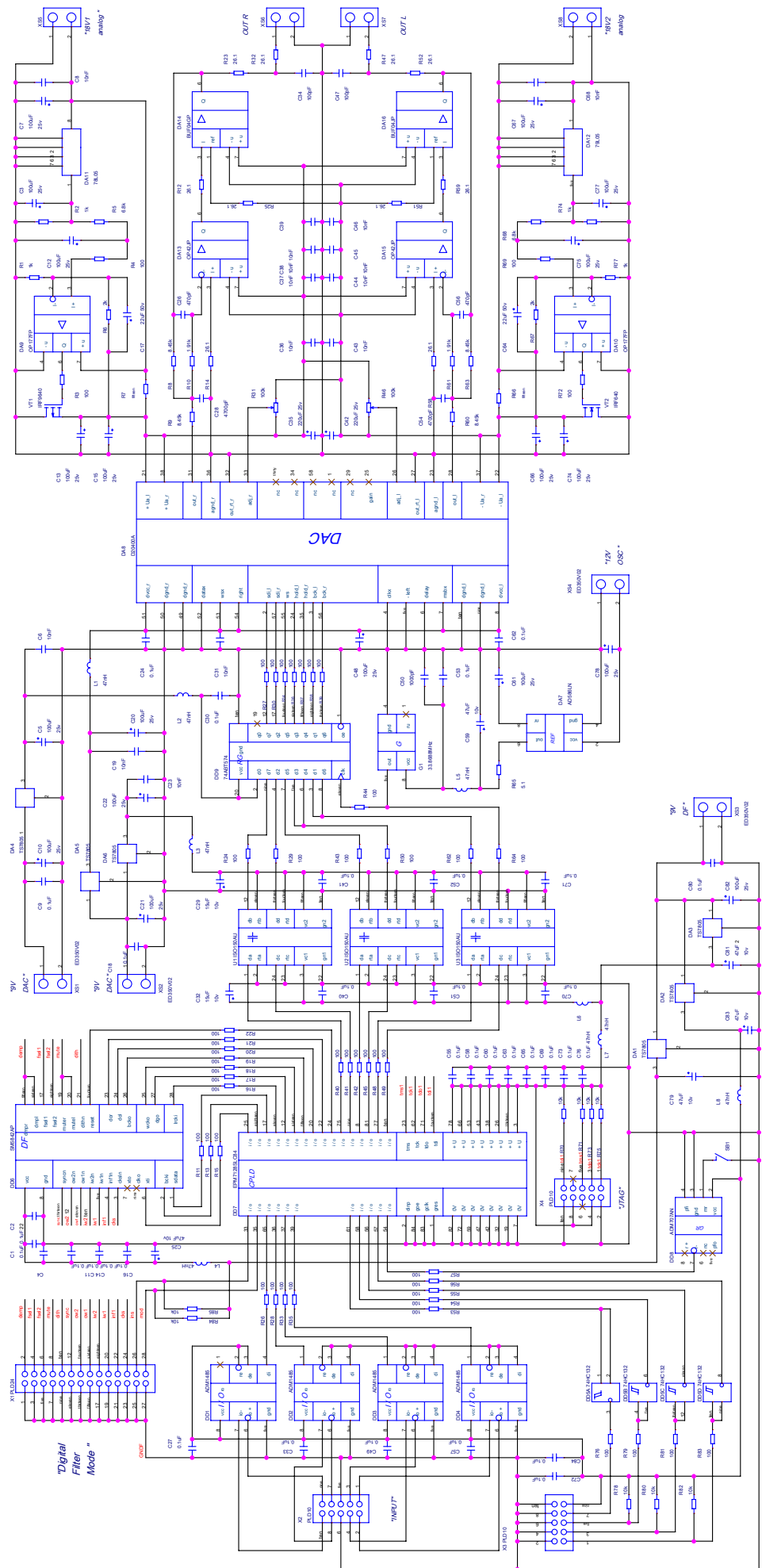


Figure: nine

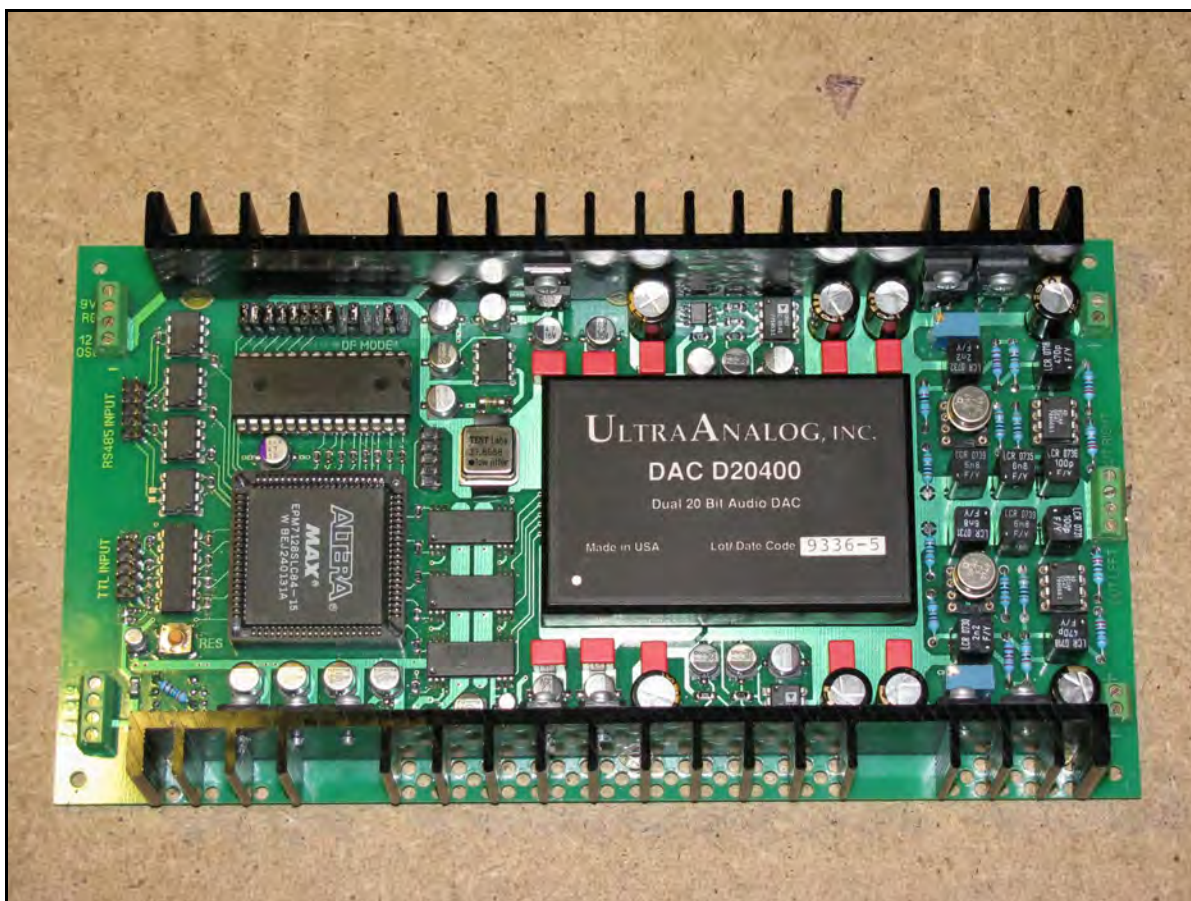


Figure: 10 Lynx30v3 DAC board layout

A subjective comparison of the DAC based on the Lynx30V3 module and the well-known Mark Levinson 30.5 processor, performed on the same D20400 modules when working with the Esoteric P700 CD transport, showed some advantage of the Lynx30V3 in the transmission of sound images, clarity and depth of the stereo picture, a greater emotional saturation reproduced with using Lynx30v3 music pieces.

In conclusion, I would like to thank from the bottom of my heart for the help and support of all those who, one way or another, directly or indirectly, took part in the creation of this device: my comrades and colleagues Sergey Zhukov (St. Petersburg), Alexander Bakharev ( St. Petersburg), Alexey Nikitin (London), Evgeny Artyomov (Moscow), Dmitry Bukvaryov (Moscow), Oleg Pilkevich (Kiev) Petersburg firms "[West-EI](#) ", "[Eltech](#) ", " Gamma ", "[EFO](#) ", "[Mega-Electronics](#) ", "[Samodelka.ru](#) ", The Novosibirsk firm " PS Electro ", as well as my wife, son and mother for constant attention, warmth and care, without which successful creativity would be impossible.

Dmitry Andronnikov  
St. Petersburg,  
January 2006 - March 2009