Lynx24 DAC Module

When developing this digital-to-analog converter for audio signals, the task was to create a device that could replace the well-known Lynx20 DAC, since it is becoming more difficult to get out of production AD1862, and there are more and more fakes and re-labeling of these microcircuits. In addition, lessons learned from making and customizing over twenty Lynx20s and personally operating four of them were taken into account.

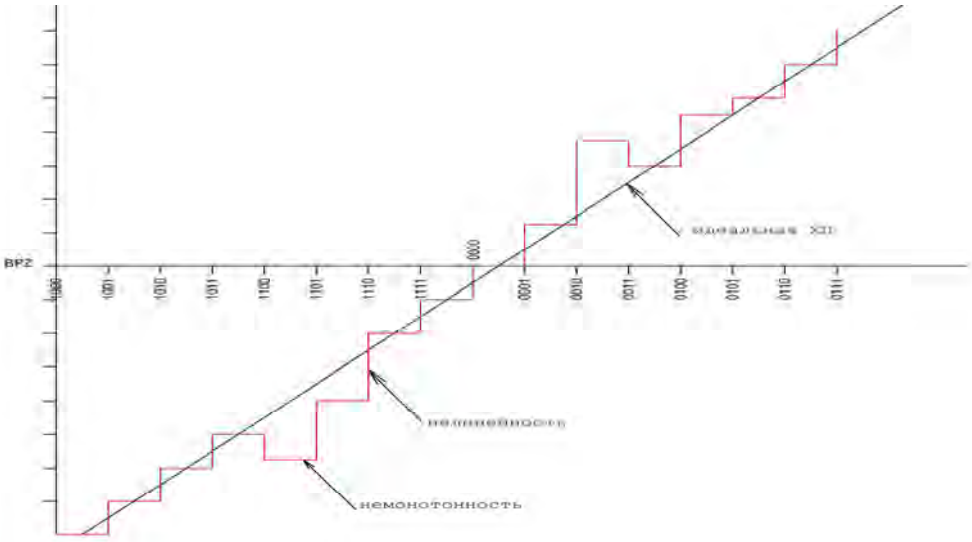
All the theoretical prerequisites for working on this design are the same as for the Lynx20, they are detailed in the article "The Last Song of an Analog" dedicated to this DAC. Therefore, now we will consider only those moments that determine the significant differences between the new DAC from the previous one.

The described device is intended for digital-to-analog conversion of audio signals recorded with a sampling frequency of up to 100 kHz and a bit depth of up to 24 with 8-fold oversampling in a digital filter. In 4x oversampling mode, the allowable operating sampling rate is 200 kHz. The DAC is connected to the digital signal source via a two-channel synchronous interface with time division of channels (I2S of various modifications). The DAC is designed to work in master mode, being a source of clock signals for a data reader / storage device. A lot has been said about the advantages of this mode in terms of the sound quality of the system and, in fact, only it (in various modifications) should be considered acceptable for high-end sound reproduction systems.

After studying and analyzing the range of multi-bit parallel DACs produced today (unfortunately, very scarce compared to the end of the last century, if we take only those devices that are available in the current production programs of manufacturers), the design of the Lynx24 was based on a very successful AD1865 by Analog Devices. This DAC on one substrate contains two matched and very close to each other, including the magnitude and shape of the nonlinearity of the conversion characteristic (CI), 18-bit devices similar to the AD1861 and the simplest logic that combines the inputs of the bit clock of both. The presence of two DACs of a high degree of identity in one package quite logically led to the idea of using them in differential connection for mutual compensation of HP nonlinearity. Given the fact

The first experiments with the AD1865N-K gave very encouraging results - without any additional actions for signals with a level of -30 ... 40dB, it was possible to obtain an effective dynamic range (DE) for an 18-bit sinusoidal signal 104 ... 106dB, i.e. almost completely implement the 18-bit scale of these microcircuits, which is close to that for most of the AD1862 in nondifferential switching. Soon, an experiment carried out with the AD1862N-J in the same layout showed that for arbitrarily taken copies of these microcircuits, differential switching does not give any advantages, and only when performing a very laborious and metrologically complex and expensive operation to select a DAC with the same character of HP nonlinearity does gain appear in EDD. Unfortunately, out of 32 AD1862N-J microcircuits, we managed to select only one pair, possessing this property. Therefore, the method of compensating for the nonlinearity of the CP due to the differential processing of differential signals is suitable only for devices that are deliberately selected by the type of nonlinearity of the CP.

Let us consider in more detail the issue of nonlinearity of the HP DAC. Recently, in various Internet resources, questions are often encountered, one way or another related to the bit depth and linearity of the DAC. Many of them are caused either by insufficient understanding of the nature of digital-to-analog conversion, or by an incorrect methodological approach to measuring and evaluating the parameters of converters. Let's try to pay attention to the most common mistakes. Very often, when trying to measure the parameters of a DAC with a large bit depth (for example, 24), the criterion for monotonicity and / or linearity of the conversion is the ability of the DAC to convert 1 LSB in the middle of the scale to the corresponding analog levels. In this case, the researcher feeds the mid-scale code (BPZ) to the DAC input with an increment of ± (1 ... 2) LSB (least significant bit) and sees steps at the output close to the analog value of the LSM, on the basis of which he makes a conclusion about the resolution and monotonicity of the DAC in 24 bits. Moreover, this conclusion is made even by some fairly qualified and competent specialists. However, this is methodologically and theoretically incorrect. Let's refer to the figure, which shows a typical conversion characteristic of a 4-bit DAC with various types of nonlinearities:



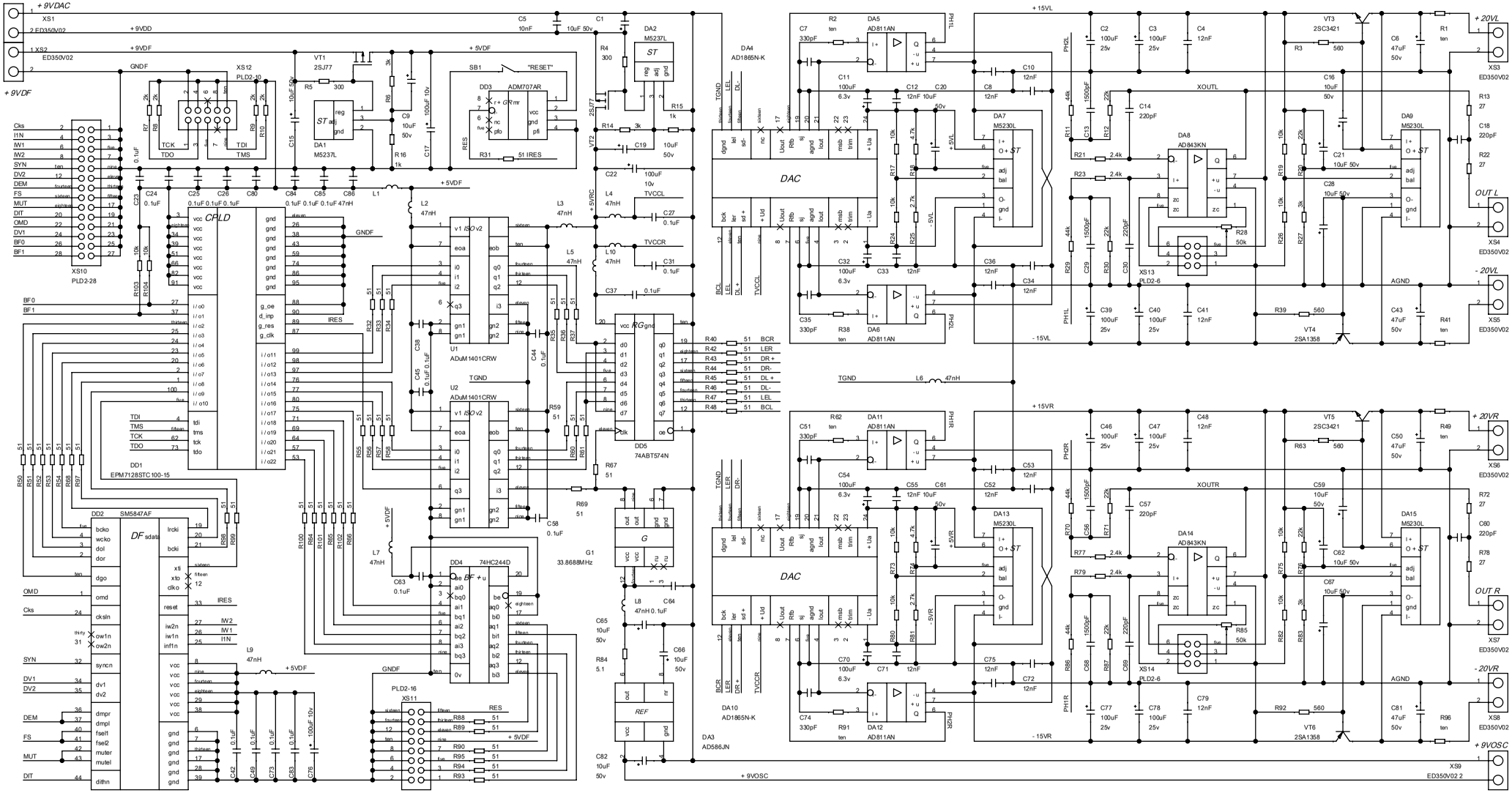
Monotonicity, nonlinearity and differential nonlinearity of the HP, as well as the associated resolution (otherwise - the effective number of bits, ENOB), by their nature cannot be determined for one point of the HP (unless, of course, it consists of 3 levels •). These are integral parameters of the ENTIRE scale and therefore in order to conclude that the 24-bit DAC is monotonous, it is necessary to measure at (16777216 - 2) points of the scale, giving an increment of ± 1 LSB for each point and make sure that the analog level for each increment of the code changes respectively. Only in this case can we talk about the monotony of the entire CP. It is even more difficult to measure the order of differential nonlinearity, since in this case it is necessary not only to ensure that the sign of the output signal increment corresponds to the sign of the code increment, but also the correspondence of the value of the output signal increment to the code increment. Therefore, the process of observing steps by the LSM value in the BPZ region in no way reflects the real properties of the DAC, but only shows the ability of the researcher to measure and observe signals of low levels.

A general criterion for monotonicity and differential nonlinearity of the transformation characteristic (but without determining specific zones of nonmonotonicity and polarity of the differential nonlinearity of the HP) can be a spectral analysis of the converted full scale signal. In this case, all deviations of the CP from the linear one manifest themselves in the form of an increase in nonlinear distortions, the value of which characterizes the total nonlinearity and non-monotonicity of the CP. The distortion level of an ideal digital sinusoidal signal converted by a DAC is uniquely related to the total nonlinearity of the HP and can be easily recalculated into the DAC ENOB using a simple formula:

ENOB = (-Dx - 2) ÷ 6,
Where Dx is the integral level of distortion, dB

The obtained value unambiguously characterizes the DAC resolution for arbitrary signals, in contrast to the observation of steps in the MZR in the region of the middle of the conversion scale, which carries practically no useful information and is usually used only for advertising purposes. The above applies to DACs of any conversion principle, with the exception of monotony, the property of which on the entire scale according to the principle of their operation is possessed by DACs of sequential action, i.e. devices based on delta transformation. Unfortunately, such devices are characterized by a more significant than the non-monotonicity of the CP, the disadvantage that manifests itself when converting random and pseudo-random signals - this is the mutual correlation between neighboring samples over a sufficiently large time interval, in any case, exceeding the sampling period. As a result, when processing a random signal in such a converter, its autocorrelation function will differ from the original one and is a convolution of the signal's own ACF and the converter CF. Apparently, the human hearing aid is quite good at determining the change in the statistical characteristics of signals, since most listeners absolutely accurately determine the difference in the sound of parallel and delta converters, and not in favor of the latter, even with the worst values of the distortion level in parallel devices.

The schematic diagram of the Lynx24 DAC is shown in the following figure:



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In many ways, it resembles the Lynx20 circuit, but there are also a number of significant differences due to the different element base and the experience gained during the operation of the Lynx20 and Lynx23. The main processing of the digital stream is carried out in the DF DD2 (SM5847) together with the FPGA DD1, which provides optimal conditions for the DF operation. For the formation of steep edges / falls of the input signals necessary for the correct operation of the FPGA, the input signals are transmitted through the drivers of the DD4 chip, which have the hysteresis properties of Schmitt triggers. Synchronous audio bus signals are fed to the buffer drivers via an IDC - compatible XS11 header. Clock signals with frequencies 384Fs, 192Fs and 96Fs are output to the same block (through the buffer drivers of the same DD4 microcircuit), with the help of which the reader is synchronized. XS11 pins 1 through 10 are compatible with those of the Lynx20DE DAC. It is advisable to connect to external reading devices either with individual shielded conductors or a flat ribbon cable. The length of the connection should not exceed 200 ... 300mm, otherwise you should apply signal transmission in differential form, for example, using LVDS, RS485 or ECL transceivers.

When developing this DAC, it was decided to abandon the control of the modes of operation of the digital converter through the FPGA and the possibility of organizing the reception of control signals via a serial port due to the fact that such control turned out to be practically unclaimed. Thanks to this, it was possible to significantly reduce the required amount of FPGA resources and use a different device, characterized by a lower level of noise induced in the power rails and the surrounding space. The new device uses FPGAs of the MAX7000S (EPM7128) series with the lowest performance grade, since the logic elements of such FPGAs, other things being equal, create less interference. In reality, the level of noise in the power supply (in the frequency range up to 10 GHz) from EPM7128 with a grade of 15ns is lower than that of an FPGA with a grade of 10ns by 2 ... 3dB. The current project is written to the FPGA using the standard JTAG interface through the XS12 connector.

DF operation modes and input bus format (RJ, I2S-48, I2S-64) are set
the appropriate set of jumpers on the XS10 block (the installed jumper corresponds to the supply of digital 0 to the control input). These switches can also be performed using TTL or 5V - CMOS logic signals supplied from the control system to the required pins. Below is a table of correspondence of jumpers to the control inputs of the digital filter:

Table 1

No. lockable contacts	Function or parameter being implemented	Parameter value	
		open	closed
12	The value of the clock frequency of the filter core	192Fs	256Fs
3 - 4	Format of the filter input signals Setting the width of the	**Do not use!**	working
5 - 6	input data	Set the required bit depth input data according reference data on the digital filter SM5847	
7 - 8	Setting the bit width of the input data 2		
9 - 10	Internal Office filter timing	Synchronization from Synchronization clock frequency	from the input bus
11 -12	Setting the division ratio clock frequency (DV2)	Choose according to recommendations reference data on CF SM5847	
13 - 14	Demphasis mode	included	switched off
15 - 16	Demphasis filter coefficients selection Mute mode	For Fs = 32kHz	For Fs = 44.1kHz
17 - 18		Signal muted	There is a signal
19 - 20	Dither mode	switched off	included
21 - 22	Selection of the oversampling factor	8x	4x
23 - 24	Setting the division ratio clock frequency (DV1)	Choose according to recommendations reference data on CF SM5847	
25 - 26	Input bus format	I2S	Right - justified
27 - 28	The number of pulses for writing data to the DAC register during the sampling period	64	48

The digital part of the device is powered from a + 5V stabilizer on DA1 of the M5237L and VT1 types through individual LC filters. The choice of the M5237 microcircuit is due to its good noise properties (in a 5-volt regulator its noise voltage is about 7 ... 10 times lower than that of standard 7805 regulators) and availability. The use of a p-МДП structure device as a regulating transistor makes it possible to slightly reduce the possible penetration of interference from the digital part into the primary source and vice versa due to the large value of the dynamic resistance of the PT channel.

The output signals for controlling the DAC microcircuits from the FPGA are fed to high-speed isolators U1 and U2 (ADuM 1401CRW), which, as in previous designs, serve for isolation

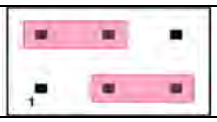
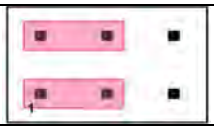
digital circuits from analog and digital-to-analog to reduce uncorrelated noise in the output analog signal. The clock generator and resynchronization register are isolated from the “digital” part of the circuit and placed on the “analog” side. The generator is powered from its own low-noise stabilizer, which is used as a precision reference type AD586 with the possibility of organizing a noise filter, which is used in this case. For better suppression of low-frequency noise components, the capacitance of the filter capacitor is increased by 10 times compared to the recommended one in the reference materials. Clock generator frequency

33.8688MHz (768Fs) - the same as in the Lynx20, manufactured by the English company Golledge. This generator, when powered from a very “clean” source, provides a jitter value not exceeding 5 ... 7 ps (depending on the instance). Resynchronization register - 74ABT574, in fact, has no alternative from the point of view of its own aperture uncertainty, its value (0.8 ... 1 ps) is approximately two times lower than that of the closest analogue 74AC574. The register, the “analog” side of the decoupling and the digital part of the DAC microcircuits are powered by their own stabilizer on DA2 and VT2 (similar to the power supply regulator of the “digital” part) through individual LC filters for each microcircuit.

The analog circuits of both channels are completely identical. Each channel uses one dual DAC type AD1865N-K (J). Its converters receive direct and inverted data in "two's complement" code, thereby providing antiphase increments of currents at their outputs. The output currents are converted to the corresponding voltages by stages on an op amp with a TOC type AD811, which has proven itself well. At the input of the current-voltage converters, capacitors C7, C35, C51, C74 are installed, which together with the output resistance of the current output of the DAC form a first-order low-pass filter with a cutoff frequency of about 500 ... 600 kHz, which reduces the level of RF components at the inputs of the converters. This measure made it possible to somewhat reduce (albeit insignificantly, because of the very high intrinsic speed of the op-amp converters) the intermode pedestal of the device.

The output antiphase signals are fed to the subtractive low-pass filter, which forms one of the two antiphase signals, and also carries out recovery filtering. The cutoff frequency of the filter is chosen equal to 40 kHz, which, on the one hand, is sufficient for effective filtering of the high-frequency components of the converted signal spectrum with 8x oversampling, and, on the other hand, it is one octave away from the upper frequency of the spectrum of the useful signal, which guarantees sufficient linearity of the phase response. The subtractive filter itself is made according to the scheme with multiloop OOS. Compared to the Salena-Kelly filter, the multiloop feedback circuit provides better suppression of high-frequency components with frequencies of 300 ... 400 kHz and higher due to the fact that the capacitors of the first filter link are not included in the feedback circuit (to the op-amp output), but are grounded and, thus, the work of the first link, perceiving the most "hard" signal from the point of view of the spectrum, does not depend on the frequency properties of the OA loop. In addition, the multi-loop OOS circuit allows you to very simply and beautifully implement a subtractive filter and thus combine both filtering and the formation of a single signal from a pair of differential in one stage. In the same stage, DC balancing of the op-amp was introduced in order to compensate for the displacement that occurs in the converter stages due to the significant bias currents of the op-amp with TOC and the DAC's own initial output current. The balancing circuit is built in such a way that as the opamp of the subtractive filter, the circuit with multi-loop OOS allows you to very simply and beautifully implement a subtractive filter and thus combine in one stage both filtering and the formation of a single signal from a pair of differential ones. In the same stage, DC balancing of the op-amp was introduced in order to compensate for the displacement that occurs in the converter stages due to the significant bias currents of the op-amp with TOC and the DAC's own initial output current. The balancing circuit is built in such a way that as the opamp of the subtractive filter, the circuit with multi-loop OOS allows you to very simply and beautifully implement a subtractive filter and thus combine in one stage both filtering and the formation of a single signal from a pair of differential ones. In the same stage, DC balancing of the op-amp was introduced in order to compensate for the displacement that occurs in the converter stages due to the significant bias currents of the op-amp with TOC and the DAC's own initial output current. The balancing circuit is built in such a way that as the opamp of the subtractive filter, arising in the cascades of converters due to significant displacement currents of the op-amp with TOC and its own initial output current of the DAC. The balancing circuit is built in such a way that as the opamp of the subtractive filter, arising in the
different types of microcircuits (for example, OPA627, OPA132, AD843, AD845, AD817, LT1363, LM6171). Wherein
you just need to install the appropriate jumpers on the XS13 and XS14 pads in such a way as to implement the balancing scheme of a specific op amp. The location of the jumpers on these blocks for the indicated types of op amps is shown in the table:

table 2

The type of op amp used in the LPF	Location of jumpers XS13 and XS14
AD843, AD845, OPA132, OPA134	
AD817, AD847, LT1363	
OPA627, OPA671	

The signal from the output of the subtractive filter is the output signal of the DAC; it is fed to external devices through a T-shaped RC filter, which protects the OA circuit from high-frequency interference from the outside.

The analog circuits of each channel are powered from bipolar sequential stabilizers based on Mitsubishi M5230 microcircuits. These stabilizers are distinguished by low noise level, rather high speed, inherent linearity and stabilization coefficient. Voltage stabilizers ± 15V (DA9, DA15, VT3 - VT6) for powering the op-amp are made using additional external transistors, since the current consumed by them exceeds the maximum value of 30mA for the M5230. Voltage stabilizers ± 5V for DAC chips (DA7, DA13) do not have external regulating transistors.

Structurally, the DAC is made on a 4-layer double-sided printed circuit board made of FR4 material 2mm thick and 180 x 100mm in size. This solution made it possible to make "ground" circuits in the form of solid polygons and thus both reduce the RF interference radiated into the surrounding space and increase the system's resistance to external interference.

The element base of the Lynx24 DAC is close to that of the Lynx20. In the digital part, SMD resistors and capacitors of standard size 0805 are used. Each microcircuit of the digital part has its own power filter based on a ferrite bead and a blocking capacitor. Such individual filter cells can significantly reduce the mutual influence of digital microcircuits and thereby reduce the likelihood of "induced" jitter. Electrolytic capacitors used to block the digital power supply and power the digital part of the DAC - Rubycon Black Gate PK or Sanyo OS-CON SA. It is advisable to use Black Gate capacitors in the generator supply filters and noise filter of the AD586 ION, since they have minimal "capacitive" noise compared to other types of electrolytic capacitors.

It is advisable to use blocking capacitors of the Black Gate FK or NX types in the power circuits of the analog part of the DAC and the op-amp, which are characterized not only by low "capacitive" noise, but also by a high degree of intrinsic linearity. Additionally, "analog" power supplies are blocked by Wima FKP2 foil polypropylene capacitors in the immediate vicinity of the microcircuit power pins.

The subtractive LPF uses 1206 SMD resistors and Wima FKP2 output foil polypropylene capacitors with an accuracy of 2.5%. This accuracy is quite sufficient for the implementation of a second-order low-pass filter.

When working with microcircuits of multi-bit parallel DACs, it should be borne in mind that even a slight overheating of their terminals during soldering can significantly and irreversibly deteriorate the linearity of the HP of these devices, so it is advisable to install the DAC in contact sockets. To ensure high reliability of contact with the microcircuit terminals, it is better to use AMP collet-type sockets

or Scott SA.

The regulating transistors of power stabilizers (VT3 ... VT6) should preferably be equipped with heat sinks that ensure the temperature of the instrument cases in the steady state is no more than 40 ... 50C. For transistors VT1 and VT2, heat sinks are not needed if the input voltages of the stabilizers do not exceed 8 ... 9V.

In the best case, it is desirable to use 7 independent stabilized sources to power the device:

1. + 8 ... 12V 200 ... 250mA (power supply of the CF and FPGA)
2. + 8 ... 12V 100 ... 130mA (power supply of the resynchronization register)
3. + 9 ... 15V 50mA (clock generator power supply)
4. + 20 ... 24V 100mA (power supply of the positive arm of the analog part of the left channel)
5. - 20 ... 24V 100mA (power supply of the negative side of the analog part of the left channel)
6. + 20 ... 24V 100mA (power supply of the positive arm of the analog part of the right channel)
7. - 20 ... 24V 100mA (power supply of the positive arm of the analog part of the right channel) The last 4 primary power supplies are connected together and form an "analog" ground at the connection point on the DAC board itself.

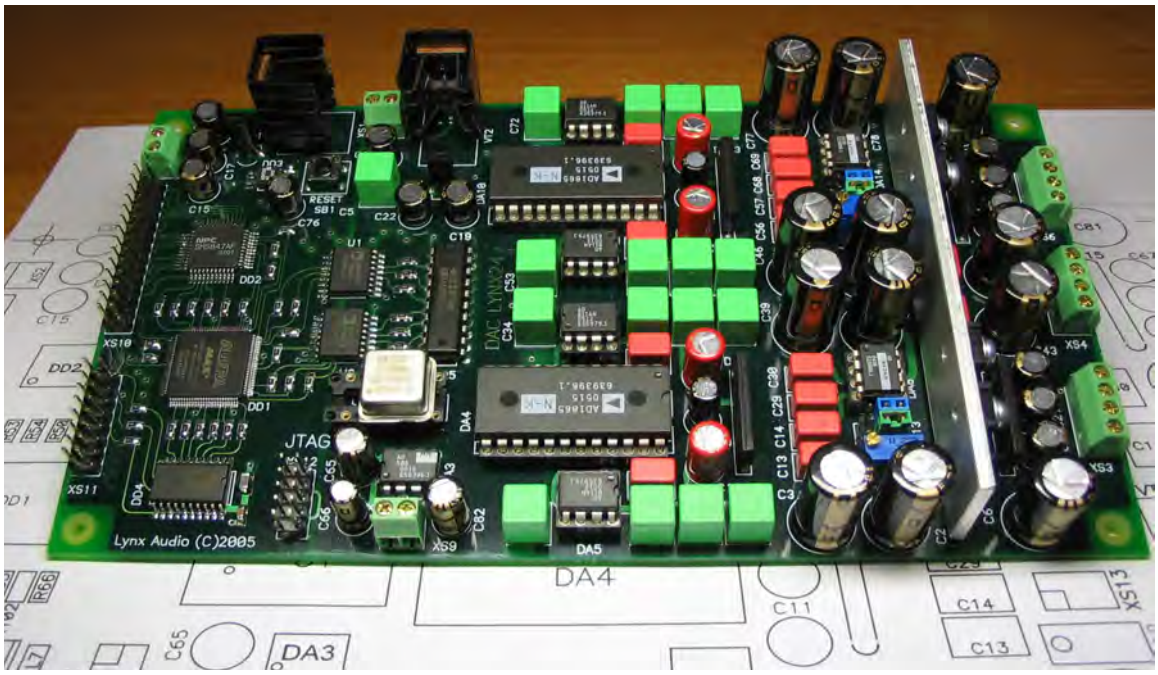
If the device is not required to obtain the limiting parameters, then the power system can be significantly simplified, for example, by using one primary source instead of item 1) and item 2), two or one bipolar source instead of item 4) ... item 7)

In this case, electrolytic capacitors of the Black Gate type are quite replaceable with similar denominations of the following types (as they deteriorate): Elna Silmic, Sanyo MV-AX, Panasonic FA, Elna RJH, and p-type field-effect transistors VT1 and VT2 - to bipolar pnp structures (source = emitter, drain = collector, gate = base) with a dissipation power of at least 800 mW, for example, 2SA1315.

Primary power supplies can also be unstabilized, since all the necessary local stabilizers are available on the device board, and their quality is quite sufficient to operate from unstabilized input voltages. In this case, rectifiers with capacities should be used

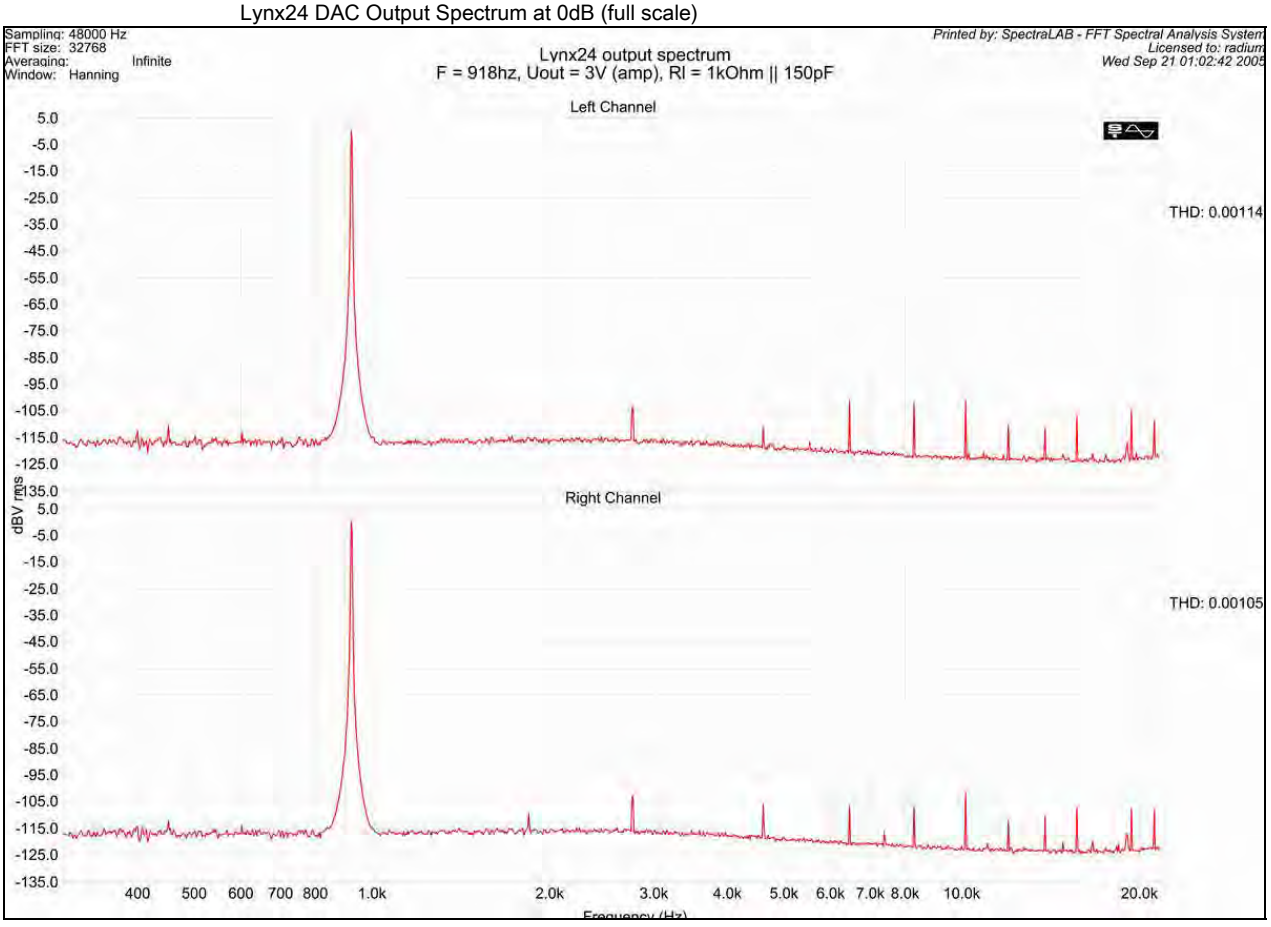
filters not less than 2000 ... 3000 mkF for "digital" power supplies, 5000 mkF for generator supply and 4000 mkF for "analog" power supplies.

The appearance of the mounted Lynx24 DAC module is shown in the figure:

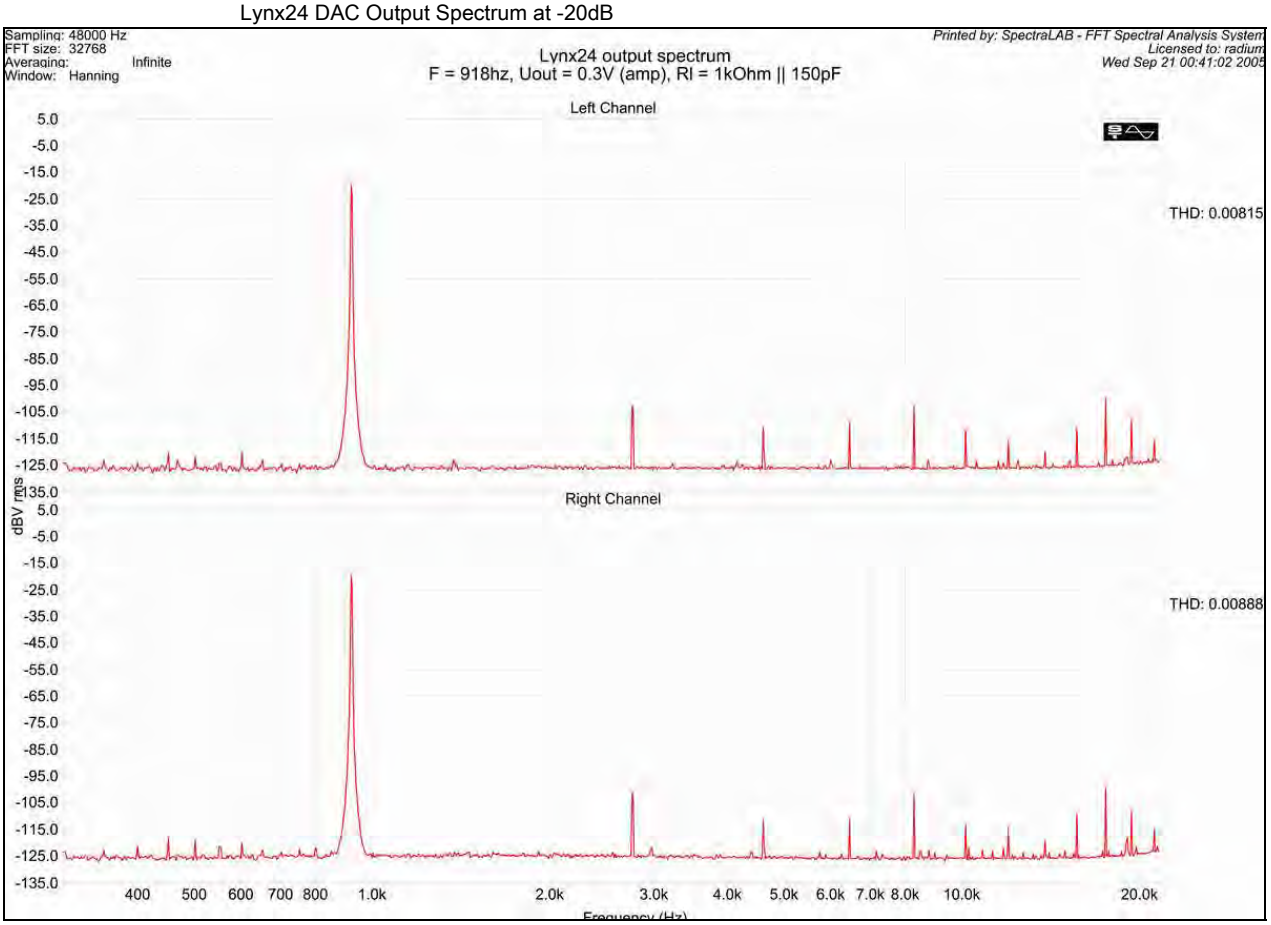


Spectra of the output signal for different levels (0dB, -20dB, -40dB and -60dB), taken using a PCI measuring ADC based on the AK5395 microcircuit intrinsic distortion -125dB, so that the resolution of the ADC at this frequency was -117dB) are given below. All spectrograms show that the realized dynamic range is not less than 98 dB, determined by the 16-bit signal at the device input.

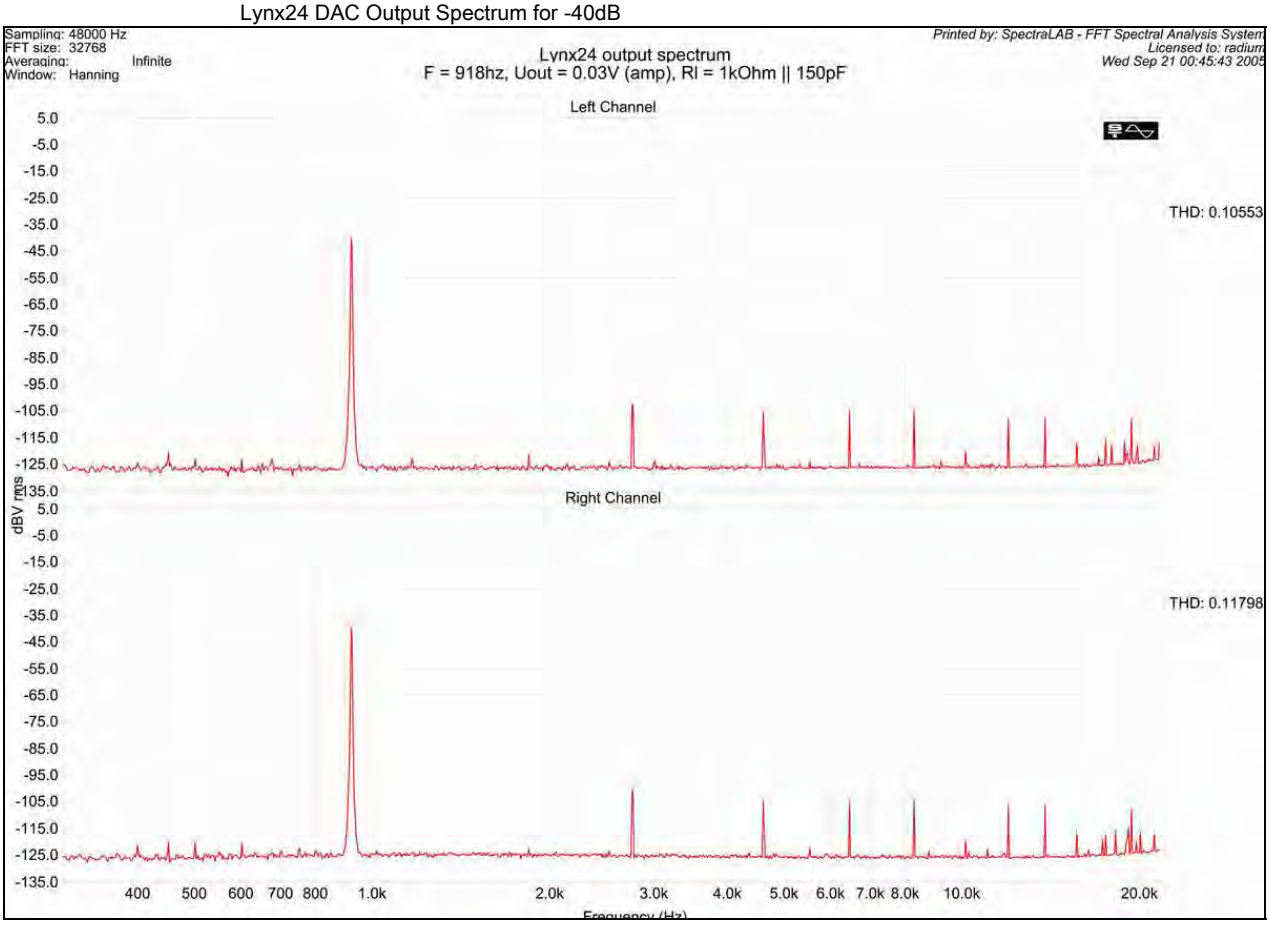
Lynx24 DAC Output Spectrum at 0dB (full scale)



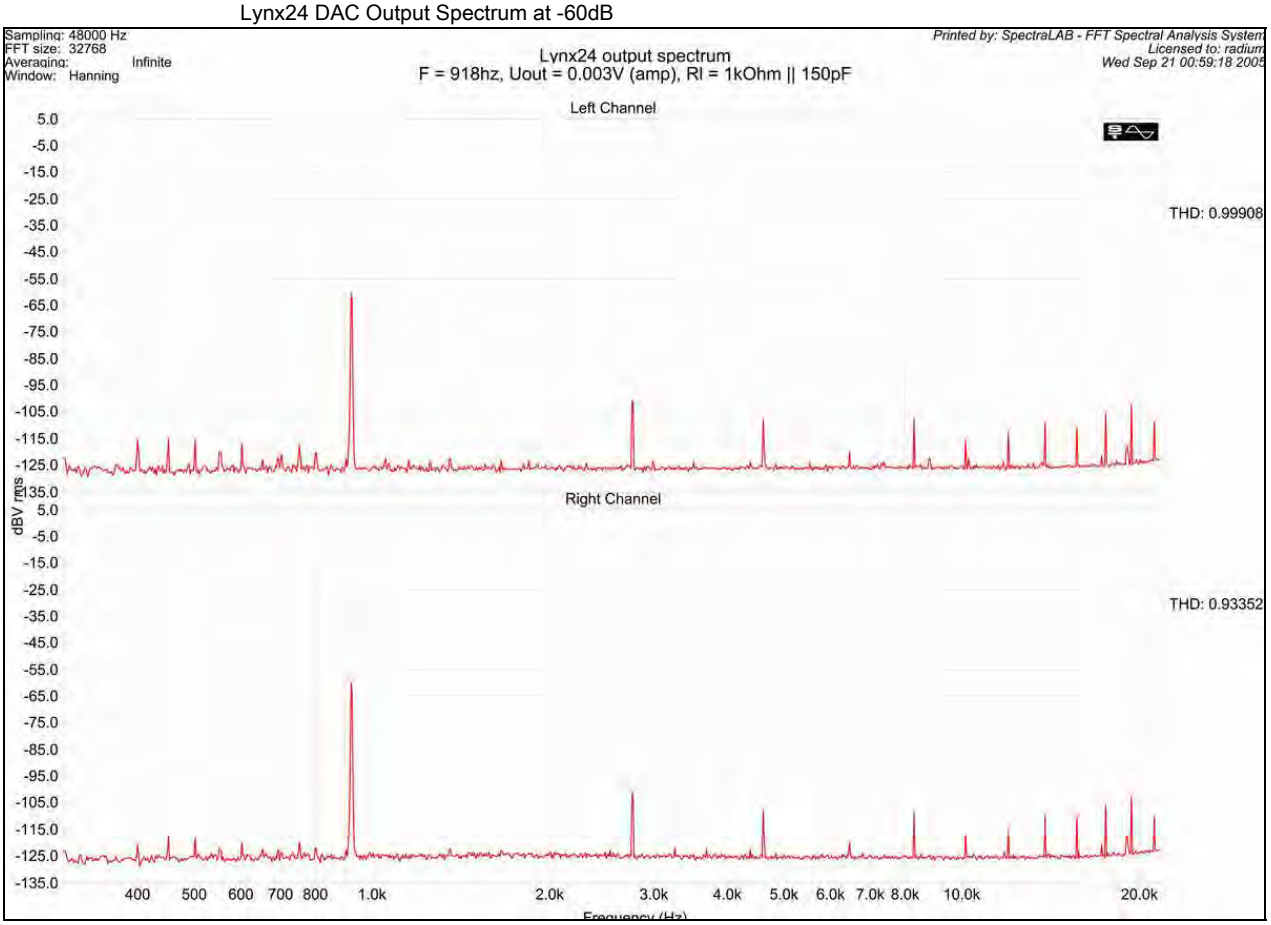
Lynx24 DAC Output Spectrum at -20dB



Lynx24 DAC Output Spectrum for -40dB



Lynx24 DAC Output Spectrum at -60dB



The author's copy of the Lynx24 DAC (DAC with "grade" -K) has the following technical characteristics (at a sampling rate of 44.1 kHz):

1) rated output voltage, corresponding to full scale conversion, V (RMS)	2.12
2) the relative level of noise at the output (at zero input signal), dB	below -110
3) the relative level of harmonic distortion and interference in the 45 kHz frequency band for the test 16-bit signal with a frequency of 918 Hz full scale, dB	- 98
5) Noise level in the 100 MHz band at analog outputs, dB	below -75
6) RMS jitter of the clock generator signal, ps	less than 6

The subjective sound of the Lynx24 DAC is very similar to that of the Lynx20 - neutral, transparent and clear, with excellent resolution and high detail. Almost completely there is no color, and as a result, the device well reveals the shortcomings of both the recordings themselves and other links of the sound reproduction path.

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St. Petersburg,
June - October 2005