

that the in-band noise due to jitter is

$$J = \left(\frac{\sigma_{\Delta t}}{T_s} \right)^2 \frac{8}{OSR}. \quad (9.19)$$

For a 1-bit modulator, therefore, an RZ DAC performs about 4 dB worse than an NRZ DAC for the same clock jitter. What happens in the multi-level case? In contrast to an NRZ DAC, where the heights of the transitions in the DAC waveform are a few levels, an RZ DAC's output goes all the way from 0 to $2 \cdot v[n]$ and back in every cycle. In the jitter scenario we have assumed (namely, white jitter), this puts an RZ DAC at a significant disadvantage with respect to jitter.

Further, while the RZ DAC is itself very linear, such a DAC increases the demands placed on the linearity of the loop-filter. This is due to the following. The loop-filter in a CT $\Delta\Sigma$ M processes the difference between the input and feedback *waveforms*. The RZ DAC results in a feedback waveform with twice the peak-to-peak amplitude when compared to its NRZ counterpart. As a result, the error waveform is much larger in magnitude in the former, even though the low-frequency content of both waveforms is the same. The loop-filter, therefore, has to be much more linear in the RZ case.

In [6], Adams proposes interleaving two RZ DACs to obtain the linearity of an RZ DAC while avoiding the jitter sensitivity of a single RZ DAC. This is often called the dual-RZ DAC.

9.3.5 Real Clock Sources and Phase Noise

So far in this section, we have gained an understanding of the mechanisms through which clock jitter degrades the performance of a CT $\Delta\Sigma$ M. Our analysis assumed white jitter – something that is not quite true in practice. It turns out that the output of a practical clock source can be expressed as

$$v_{clk} = \sin(2\pi f_s t + \phi(t)), \quad (9.20)$$

where $\phi(t)$ is small, and varies slowly when compared to $2\pi f_s t$. $\phi(t)$ results due to noise processes in the clock source, and perturbs the phase of the clock from its ideal trajectory of $2\pi f_s t$. It is, therefore, referred to as *phase noise*.

For small $\phi(t)$, (9.20) can be written as

$$v_{clk} \approx \sin(2\pi f_s t) + \phi(t) \cos(2\pi f_s t). \quad (9.21)$$

The power spectral density of v_{clk} is given by

$$P_{clk}(f) = \frac{1}{4}(\delta(f - f_s) + \delta(f + f_s)) + \frac{1}{4}(S_{\phi}(f - f_s) + S_{\phi}(f + f_s)), \quad (9.22)$$

where $S_{\phi}(f)$ represents the power spectral density of $\phi(t)$.

It is thus seen that in the presence of phase noise, the spectrum of the clock source can be thought of as consisting of the carrier, with power 1/2, and the spectrum of $\phi(t)$, which is translated around $\pm f_s$. It turns out that a large part of $\phi(t)$ varies slowly in relation to $2\pi f_s t$. $S_{\phi}(f)$ is thus lowpass in nature, and reduces with frequency, before flattening off. When v_{clk} is measured on a spectrum analyzer, the power at negative frequencies folds

atop that at positive frequencies, resulting in a spectrum similar to that in Figure 9.26. As the figure shows, $S_\phi(\Delta f)$ is the ratio of the power of v_{clk} in a 1 Hz bandwidth around $(f_s + \Delta f)$ to the power of v_{clk} ($=1/2$). In practice, therefore, $S_\phi(\Delta f)$ is specified (usually in dBc) in terms of the power spectral density of v_{clk} at a frequency Δf offset from f_s .

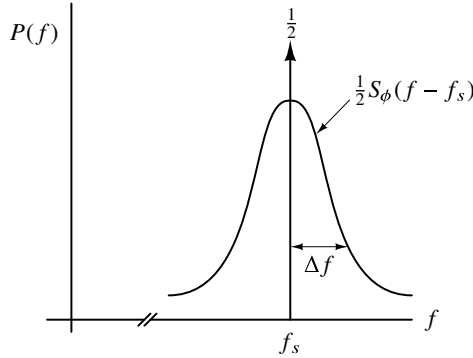


Figure 9.26 Power spectral density of v_{clk} as observed on a spectrum analyzer.

How does $\phi(t)$ manifest in the time domain? Without noise, $\phi(t) = 0$ and the rising edges of v_{clk} occur precisely at integer multiples of $1/f_s = T_s$. Phase noise causes a deviation in the zero-crossings of v_{clk} from their noise-free values. It is easy to see that $\phi(t)$ displaces the rising edges of v_{clk} by

$$\Delta t[n] = \frac{\phi[nT_s]}{2\pi} T_s. \quad (9.23)$$

We have earlier seen that the effect of clock jitter on a CT Δ ΣM with an NRZ feedback DAC can be modeled by adding an error sequence $e_j[n] = (v[n] - v[n-1])(\Delta t[n]/T_s)$ to the modulator output. Assuming an in-band input $u(t) = A \cos(2\pi f_{in}t)$ and that $|STF| \approx 1$, we see that

$$v[n] - v[n-1] \approx 2\pi A f_{in} T_s \sin[2\pi f_{in} n T_s] + (e[n] - e[n-1]) * h[n], \quad (9.24)$$

where $h[n]$ is the impulse response corresponding to the NTF. Using (9.23), we can express $e_j[n]$ as

$$e_j[n] = \underbrace{A(f_{in}/f_s)\phi[nT_s] \sin[2\pi f_{in} T_s n]}_{e_{j1}=\text{input signal component}} + \underbrace{[(e[n] - e[n-1]) * h[n]] \cdot (\phi[nT_s]/2\pi)}_{e_{j2}=\text{shaped quantization noise component}} \quad (9.25)$$

where e_{j1} is due to the interaction of jitter with the input signal, while e_{j2} models the mixing of shaped quantization noise with jitter. The spectrum of e_j is illustrated with the simplified sketch shown in Figure 9.27. Since multiplication in the time domain corresponds to convolution in the frequency domain, it follows that the spectral density of e_{j1} is that of $\phi[nT_s]$, scaled by $(A^2/2)(f_{in}/f_s)^2$ and translated around f_{in} . The input tone has an amplitude A . Therefore, the power spectral density of e_{j1} at a frequency Δf offset from f_{in} in relation to that of the input ($= A^2/2$) is simply $(f_{in}/f_s)^2 S_\phi(\Delta f)$. Hence, the effect of the close-in phase noise of the clock source is to broaden the line spectrum that we would expect for a sinusoidal input.

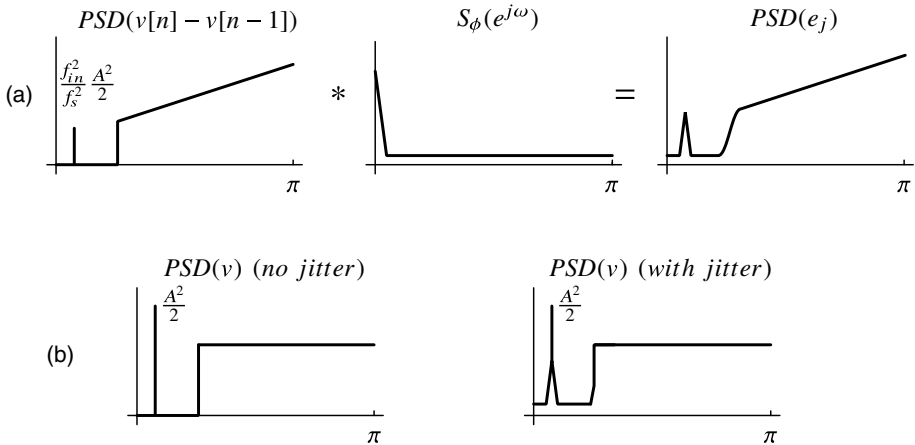


Figure 9.27 Simplified sketch illustrating the effect of clock phase noise on the PSD of a CTΔΣM.

The PSD of e_{j2} is the result of convolution of the spectra of the first difference of the shaped quantization noise and the phase-noise sequence. It is the in-band power of e_{j2} that we are interested in. From Figure 9.27(a), we see that the majority of the (white) in-band noise due to jitter is contributed by the far-out phase noise convolving with the shaped noise at high frequencies. Without jitter, $PSD(v)$ should have very little in-band noise and shaped out-of-band noise, as shown in Figure 9.27(b). With jitter, however, the in-band spectrum is corrupted by sidebands around the input tone, as well as an increased noise floor.

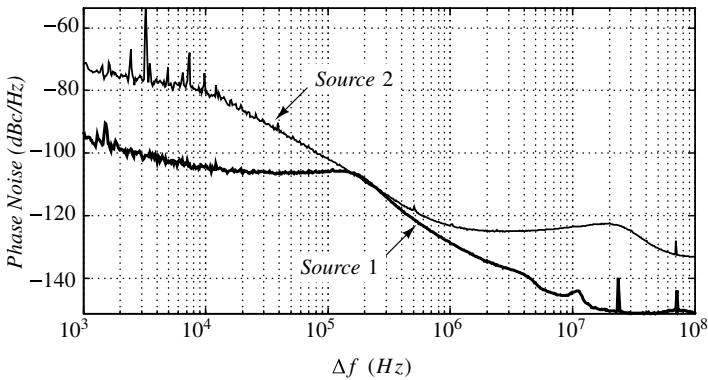


Figure 9.28 Measured phase noise of two 6 GHz clock sources as a function of frequency offset.

Figure 9.28 shows the measured phase noise plots of two 6 GHz clock sources as a function of frequency offset. It is apparent that the first source should result in a much smaller in-band noise due to jitter, since its phase noise at large frequency offsets is about 20 dB lower than that for source 2. Are any (or both) of these clock generators suitable for a single-bit CTΔΣM operating with OSR= 50, and targeting an SNDR of 75 dB?

Source-1 has a far-out phase noise spectral density of about -150 dBc/Hz. Over a 6 GHz bandwidth ($= f_s$), this corresponds to -52.2 dBc. The rms phase error is $\phi_{rms} = \sqrt{10^{-5.22}} = 2.45 \times 10^{-3}$ radians. In the time domain, this corresponds to an rms (white) jitter of $\phi_{rms}/(2\pi f_s) = 65 \times 10^{-15}$ s. Using (9.18) with $p = 0.8$, and assuming that the MSA is -3 dBFS, the peak signal-to-jitter-noise ratio is calculated to be 74 dB. To the jitter noise, we must also add thermal and quantization noise, which will degrade the in-band SNDR further. The conclusion is that both these clock sources are incapable of achieving the performance we seek from our 1-bit CT $\Delta\Sigma$ with an NRZ DAC. Architectural changes are necessary to reduce the susceptibility of this modulator to clock jitter. Several alternatives exist; we will examine some of these in the next section.

9.4 Addressing Clock Jitter in Continuous-Time Delta-Sigma Modulators

From our discussion on the manifestation of jitter in RZ and NRZ DACs, it is apparent that the shape of the DAC pulse has a significant bearing on the jitter sensitivity of a CT $\Delta\Sigma$. One approach to mitigating the effect of jitter, therefore, is to choose the DAC pulse shape in a way that jittery clock edges have little or no effect on the low frequency content of the feedback DAC waveform. This, for example, can be accomplished by using an impulsive feedback DAC, as we show below. Figure 9.29(a) shows the outputs of a

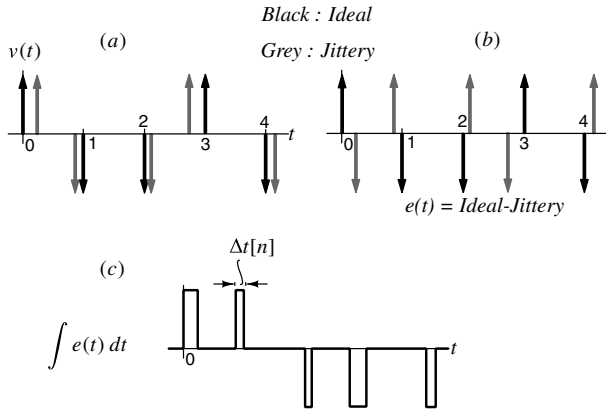


Figure 9.29 Effect of clock jitter on an impulse DAC waveform. (a) Outputs of a jitter-free and jittery DAC, (b) $e(t)$, and (c) integral of $e(t)$.

jitter-free and jittery impulsive 1-bit DAC. The difference between these two waveforms, which corresponds to the error caused by jitter, is shown in part(b) of the figure. The in-band components of $e(t)$ are responsible for the degradation of the modulator's SNR. To better understand the low-frequency power spectral density of $e(t)$, consider the integral of $e(t)$, shown in Figure 9.29(c). The area of each pulse is $v[n]\Delta t[n]$. As we concluded when we evaluated the jitter error of an NRZ DAC, the low-frequency spectral density of this waveform is the same as that of the sequence $v[n](\Delta t[n]/T_s)$. If jitter is assumed to be white, it follows that the power spectrum of the *integral* of $e(t)$ is also white. The PSD of $e(t)$ must hence be proportional to ω^2 , indicating that noise due to clock jitter is, to first order, shaped out of the signal band. An impulsive DAC is, therefore, less susceptible