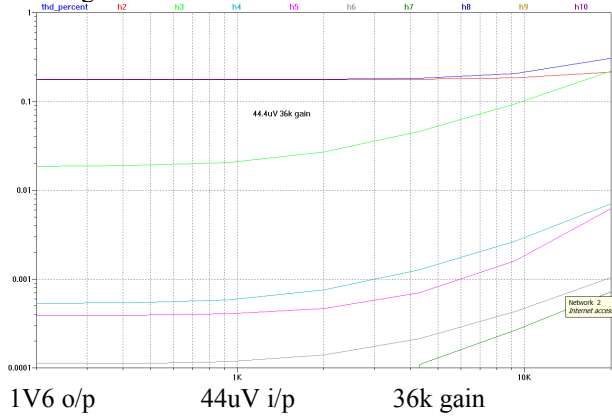


Adjust R17 for output DC offset less than 1mV in all these THD investigations

Investigate 2nd & 3rd with low LG in CE50d

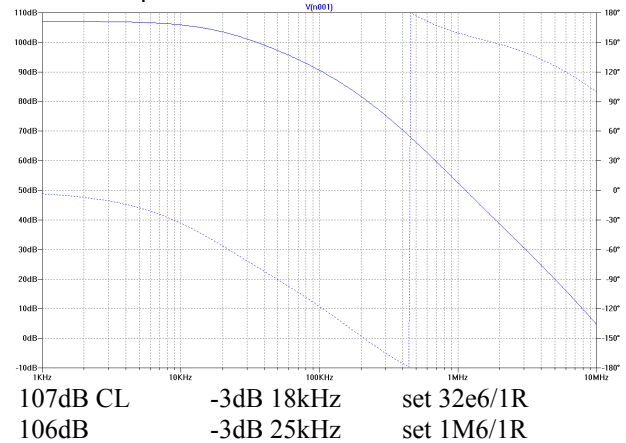
C3/4/5/6/1/7 set to 0p1



1V6 o/p

44uV i/p

36k gain



107dB CL
106dB

-3dB 18kHz
-3dB 25kHz

set 32e6/1R
set 1M6/1R

0dB LG -3dB 19.5kHz set 235k/1R CL 101.4dB

```

:SQUARES
V3 Vein 0 PULSE((-Ag) {Ag} {delaytime} 1n 1n {tperiod} {cycles})
.param prb 0
.tran 0 {simtime} 0 {stepsize}
.param freq 20k
.param cycles=9
.param delaycycles=0.5
.param simtime=delaycycles+cycles/freq
.param stepsize=simtime/10000
.param tperiod=1/freq
.param ton=tperiod/2

```

```

:THD
.param Ag 400e-6
.param RL 8
.param prb 0
.inc Analyzer_Controls.btx
.tran 0 {AnaTime} {SettleTime} {MaxStep/4}

```

```

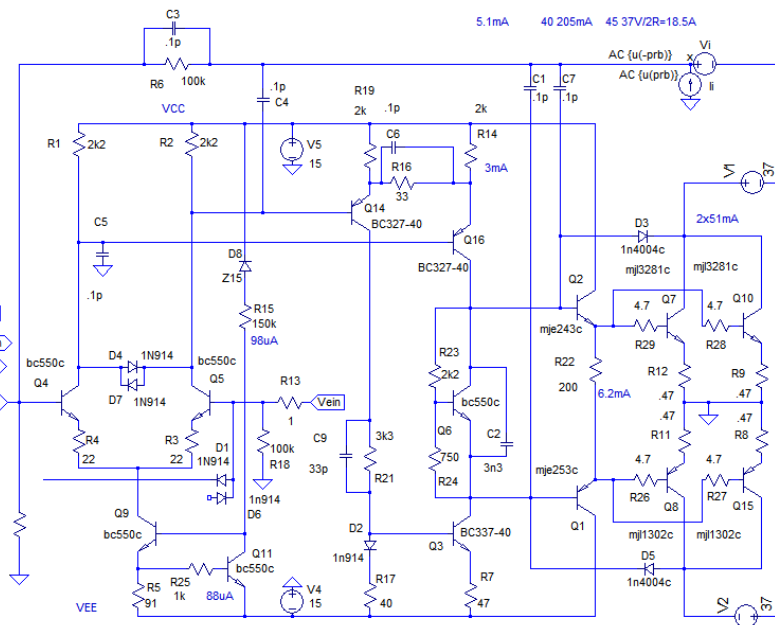
U1 THD meter
Analyzer_Controls.btx to adjust
settings & instructions
".inc Analyzer_Controls.btx" &
".tran 0 {AnaTime} {SettleTime} {MaxStep}"
into main schematic

```

```

.param Ag 1.7
.param Ag 1.831
.step param Ag LIST 0.1 0.3 1 1.82
.step param RL LIST 4 3 2.5 2
.options plotwinsize=0

```



```

CE50d.asc 23mar17r1
17.67x 24.9dB
750 2x51mA 0R47 xover
check load stab, O/L,
lib ..\vicardo.btx
lib ..\Cordell-Models.btx
lib 2sc5171_2sa1930.lib
lib 2sc5200_2sa1943.lib
lib mlylts.btx

```

```

.param Ag 400e-6
.param RL 8
.param prb 0
.tran 0 0.1m 0 0.1u
V3 Vein 0 SINE(0 {Ag} 2e4)
:LOOP GAIN
.param RL 8
.step param prb list -1 1
.ac dec 30 10k 100Meg
V3 Vein 0 AC 0

```

```

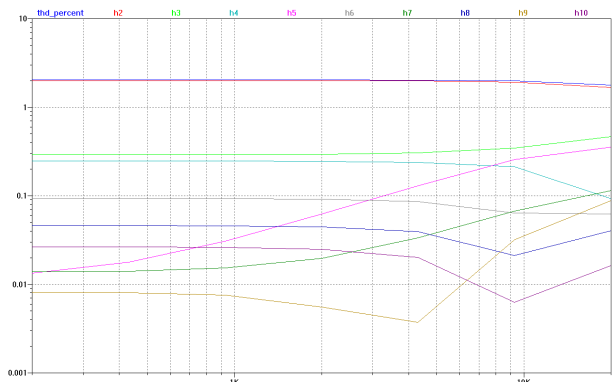
.param prb 0
.param RL 8
V3 Vein 0 0
.op

```

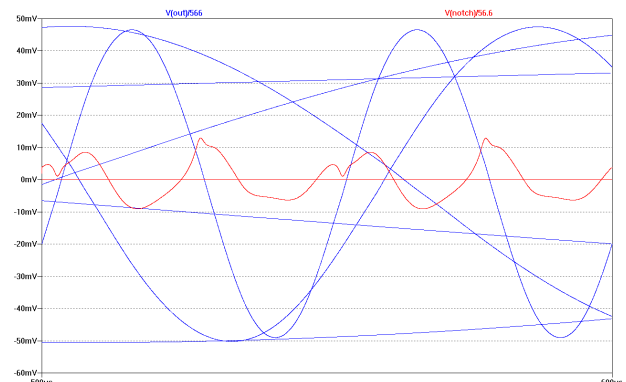
```

:CLOSED LOOP
.param RL 8
.param prb 0
V3 Vein 0 AC 1
.ac oct 24 1k 100e5

```

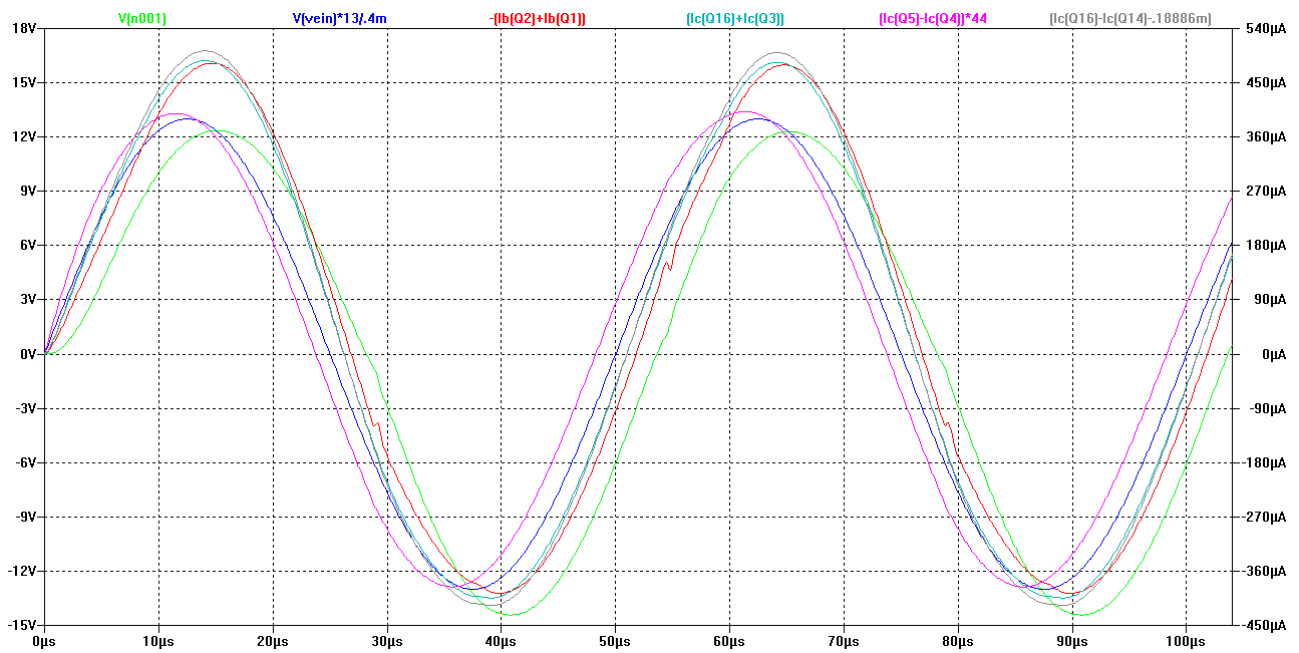
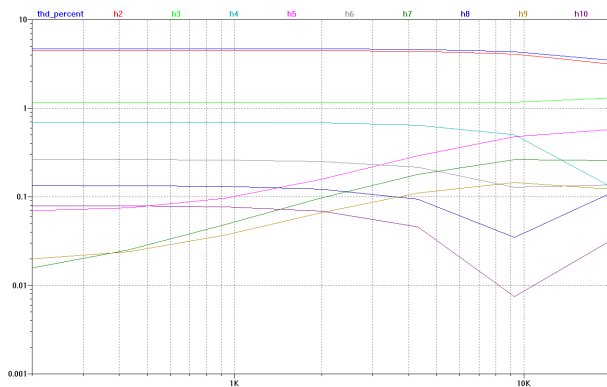
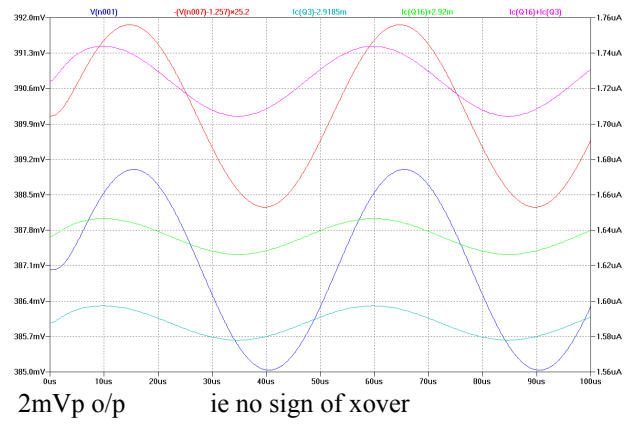
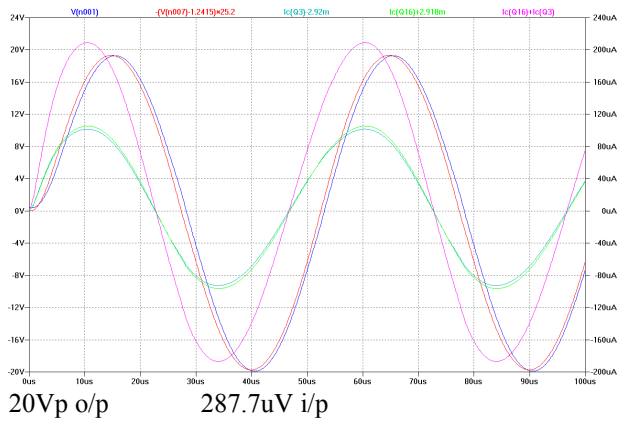


97dB gain (set 100dB 100k/1R) -3dB 75kHz

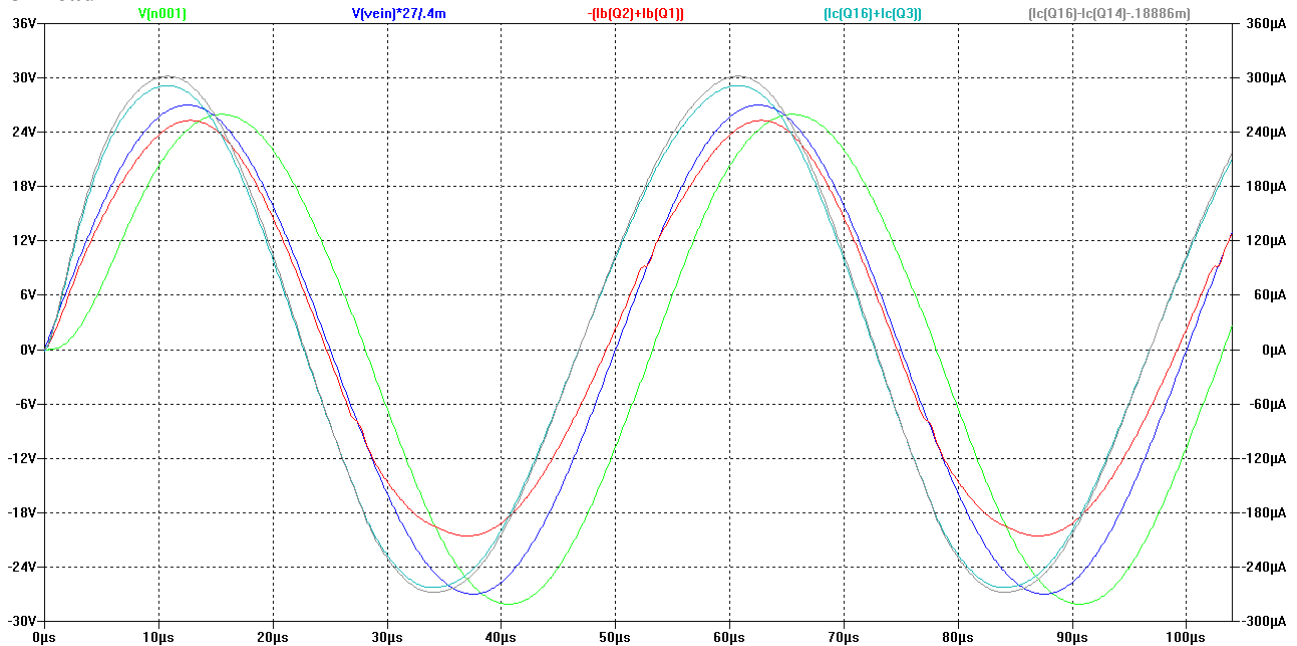


V(out) 28Vp at 10% THD

400uV i/p



Output wonky 2nd but **other way!**
6dB FB trying to correct O/P stage 2nd?

8R load

Why is $I_{b1/2}$ so much smaller than $I_{c16/3}$ VAS current compared to 2R case?

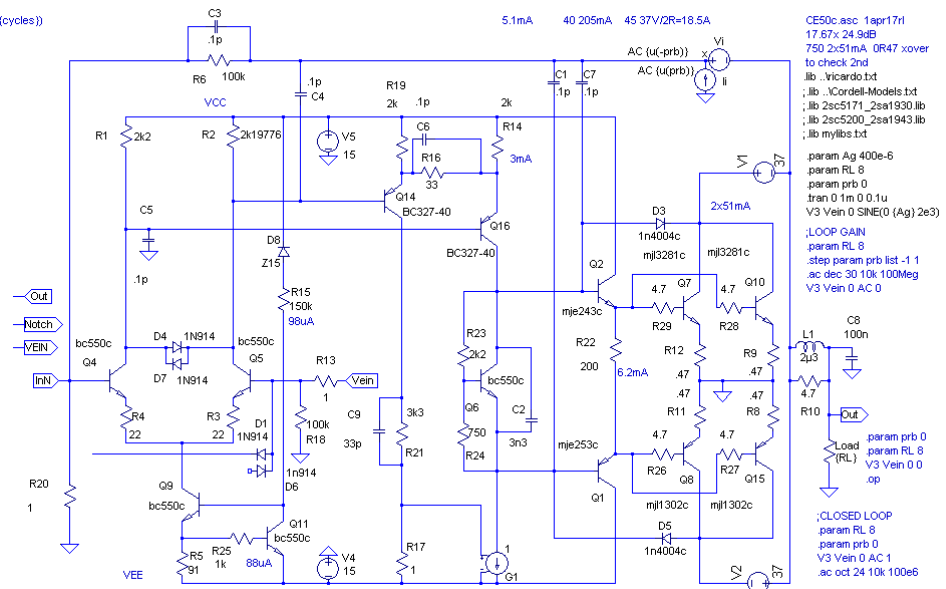
CE50c.asc & CE50c.plt started to investigate further

- Gain 100k/1R and 235k/1R
- use 2kHz instead of 20kHz
- D2/Q3 current mirror replaced by G1 transconductance (little/no dif. in THD)
- Offset tweaked with R2 on LTP

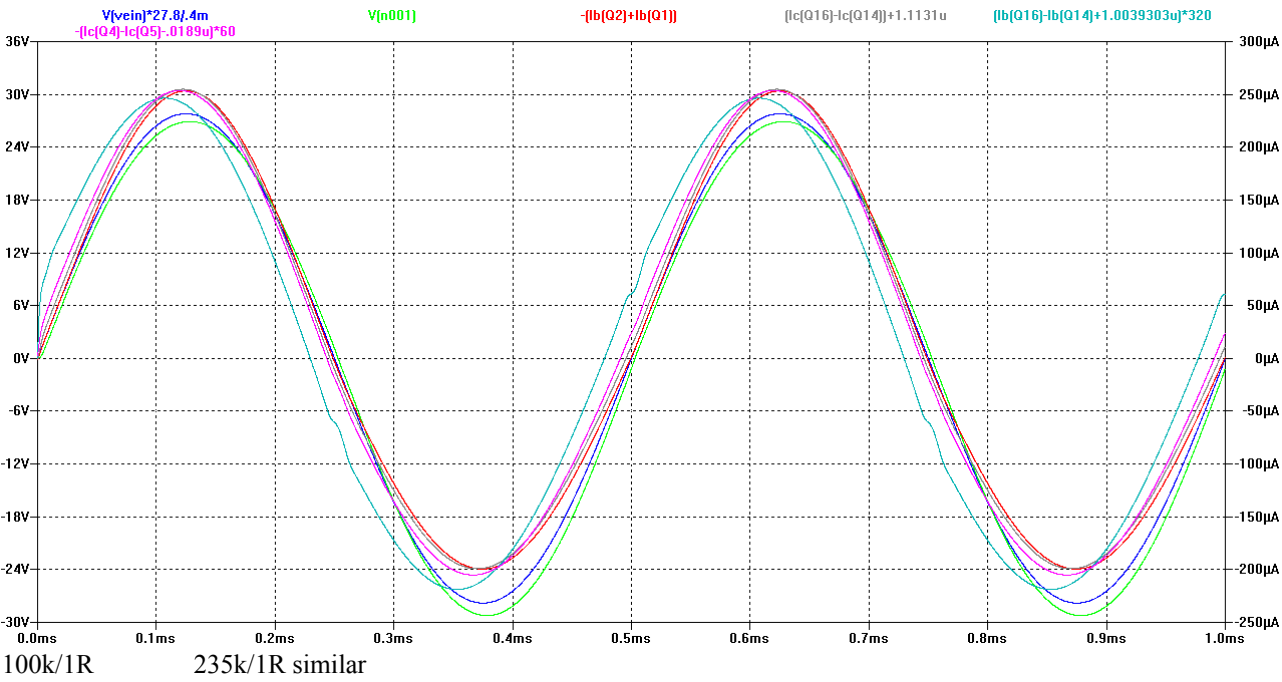
```
;SQUARES
V3 Vein 0 PULSE(-.Ag) (Ag) (delaytime) 1n 1n (ton) (tperiod) (cycles))
param prb 0
tran 0 (simtime) 0 (stepsize)
param freq 20k
param cycles=9
param delaycycles=0.5
param simtime=(delaycycles+cycles)/freq
param delaytime=delaycycles/freq
param stepsize=simtime/t0000
param tperiod=1/freq
param ton=tperiod/2
```

```
;THD
param Ag 1.6
param RL 8
param prb 0
inc Analyzer_Controls.tbt
tran 0 (AnaTime) (SettleTime) (MaxStep/4)
```

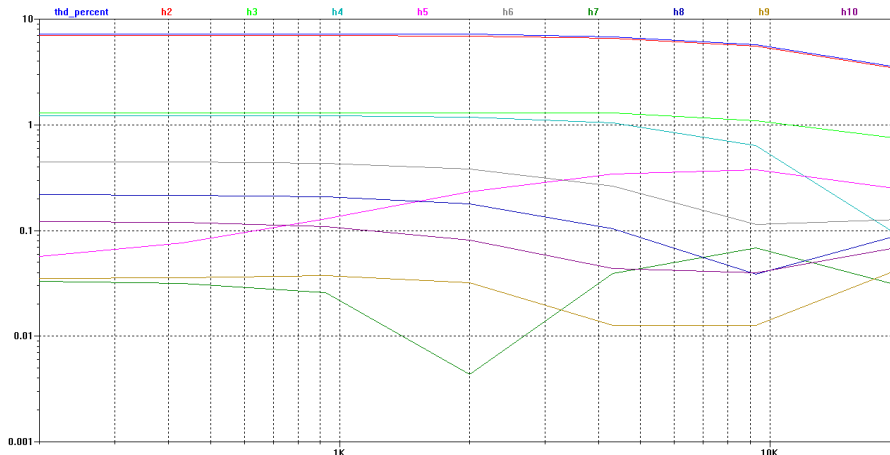
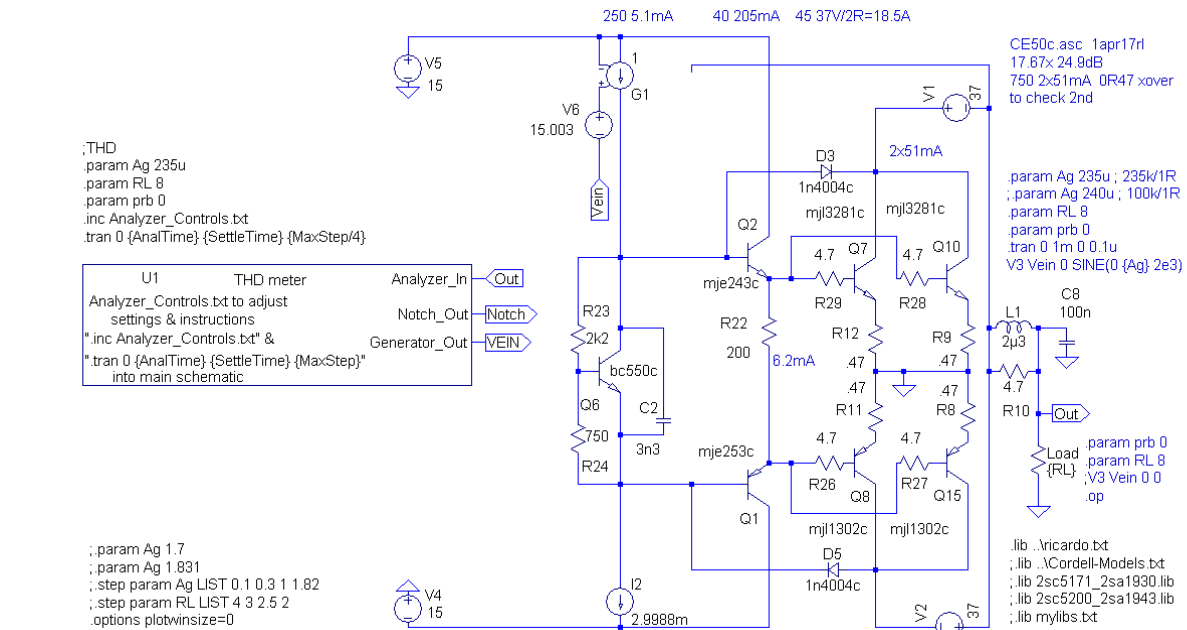
```
;param Ag 1.7
;param Ag 1.831
;step param Ag LIST 0.1 0.3 1 1.82
;step param RL LIST 4 3 2.5 2
options plotwinsize=0
```



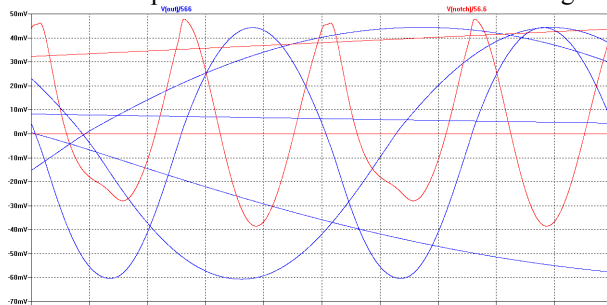
- Generally similar results to 20kHz
- from $I_{c4/5}$ i/p LTP output to $I_{b14/15}$ loses 5.33x (-14.5dB) current ie explains big improvement of CE50f with current loads on LTP i/p
- similar results at 100k/1R gain as well as 235k/1R gain



check out current driven O/P

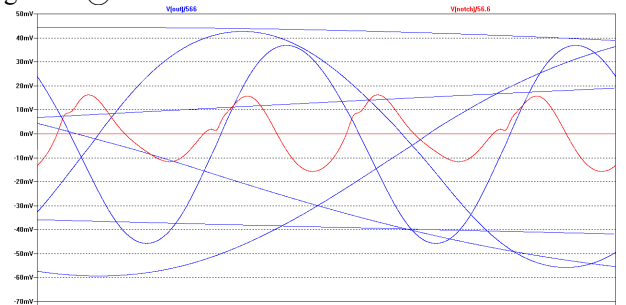


similar THD profile to CE50d & CE50f ... including dropping THD @ 20kHz in earlier versions



Vout @ 10% level

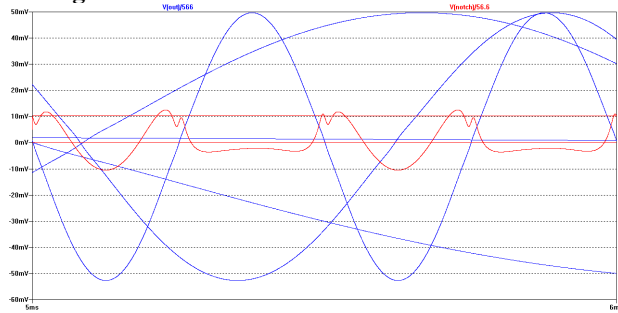
2kHz 7.2%



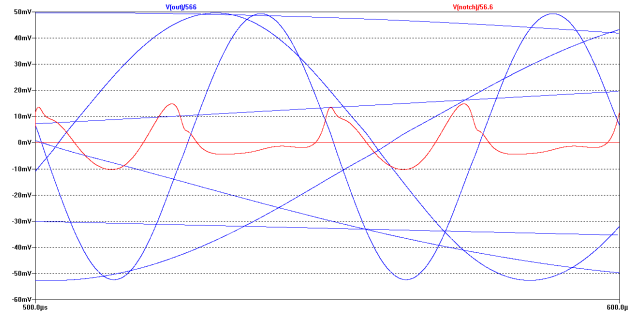
20kHz 3.5%

- 'rectified' residual at LF characteristic of 'change of hfe slope' THD
- higher orders low
- Q1/2 base at very high Z .. about 200k @ 2kHz
- ie using 1M resistor from o/p to Q1 base for offset (instead of twiddling I2) drops Ib Q1/2 & level by 2dB (80%)
- lower THD20k cos wonky Cob of outputs cancel? CE50d has 220p caps
- V&K output allows FB around whole Class B stage instead of individual halves for EF

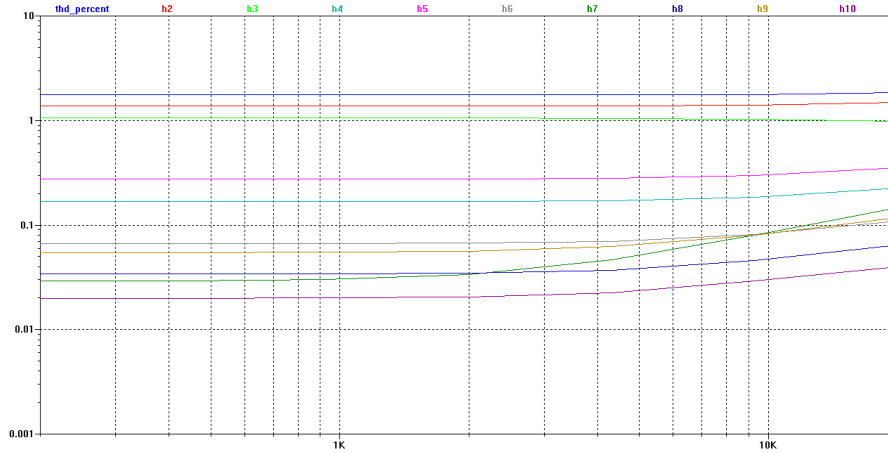
Voltage drive



2kHz 1.8%



20kHz 1.85%

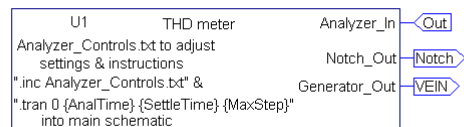


2 x 58mA Iq

```

;THD
param Ag 1.12
param RL 8
param prb 0
inc Analyzer_Controls.txt
tran 0 {AnalTime} {SettleTime} {MaxStep/4}

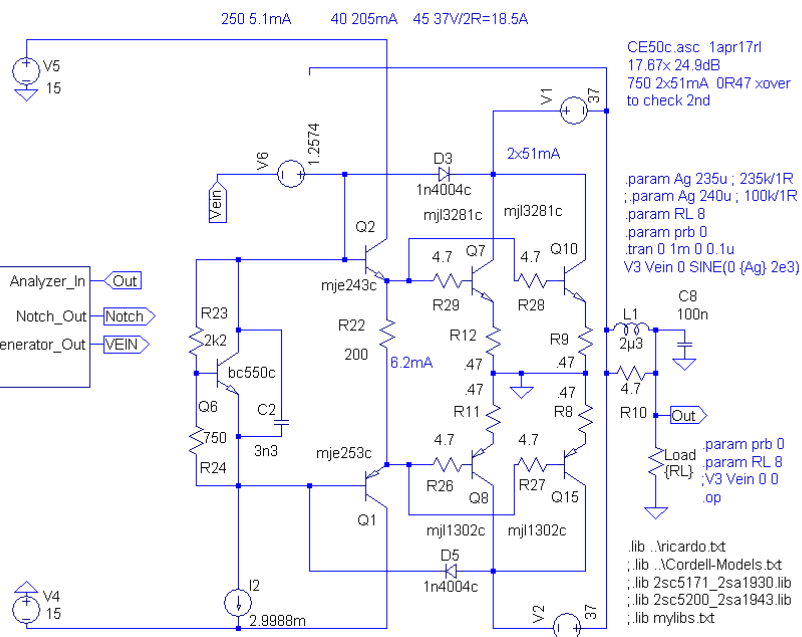
```



```

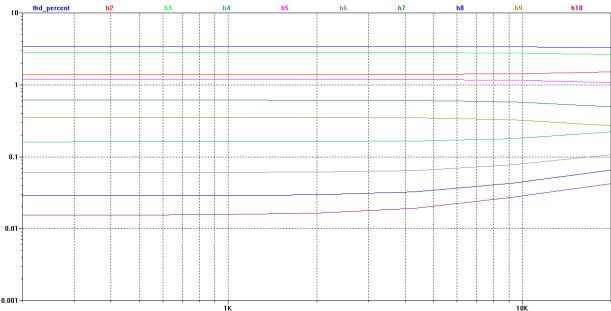
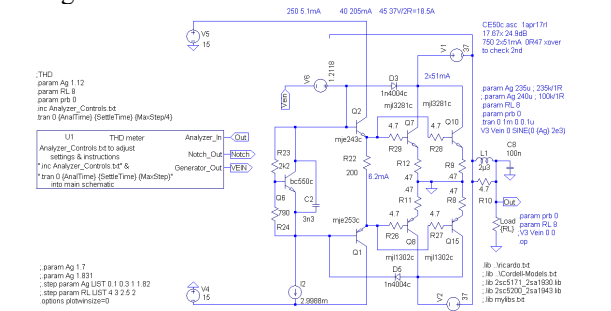
;param Ag 1.7
;param Ag 1.831
;step param Ag LIST 0.1 0.3 1 1.82
;step param RL LIST 4 3 2.5 2
.options plotwinsize=0

```

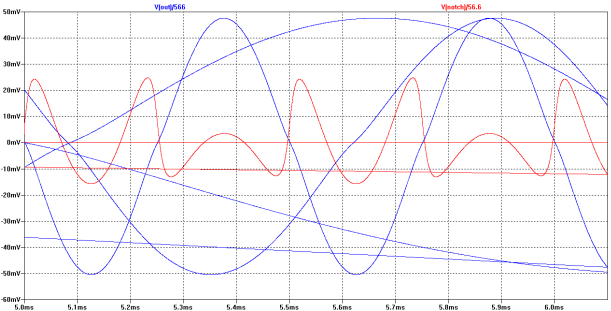


Try R24 790 **Iq 2x20.8mA** minimal bias

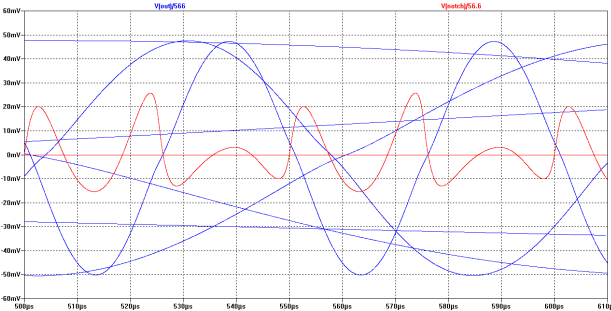
Voltage



3rd higher than 2nd

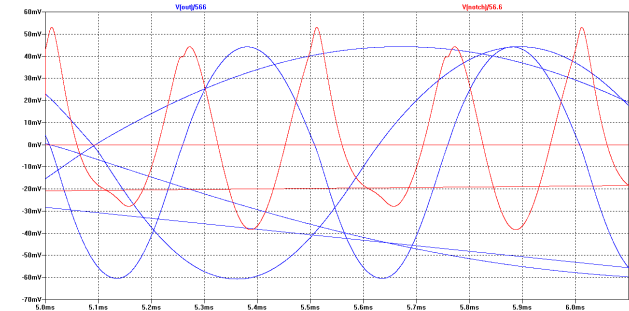
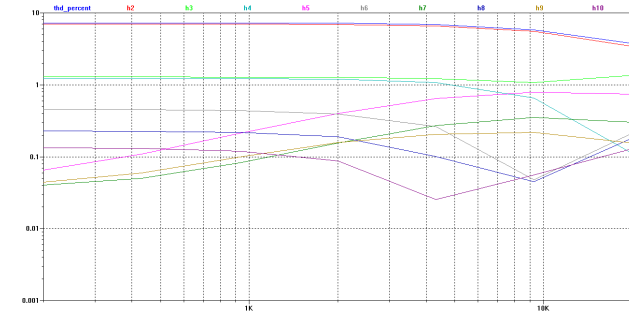
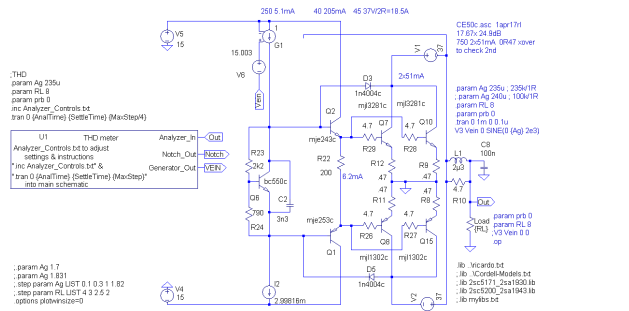


2kHz 3.4% visible xover

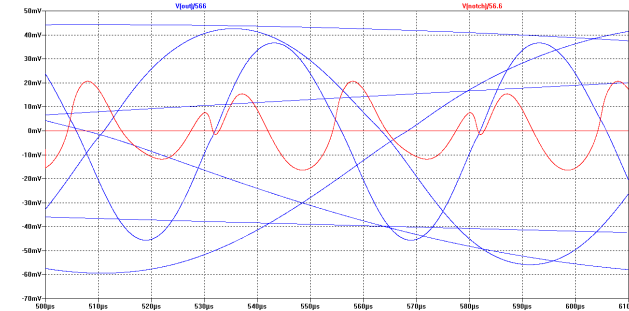


20kHz 3.3% little change from 2kHz

Current



7.2% visible 2nd



3.8%

History

1may Sent to diyaudio & D Zan.
28apr17 edited from VandK.doc.