Yongzhuo version Shenzhen Yongfukang Technology Co., Ltd.

SHENZHENSHI YONGFUKANG TECHNOLOGY CO.,LTD

CS8673E

With spread spectrum function, low no-load current, fixed 24 times gain, filter-free, 2X40W stereo, 80W mono Class D audio amplifier

summary

CS8673E is a 2x40W stereo; when used in mono, it can output up to 80W high-efficiency Class D audio power amplifier circuit. Advanced EMI suppression technology allows the use of cheap ferrite bead filters at the output port to meet EMC requirements. The CS8673E audio power amplifier is designed for systems that need to output high-quality audio power. It uses surface mount technology and only A small number of peripheral components are required to enable the system to have high-quality audio output power.

CS8673E has built-in overcurrent protection, short circuit protection and overheating protection, which effectively protects the chip from damage under abnormal working conditions. The CS8673E can drive speakers with loads as low as 40 and can provide up to 80W of continuous power; the CS8673E has an efficiency of up to 92%, eliminating the need for additional heat sinks when playing music.

CS8673E provides a small ESOP16 package for customers to choose, which can save customers considerable PCB area. Its rated operating temperature range is - 40°C to 85°C.

describe

• Output power@single channel

PO at 10% THD+N, VDD = 18V@RL = 4 Ω 47W
PO at 10% THD+N, VDD = 21V@RL = 4 Ω 64W
PO at 10% THD+N, VDD = 24V@RL = 4Ω 82W

• Output power@stereo

PO at 10% THD+N, VDD = 16V@RL = 4 Ω 2X33W
PO at 10% THD+N, VDD = 21V@RL = 8 Ω 2X33W
PO at 10% THD+N, VDD = 24V@RL = 8Ω 2X42W

- Large power supply voltage range 5V~26V
- Efficiency up to 92%, no heat sink required
- Fixed 24x gain, integrated 15K input resistor, 360K feedback resistor
- Spread spectrum function
- Audio system with filter network, standby current less than 20mA
- Filter-free function
- Output pins facilitate wiring layout
- Good short circuit protection and temperature protection with automatic recovery function
- Good distortion and anti-pop function
- Differential input

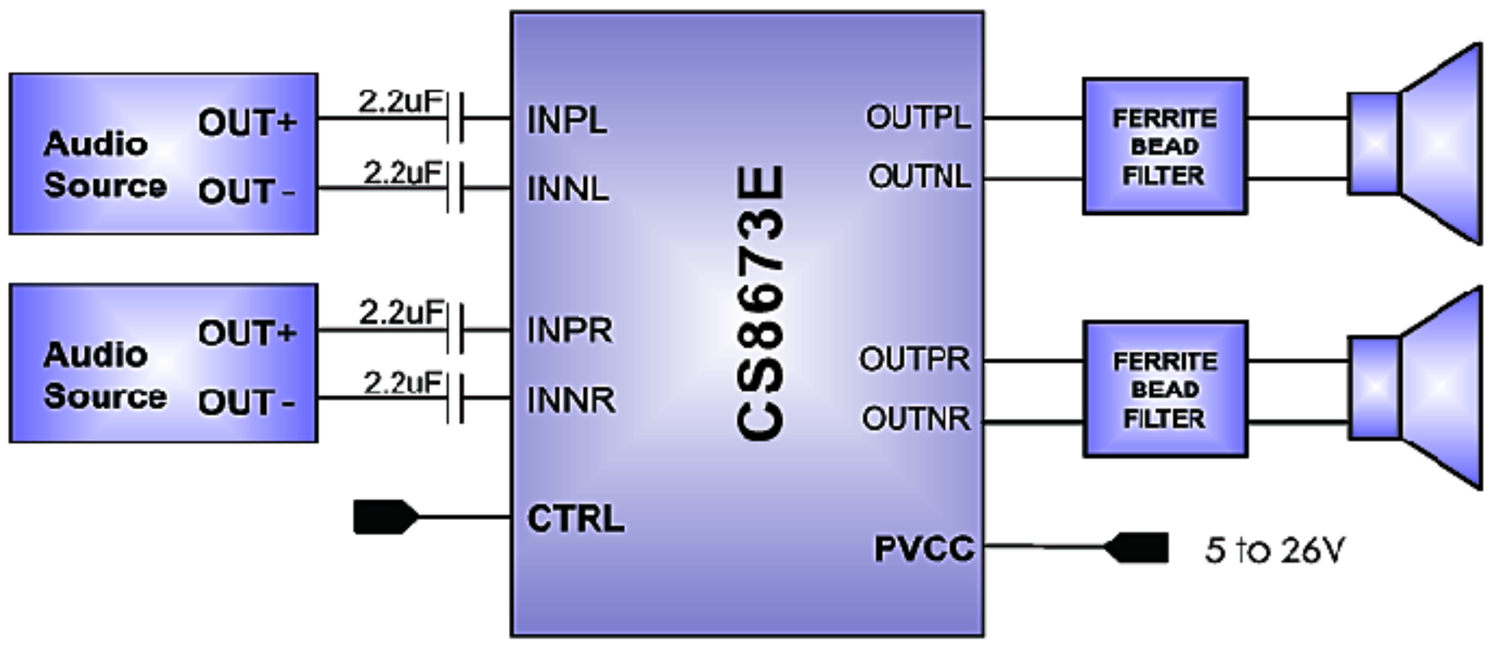
encapsulation

- ESOP16

application:

- LCD TV
- Home audio system

Typical application diagram



TEL:0755-82863877 13242913995 E-MAIL:panxia168@126.com http://www.szczkjgs.com

Typical application diagram

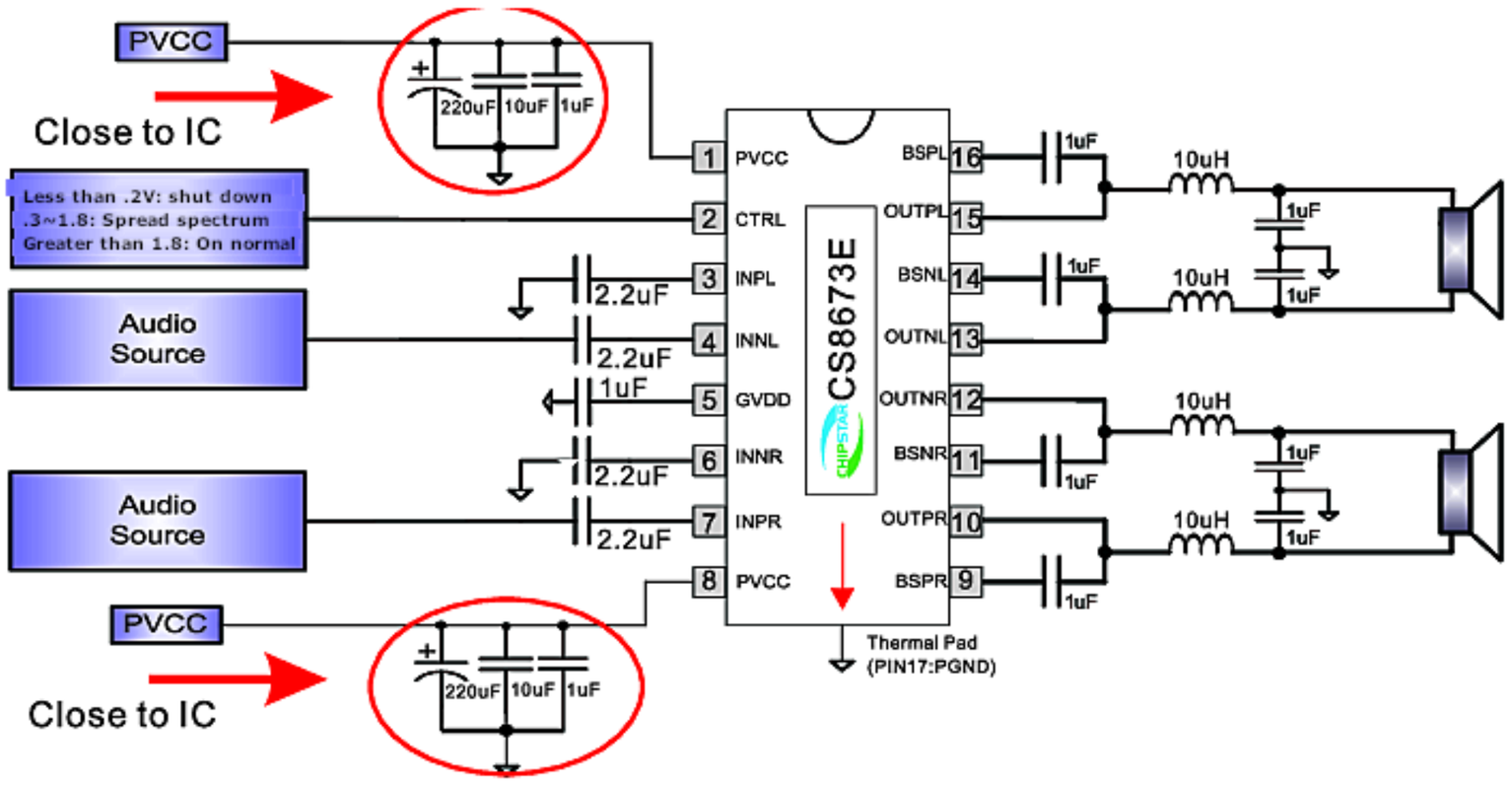


Figure 1 Typical application diagram of single-ended input stereo output

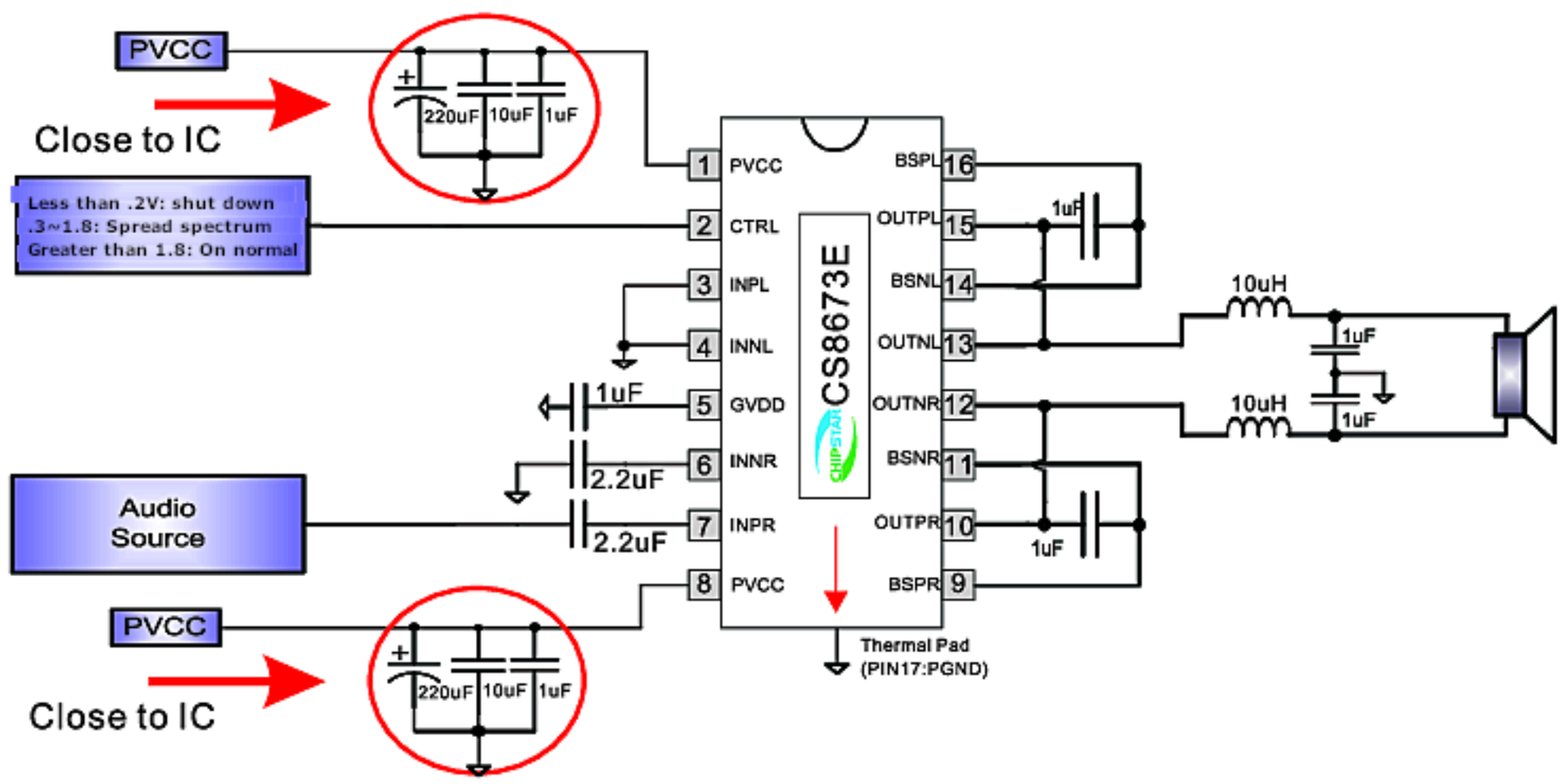


Figure 2 Single-ended input, PBTL output mono typical application diagram

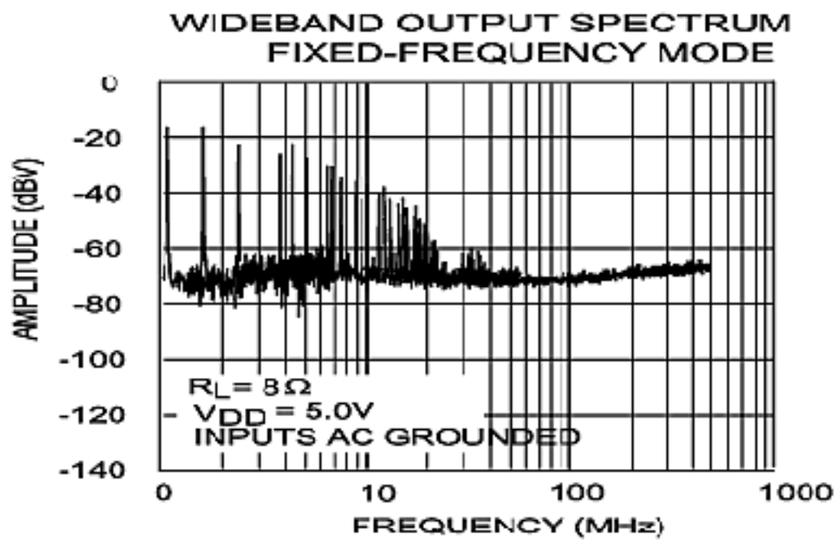
Application Notes

Standby mode and spread spectrum mode settings

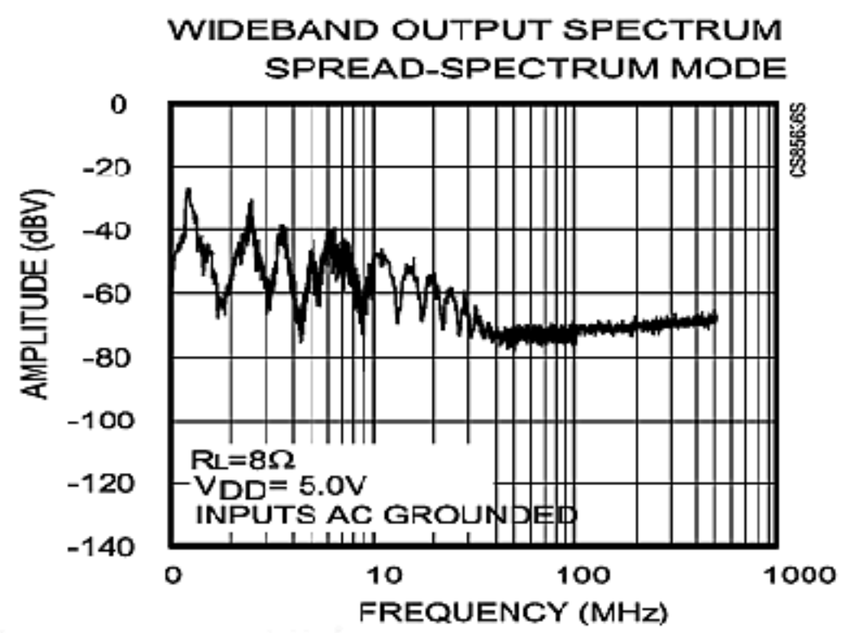
When the CTRL pin voltage is less than 0.2V, CS8673E enters standby mode. During normal operation, CTRL cannot be left unconnected, because this will cause the op amp to enter an unpredictable state. For optimal shutdown performance, place the op eration in standby mode before turning off power. When the CTRL pin voltage is between 0.3~1.8V, CS8673E operates normally and enters spread spectrum mode. When the CTRL pin voltage is above 1.8V, CS8673E operates normally and turns off the spread spectrum mode.

CS8673E has a unique spread spectrum modulation mode. In this mode, the spectrum components are spread over a wide frequency band, which can effectively reduce EMI (see the fixed frequency spectrum energy diagram and spread spectrum technology spectrum energy diagram for details). It is proprietary Technology ensures that switching frequency changes from cycle to cycle do not degrade audio reconstruction performance or efficiency. The switching frequency varies randomly within a range of ±30K near the center frequency of 300K. The modulation method remains unchanged, but the frequency of the sawtooth wave changes with the period. In this way, the energy is dispersed to the entire frequency band that increases with the frequency, instead of concentrating a large amount of spectrum energy at the co-frequency of the switching frequency, in a frequency band of up to several MHZ. , EMI is equivalent to white noise at broadband frequencies (see EMI spectrum diagram).

C38673E fixed frequency spectrum energy diagram



CS8673E spread spectrum technology spectrum energy diagram



Short circuit protection and automatic recovery

CS8673E protects the overcurrent state caused by short circuit at the output terminal. When a short circuit occurs, CS8673E immediately turns off the output. When the short circuit fault at the output terminal is eliminated, CS8673E only needs to wait for 110ms to recover itself. temperature

protection

The temperature protection of CS8673E prevents device damage when the temperature exceeds 150°C. At this temperature point, there is an upper and lower allowable range of ±15°C between devices. Once the temperature exceeds the set temperature point, the device enters a shutdown state with no output. When the temperature drops by 20°C, the temperature protection will be eliminated and the device will begin to work normally.

Single-ended input mode of CS8673E

The analog input of the CS8673E device is a standard differential input interface. In system design, it is recommended to use differential input mode to connect the audio output of the main chip. Using differential input mode can make the control of POP sound relatively simple and the signal anti-interference ability is strong. The comparison between differential input mode and single-ended input mode is shown in the following table:

Differential and single-ended input mode comparison table

	Differential input mode	Single-ended input mode
Anti-noise interference ability	Differential input has strong common mode noise rejection performance	There is no suppression function, so more attention needs to be paid to PCB trace layout.
POP sound performance on startup/shutdown	The symmetry of the differential input ensures optimal on/off POP acoustic performance	Single-ended input requires careful design of the input network and control circuit to avoid POP sounds caused by unbalanced input.

Please note the following points when using single-ended input mode:

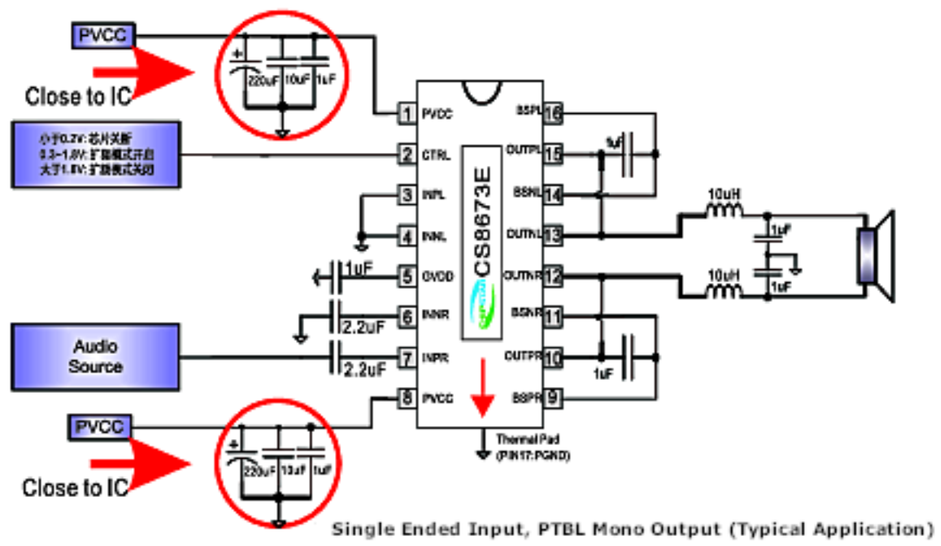
- When applying the single-ended input mode, you need to pay more attention to the routing of audio signals and the distribution of the ground plane, because the single-ended input mode does not have the ability to suppress the common mode interference signal in the system.

• Compared to differential signal input mode, single-ended input requires twice the input signal level to achieve the same output power.

• In single-ended input mode, attention must be paid to the impedance matching of the P/N pin circuit network, and try not to use complex filter networks in the input stage. Improper impedance network will cause POP sound when switching on and off.

PBTL function

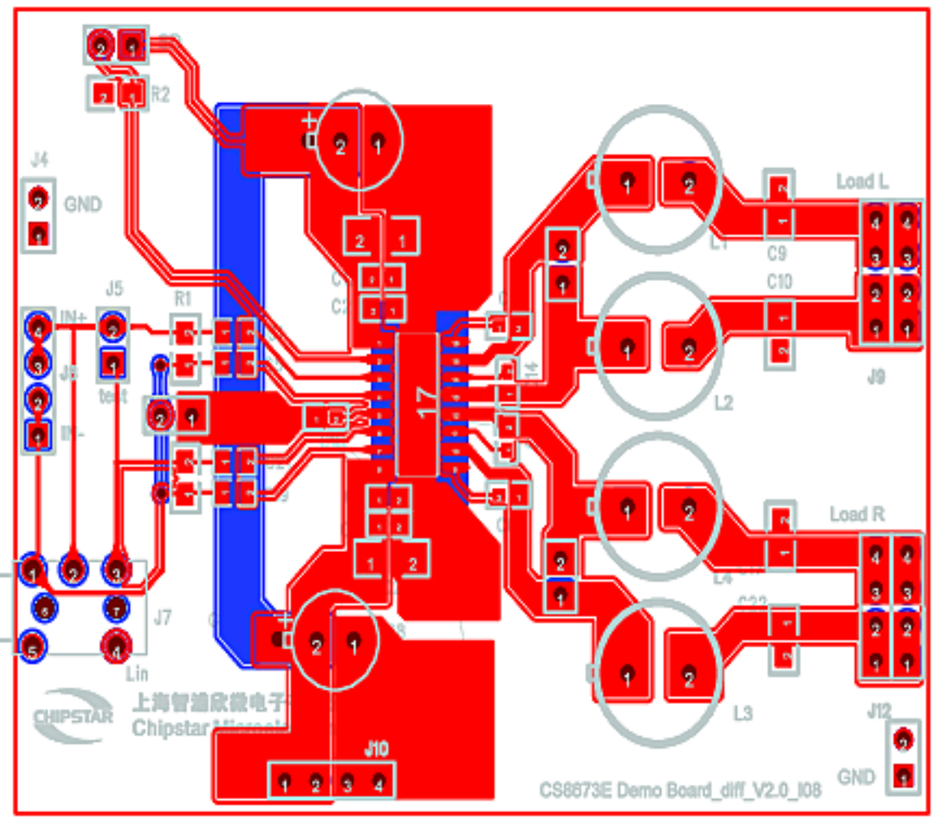
CS8673E has PBTL function. In the case of mono channel, CS8673E can drive a load as low as 4Ω. In the case of 24V power supply, CS8673E can provide more than 80W of contact power without a heat sink. In PBTL mode, You need to connect the INNL and INPL pins directly to ground without adding a coupling capacitor in front, as shown in the figure below:



Single Ended Input, PTBL Mono Output (Typical Application)

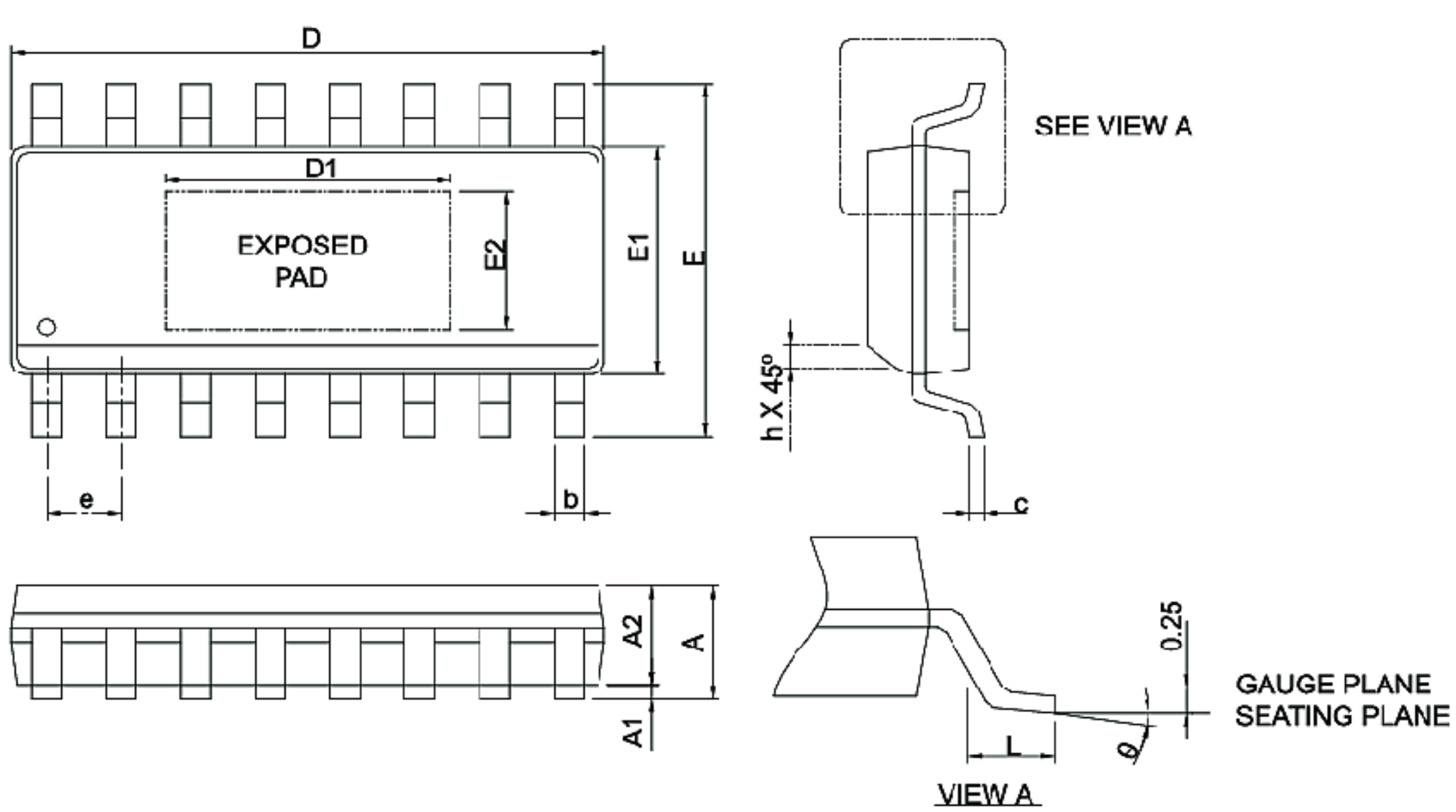
CS8673EPCB Notes:

The bottom heat sink of CS8673E must be connected to the ground of the chip, and the ground must be able to withstand a large enough current. The following is a layout diagram of a single-sided PCB.



Package information

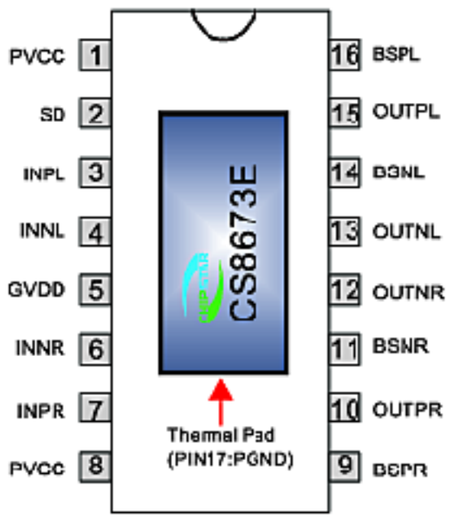
CS8673E ESOP16L



SYMBOL	ESOP16L			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.75		0.069
A1	0.00	0.15	0.000	0.006
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	9.80	10.00	0.386	0.394
D1	3.50	4.50	0.138	0.177
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
E2	2.00	3.00	0.079	0.118
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

Note : 1. Follow from JEDEC MS-012 BC.
2. Dimension "D" does not include mold flash, protrusions or gate burrs.
Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3. Dimension "E" does not include inter-lead flash or protrusions.
Inter-lead flash and protrusions shall not exceed 10 mil per side.

Pinout and definition



ESOP16L
(Top View)

serial number	illustrate	property	Function
1	PVCC	P	Power supply
2	CTRL	I	Standby logic; spread spectrum selection control terminal, TTL logic voltage allowed to AVCC
3	INPL	I	Left channel audio source input positive terminal
4	INNL	I	Left channel audio source input negative terminal
5	GVDD	P	High-side gate drive voltage
6	INNR	I	Right channel audio source input negative terminal
7	INPR	I	Right channel audio source input positive terminal
8	PVCC	P	Power supply
9	BSPR	I	Right channel positive output upper tube bootstrap
10	OUTPR	O	Right channel output positive terminal
11	BSNR	I	Right channel negative output upper tube bootstrap
12	OUTNR	O	Right channel output negative terminal
13	OUTNL	O	Left channel output negative terminal
14	BSNL	I	Left channel negative output upper tube bootstrap
15	OUTPL	O	Left channel output positive terminal
16	BSPL	I	Left channel positive output upper tube bootstrap
17	PGND	P	Power ground (heat sink)

Limit parameter table [1]

			unit
V_{CC}	power supply	PVCC	0.3Vto28V
V_I	Input pin voltage CTRL		0.3V to V_{CC}+0.3V
T_A	Operating temperature range		-40℃ to 85℃
T_J	Junction operating temperature range		-40℃to170℃
Tstg	storage temperature range		-65℃ to150℃

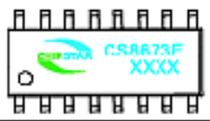
Recommended work environment

parameter	describe	numerical value	unit
V_{DD}	Supply voltage	5~26.0	V
T_A	ambient temperature range	-40~85	℃
Tj	Junction temperature range	-40~150	℃

Thermal effect information

parameter	describe	numerical value	unit
θ_{JA}	Package thermal resistance---chip to ambient thermal resistance	45	℃/W
θ_{JC}	Package thermal resistance---chip to package surface thermal resistance	10	℃/W

Ordering information

Product model	Package form	Device Identification	Packing size	Tape width	quantity
CS8673E	ESOP16L		Tube		50

ESD range

ESD range HBM (Human Body Electrostatic Mode) ---------- ±2KV

ESD range MM (machine electrostatic mode) ---------- ±200V

1. The above parameters are only the working limits of the device. It is not recommended that the working conditions of the device exceed these limits, otherwise it will affect the reliability and life of the device, or even cause permanent damage.

2. Where the CS8673E is placed on the PCB board, a heat dissipation design is required so that the heat sink at the bottom of the CS8673E is connected to the heat dissipation area of the PCB board and connected to the ground through a via hole.

Recommended working conditions

describe		Test conditions	minimum value	maximum value	unit
V_{CC}	power supply	PVCC	5	26.0	V
V_{IH}	Input high level	CTRL	2		V
V_{IL}	Input low level	CTRL		0.8	V
V_{OL}	Output high level	$R_{PULL-UP}$=100k,V_{CC}=15V		0.8	V
I_{IH}	High level input current	CTRL,V_I=2V,V_{CC}=15V		50	uA
I_{IL}	Low level input current	CTRL,V_I=0.8V,V_{CC}=15V		5	uA
OVP	Overvoltage protection			30.0	V

DC parameters TA=25°C, Vcc=12 V, RL = 80 (unless otherwise specified)

describe		Test conditions		minimum value	Typical value	maximum value	unit
$\|V_{OS}\|$	Output offset voltage	V_I=0V			1.5	15	mV
I_{CC}	Quiescent current	(CTRL=1V, no load, PVcc=12V			6.5	9	mA
$I_{CC(SD)}$	Standby current	CTRL=0.2V, no load, PVCc=12V			20	50	uA
$r_{DS(on)}$	Drain-source on-resistance	V_{CC} =12V,I_O=500mA, T_J =25°C	Top tube		80		mΩ
			Downtube		80		
t_{on}	Turn on time	CTRL=2V			100		ms
t_{OFF}	Off time	CTRL=0V			2		us
GVDD	Gate drive voltage	I_{GVDD} =100 mA		4.0	4.5	5.0	V

TA=25°C, Vcc = 16 V, RL = 80 (unless otherwise stated)

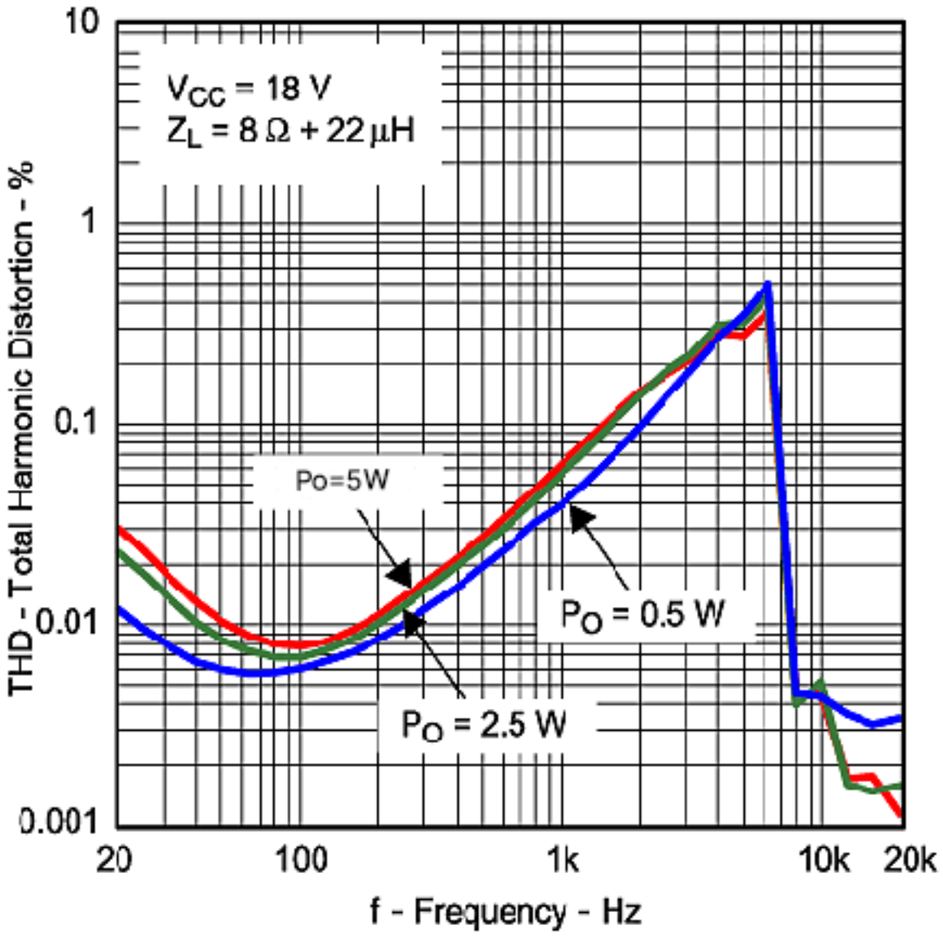
describe		Test conditions		minimum value	Typical value	maximum value	unit
$\|V_{OS}\|$	Output offset voltage	V_I=0V			1.5	15	mV
I_{CC}	Quiescent current	CTRL=1V, no load, PVcc=16V			10	15	mA
$I_{CC(SD)}$	Standby current	CTRL=0.2V, no load, PVCC=16V			50		uA
"DS(cn)	Drain-source on-resistance	V_{CC} =16V,I_O=500mA, T_J =25°C	Top tube		80		mΩ
			Downtube		80		
t_{on}	Turn on time	CTRL=2V			110		ms
t_{OFF}	Off time	CTRL=0V			2		us
GVDD	Gate drive voltage	I_{GVDD} =2mA		4.0	4.5	5.0	V

AC parameters TA=25°C, Vcc = 14 V, RL = 40 (unless otherwise stated)

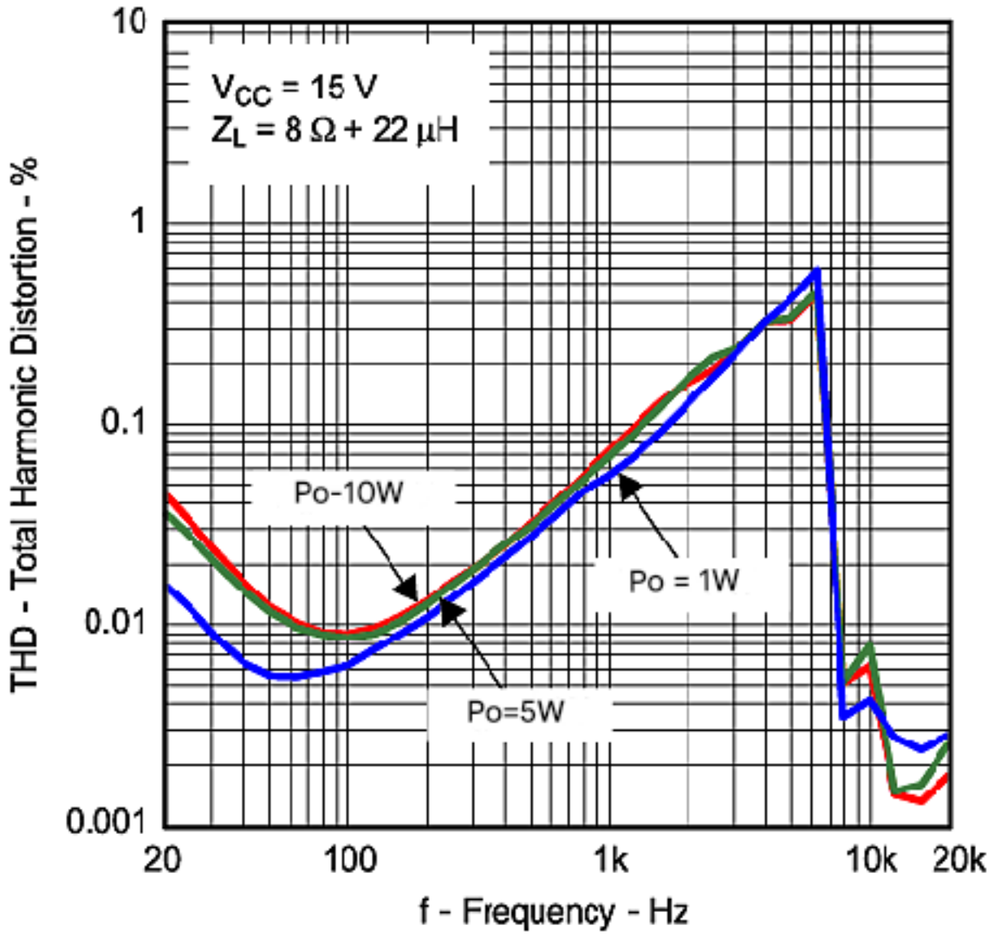
describe			Test conditions	minimum value	Typical value	maximum value	unit
K_{SVR}	Power supply ripple rejection ratio		1kHz, 200mVpp ripple Gain=20dB, input AC coupled to ground		70		dB
THD+N	total harmonic distortion plus noise		VCC=14V, f=1kHz Po=12W (half power)		0.1		%
V_n	Output noise		20~22kHz, add filter Gain=20dB		90		uV
					-80		dBV
	crosstalk		Vo=1Vrms,Gain=20dB,f=1kHz		-90		dB
SNR	signal-to-noise ratio		Maximum output when Gain=20dB THD+N < 1% , f=1kHz		102		dB
f_{osc}	Oscillation frequency				300		kHz
	Thermal protection temperature				170		℃
	hysteresis temperature				15		℃
Po	Stereo output	Output power	PO at 10% THD+N, VDD = 12V@RL = 4 Ω		20		W
			PO at 1% THD+N, VDD = 12V@RL = 4 Ω		16		
			PO at 10% THD+N, VDD = 16V@RL = 4 Ω		33.5		
			PO at 1% THD+N, VDD = 16V@RL = 4 Ω		27.5		
			PO at 10% THD+N, VDD = 18V@RL = 8 Ω		24.5		
			PO at 1% THD+N, VDD = 18V@RL = 8 Ω		20		
			PO at 10% THD+N, VDD = 21V@RL = 8 Ω		33		
			PO at 1% THD+N, VDD = 21V@RL = 8 Ω		27.5		
			PO at 10% THD+N, VDD = 24V@RL = 8 Ω		42.5		
			PO at 1% THD+N, VDD = 24V@RL =8 Ω		34.5		
	PBTL_mono	Output power	PO at 10% THD+N, VDD = 12V@RL = 4 Ω		22		
			PO at 1% THD+N, VDD = 12V@RL = 4 Ω		17.6		
			PO at 10% THD+N, VDD = 18V@RL = 4 Ω		47.6		
			PO at 1% THD+N, VDD = 18V@RL = 4 Ω		38.5		
			PO at 10% THD+N, VDD = 21V@RL = 4 Ω		64		
			PO at 1% THD+N, VDD = 21V@RL = 4 Ω		51.5		
			PO at 10% THD+N, VDD = 24V@RL = 4 Ω		82.2		
			PO at 1% THD+N, VDD = 24V@RL = 4 Ω		65.2		

Typical characteristic curves, all tests are based on 1KHz signal (unless otherwise specified)

TOTALHARMONICDISTORTION vs FREQUENCY(BTL)



TOTALHARMONICDISTORTION vs FREQUENCY(BTL)



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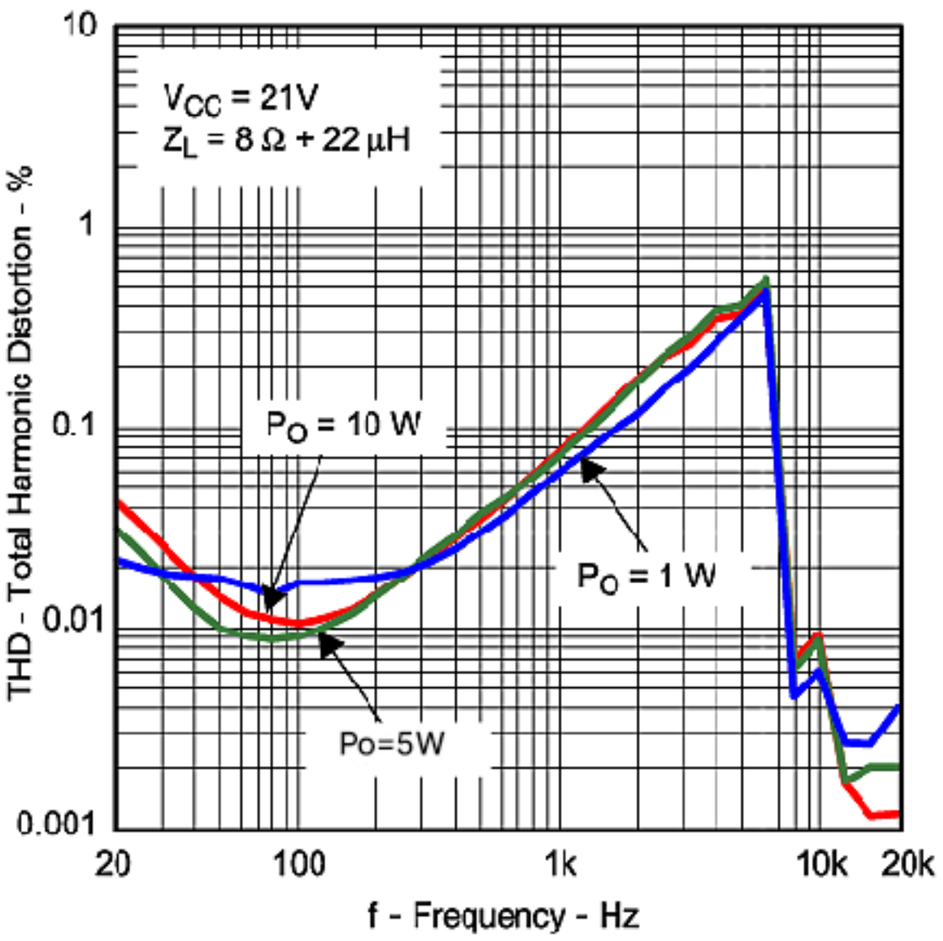

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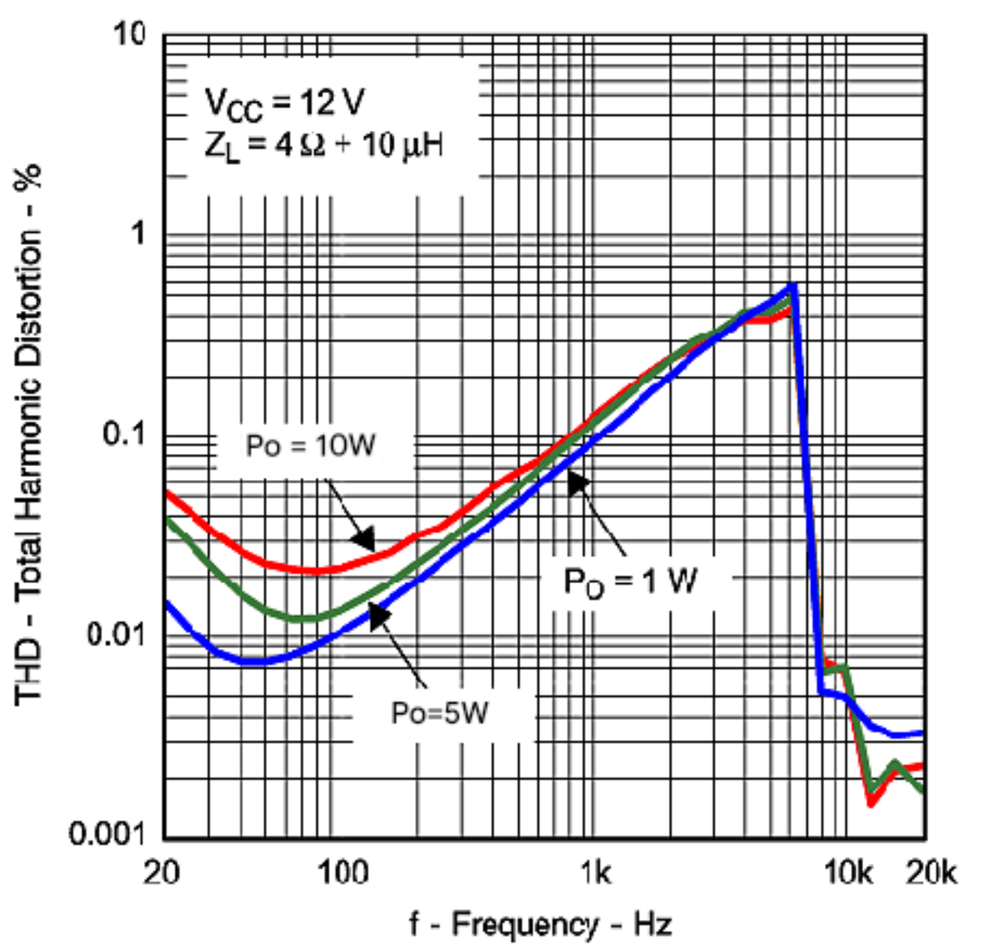
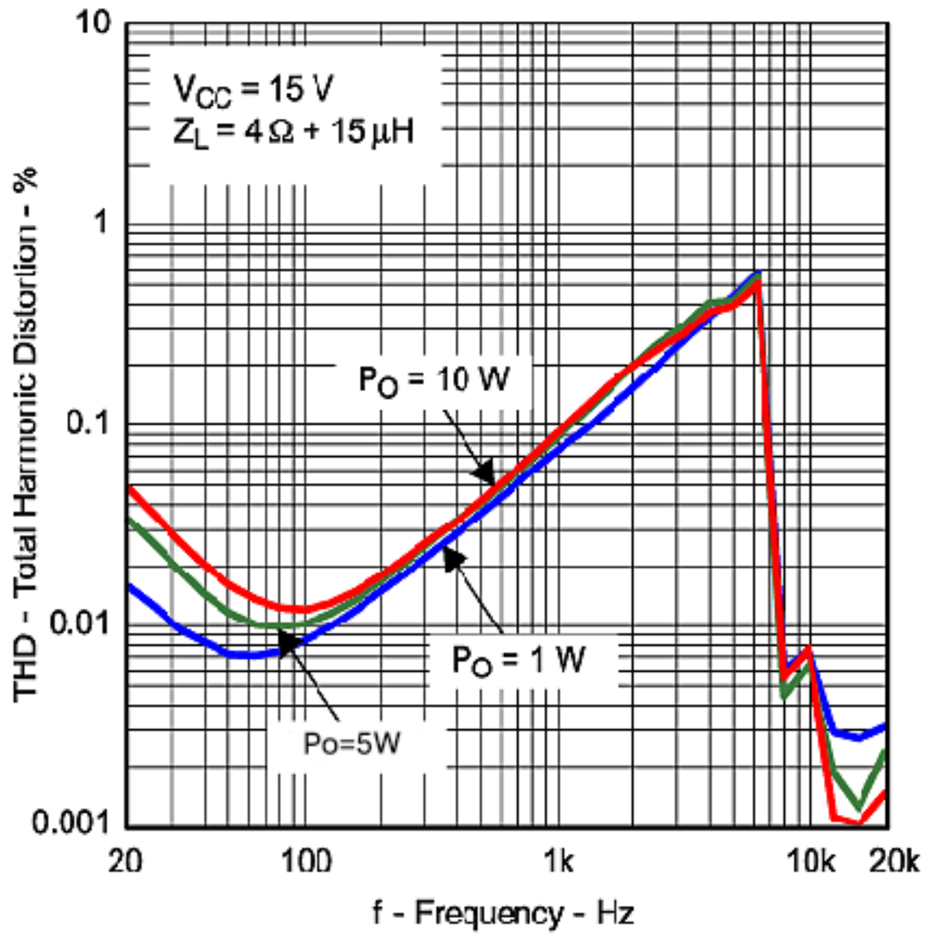
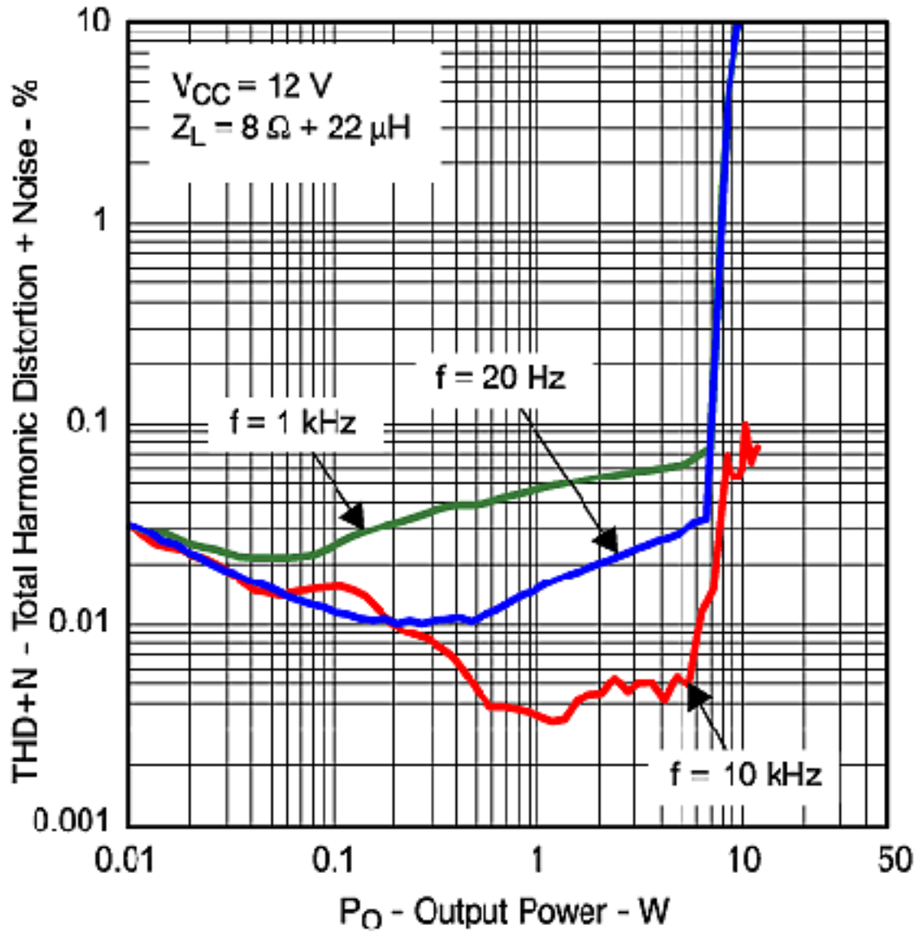


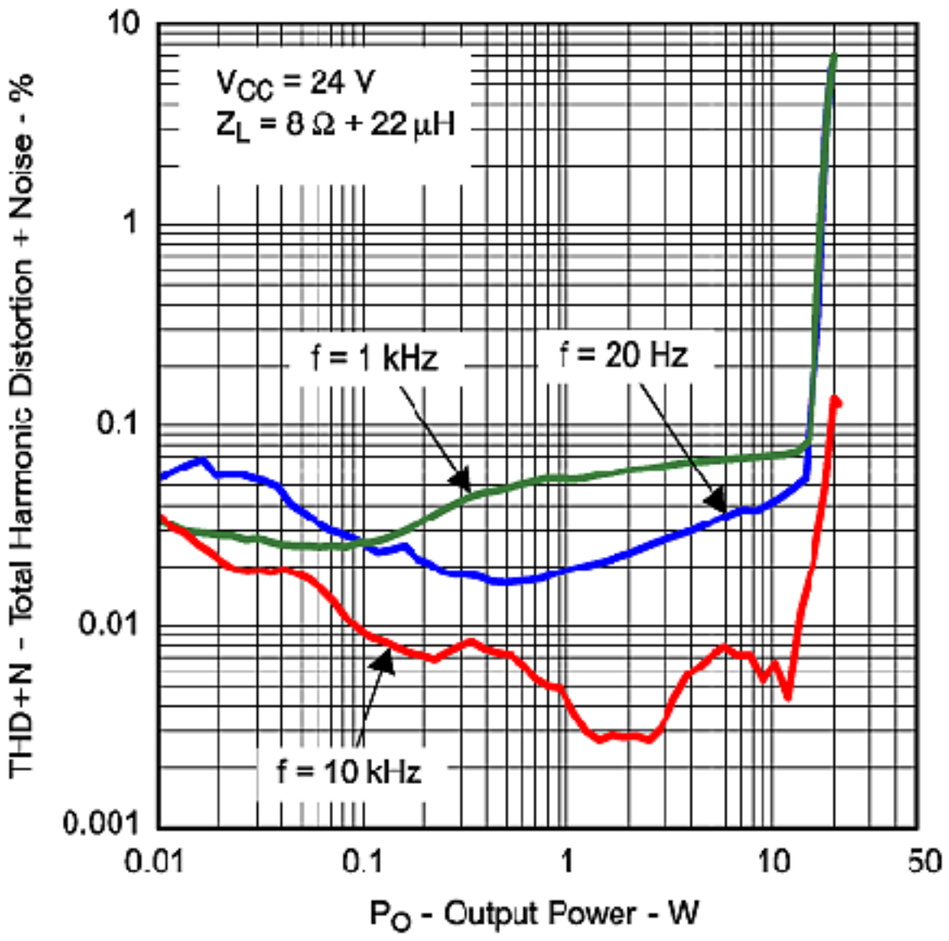
TOTALHARMONICDISTORTION vs FREQUENCY(BTL)



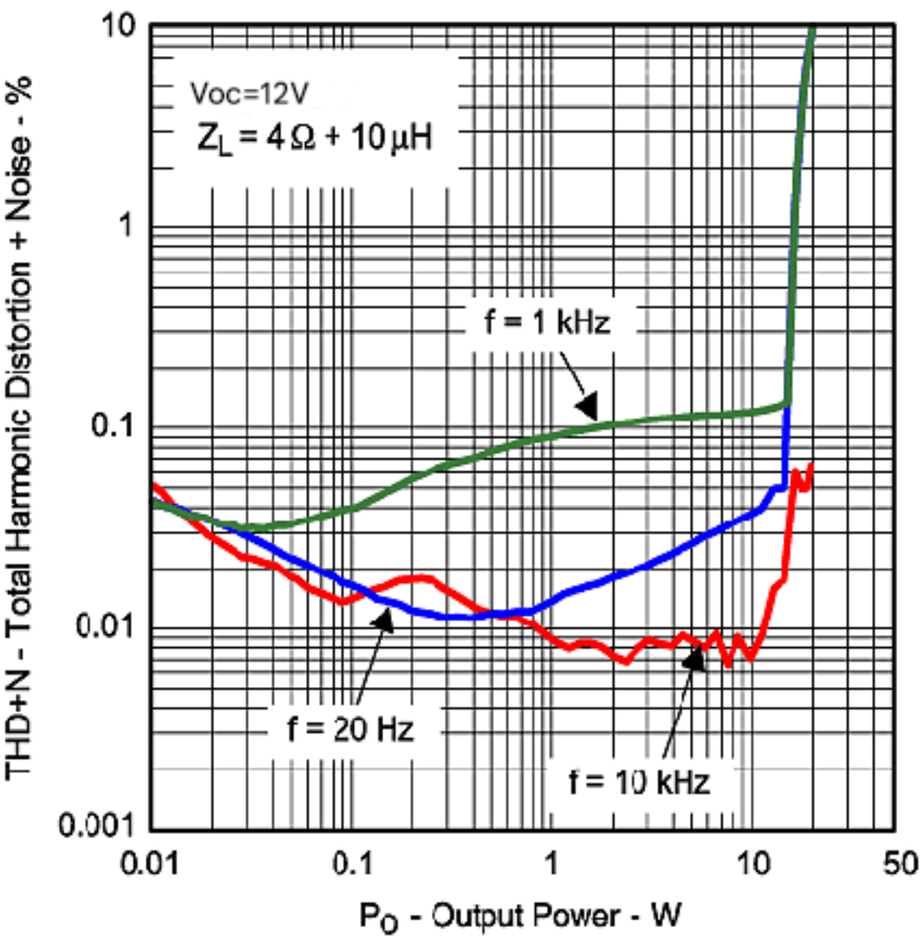
TOTALHARMONICDISTORTION+NOISE vs OUTPUTPOWER(BTL)



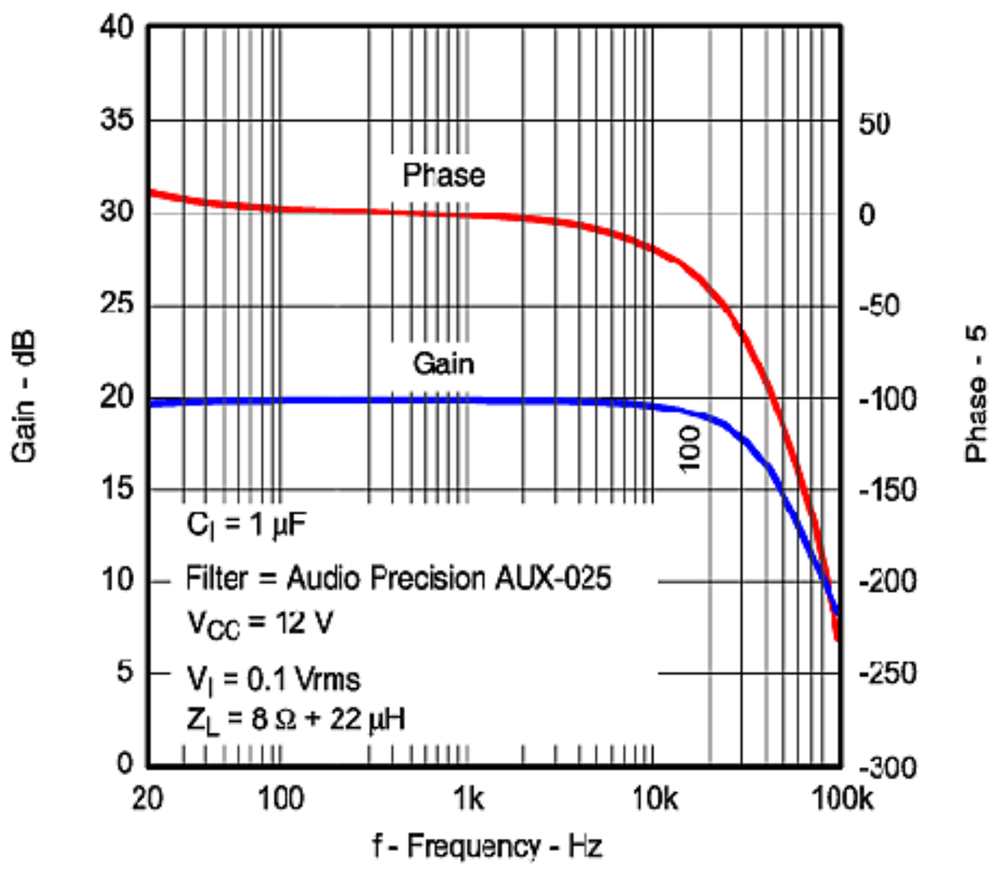
TOTALHARMONICDISTORTION+NOISE vs OUTPUTPOWER(BTL)



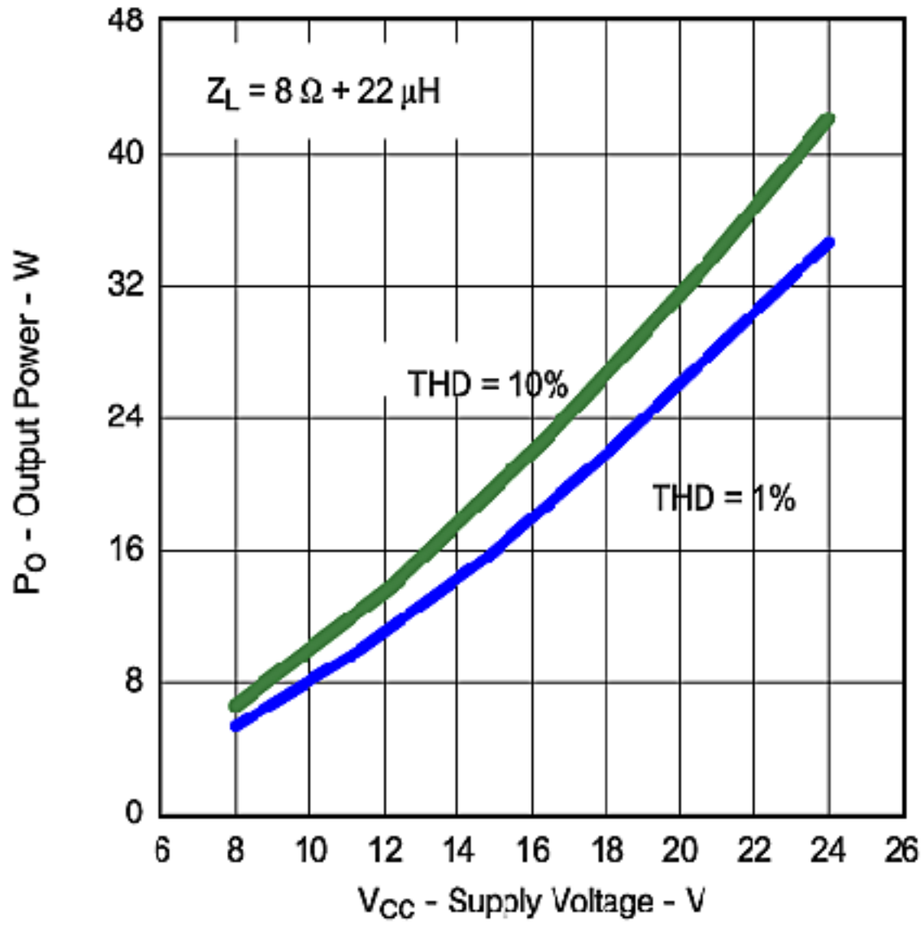
TOTALHARMONICDISTORTION+NOISE vs OUTPUTPOWER(BTL)



GAIN/PHASE vs FREQUENCY(BTL)

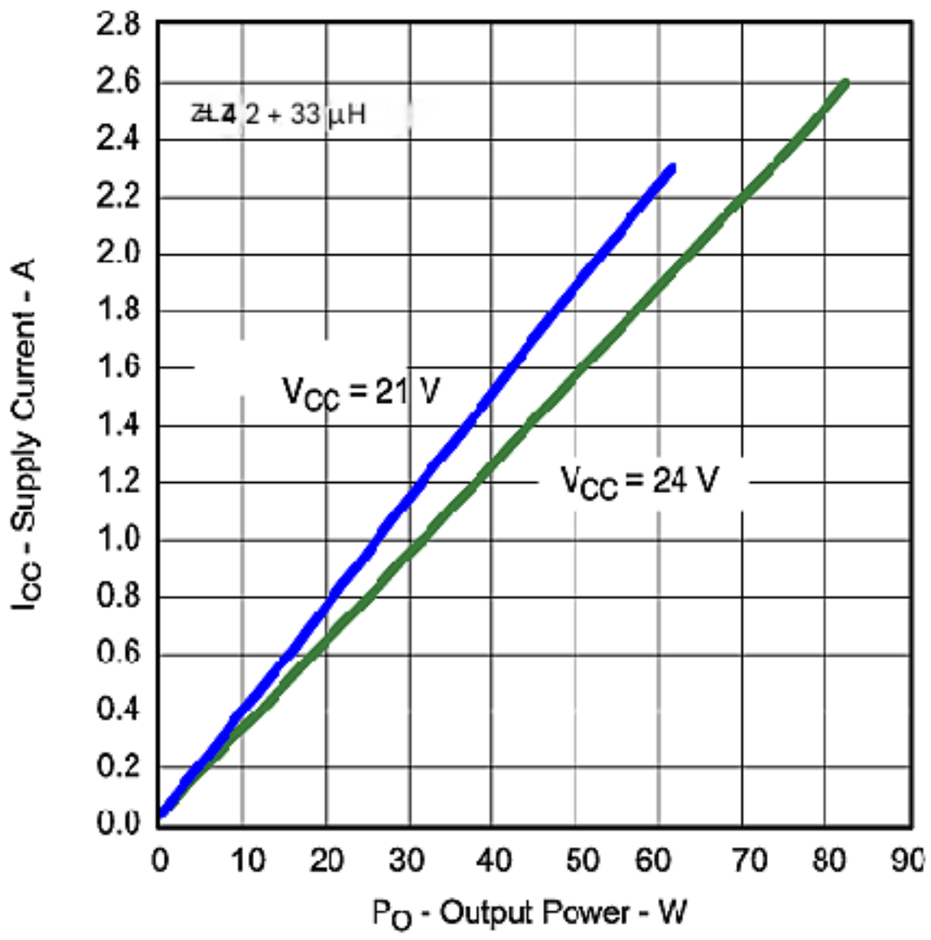


OUTPUTPOWER vs SUPPLYVOLTAGE(STERO)

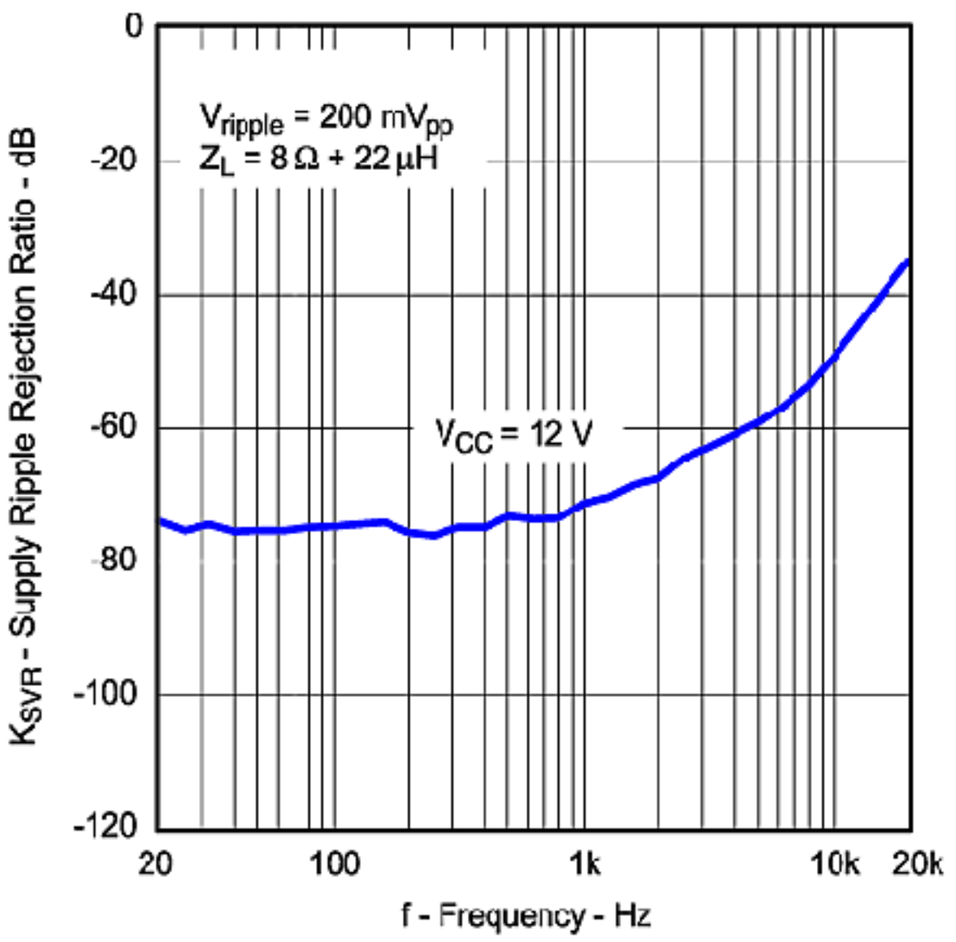


Note:DashedLinesrepresentthermallylimitedregions.

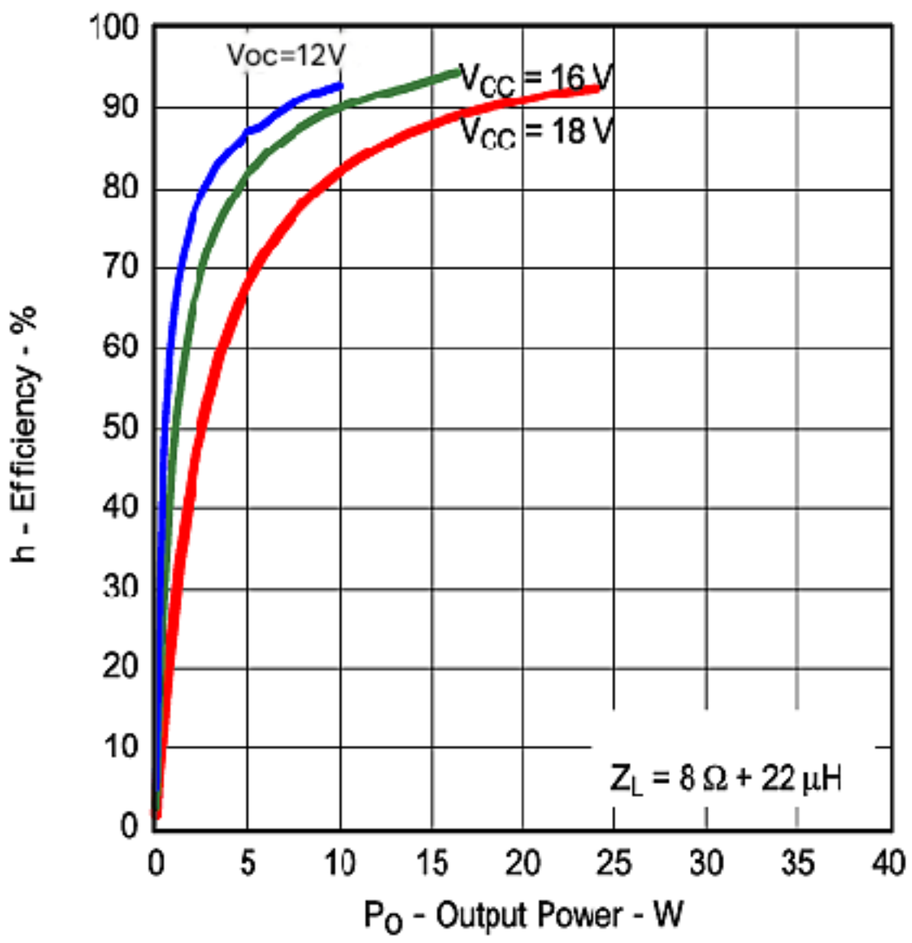
SUPPLYCURRENT vs OUTPUTPOWER(PBTL)



SUPPLYRIPPLEREJECTIONRATIO vs FREQUENCY(PBTL)

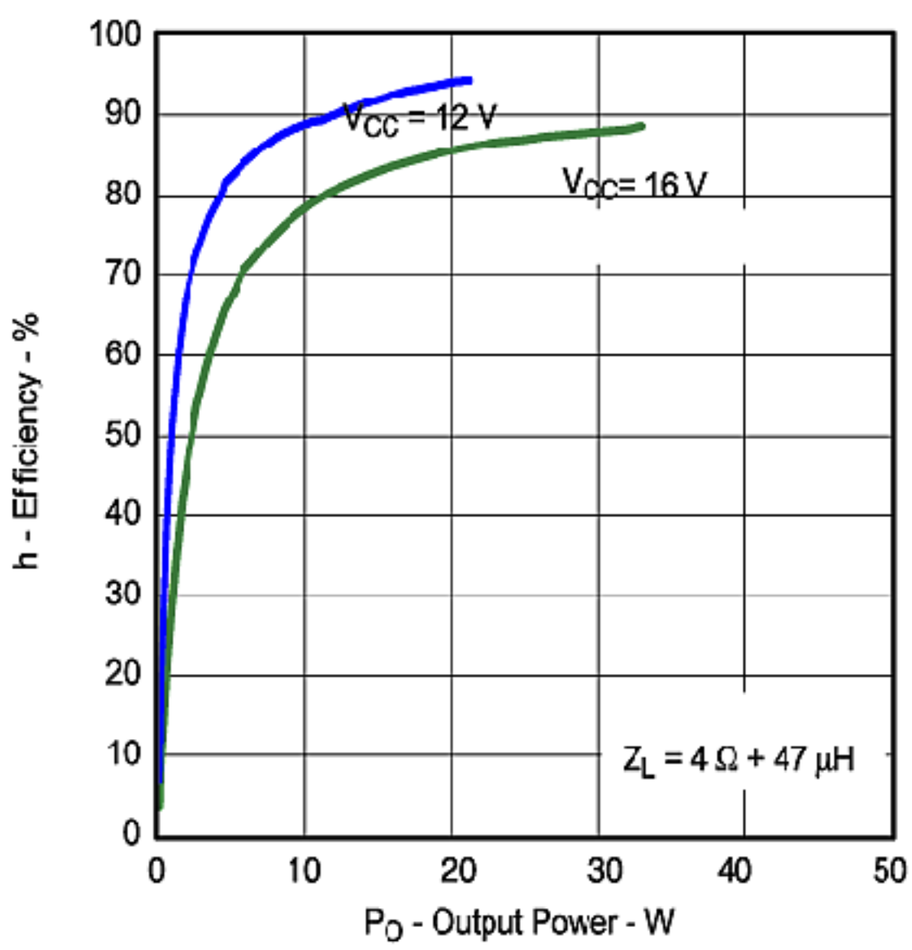


EFFICIENCY vs OUTPUTPOWER(BTL)



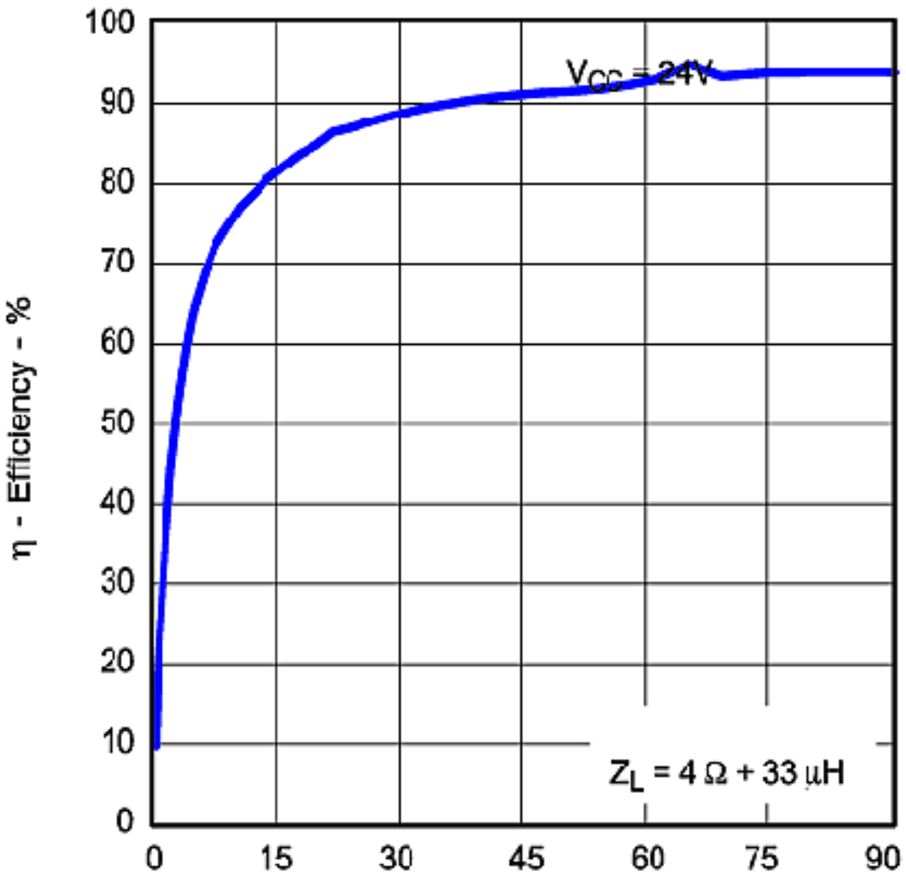
Note:DashedLinesrepresentthermallylimitedregions.

EFFICIENCY vs OUTPUTPOWER(BTL)



Note:DashedLinesrepresentthermallylimitedregions.

EFFICIENCY vs OUTPUTPOWER(BTL)



CROSSTALK vs FREQUENCY(BTL)