

Comparison of EMI Improved Differential Input Pair Structures Within an Integrated Folded Cascode Operational Transconductance Amplifier

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Abstract—This paper investigates the electromagnetic interference of integrated folded cascode operational amplifiers. In this context seven electromagnetic interference improved differential input pair structures are compared against each other in terms of their susceptibility, but also in terms of their influence on an initial standard reference circuit design and performance. Special focus is laid on not significantly altering these initial specifications that are defined for an integrated folded cascode amplifier, that is used as a case study. Comparisons are made of the investigated structures in terms of electromagnetic interference rejection ratio, area requirement, power consumption, changes in differential and common mode gain, gain-bandwidth product etc.

Index Terms—electromagnetic interference, operational amplifier, EMI improved, EMI robustness, folded cascode, EMI induced offset, differential input pair

I. INTRODUCTION

Robustness against electromagnetic interference (EMI) is a very critical aspect in modern integrated circuit (IC) designs. Conducted, coupled or radiated disturbances can lead to distortion phenomena, direct current (DC) shift and other effects hindering electronic circuits and devices to function properly. A severe effect in operational amplifier structures is a change in output voltage due to EMI, as such amplifiers are often used as input structures for sensitive analog signals, e.g. sensor interfaces. Such analog signals are often provided by wires in a cable harness or by printed circuit board (PCB) traces, and can therefore be overlaid with interference signals, as PCB traces and cables might act as receiving antennas for EMI.

There are already many different techniques described in the literature, offering concepts to reduce the effects of EMI on operational amplifiers. A recommended sequence on how to approach EMI problems is given in [1]. Therefore known countermeasures can be split into concepts of filtering [2], linearisation [3], [4] and compensation [5], [6], [7]. Most of the EMI countermeasures have the objective of cancelling disturbances coming into an IC via the inputs. These are often very complex to counteract [8, pp. 142-145]. The differential input stage plays a critical role in this, as changes of the operating point (OP) in this first stage are passed on to the next stages and would need to be counteracted subsequently. Making this first stage more EMI robust is thus critical for the

design. Most of the existing literature focuses on comparing a classical amplifier structure with an EMI improved structure of the same amplifier type. There is little information available, however, on the effects of different EMI improved input pairs in relation to each other. Furthermore, information on the influence of these different structures on the specifications of classical amplifier structures is scarcely available in any form.

This paper puts its focus on a comparison of known measures against EMI, implemented in a 0.35 μm technology, for the reasons mentioned, and does so not only in terms of effectiveness, but also in terms of area requirements, the need of matching or exact values, power consumption etc. Additionally changes on the initial amplifier specifications are investigated in a case study. This should help designers in their decision-making process when they must make a trade-off between initial specifications and the robustness requirement.

This paper is organised as follows: In section II a classical folded cascode operational amplifier, its specifications and also its susceptibility to EMI is described. In Section III seven different EMI measures on the differential input pair structure are revisited. Section IV deals with the analysis and comparison of these structures in terms of their EMI robustness, but also with the investigation of changes to the nominal specifications defined in Section II.

II. FOLDED CASCODE OPERATIONAL AMPLIFIER AND EMI CONSIDERATIONS

A folded cascode operational amplifier is used as a case study to investigate the effectiveness of different EMI robust differential input pairs. Therefore this section summarises the used circuit and highlights its EMI problems.

The basic reference schematic, called structure A further on, is shown in Figure 1, whereas the sizing of transistors M_0 to M_{10} is, in principle, not subject to change. This is done in order to keep the applied methods comparable. However, for some input structures the sizing has to be adapted. The basic folded cascode operational amplifier is designed to have an open loop gain of about 80 dB, a gain-bandwidth product (GBWP) of about 10 MHz and a phase margin of about 72° at an OP of $V_{inp} = V_{inn} = \frac{V_{DD}-V_{SS}}{2}$. A summary of all specifications is given in Table I, column A.

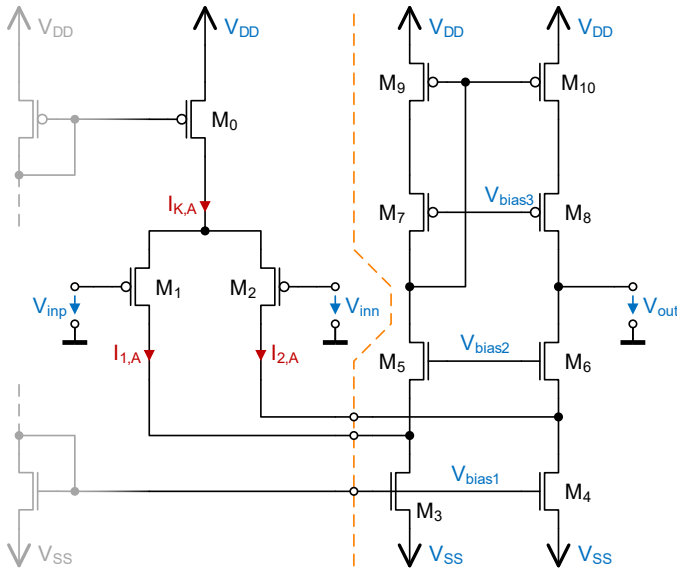


Fig. 1. Structure A: Standard initial folded cascode operational amplifier used as reference. In the course of the paper the input stage will be replaced by EMI improved structures.

The goal is to investigate the change in offset voltage at the output due to EMI disturbances. Two offset types thus need to be distinguished:

- The technological offset, which is introduced by the design and layout/matching of the amplifier and can be seen as intrinsic characteristic.¹
- The EMI induced offset arises by contrast, when an EMI signal couples into the pins of the amplifier and temporarily alters its DC OP.

Measures for reducing the technological offset need not necessarily have an effect on the EMI induced offset, which was shown in [9], [10]. This is the case due to different origins of offset generation. The technological offset mainly occurs due to non-perfect matching, whereas the EMI induced offset occurs due to non-linearities in the circuit. EMI can couple into such ICs via either input pins, the output pin or also the supply pins. However, the main focus in this case study will lie on the input pins, as these are most complex to counter [8, pp. 144-145], and especially the non-inverting input pin, when operating the amplifier as a voltage follower. This is for example of special interest, when operating the amplifier as sensor interface, where EMI could couple into PCB lines or cable harnesses of attached sensors.

There are different ways an EMI induced offset can originate due to disturbances [8, pp. 144-145]:

- Slew rate asymmetry, which is not dealt with here, as the amplifier is designed to have equal slew rates (see Table I).
- Strong non-linear distortion on the input stage, such that the transistors are forced into the cut-off or the ohmic region and
- weak non-linear distortion on the input stage. Whereas the latter is the most important EMI effect and is focused

¹The technological offset is not focused on in this paper, as there are already well-defined compensation techniques available, such as chopping or auto-zeroing.

on, as it is already occurring due to small disturbances.

Weak non-linear distortion can already be seen in the simplest level 1 transistor models, due to the drain current being quadratically proportional to the overdrive voltage ($V_{GS} - V_{TH}$). Due to this non-linear behaviour the drain currents are distorted. The offset voltage does not change much for in-band signals due to the high gain feedback loop. In the case of out-of-band signals, however, the amplifier can be seen as being operated in open loop, which leads to an EMI offset voltage being induced and therefore to a temporary, disturbance dependent output voltage change.

Different measures to mitigate these mentioned effects due to EMI injection are presented in the following. As already stated a special focus will be placed on adding EMI robustness, without significantly altering the circuit's behaviour and characteristics.

III. EMI ROBUSTNESS MEASURES

This section deals with measures and adaptations to the differential input pairs, in order to make the folded cascode amplifier more immune to EMI. In general there are four main concepts for increasing the EMI robustness of these input pairs adapted from [1]: filtering, linearisation, bandwidth and compensation. Each of these are explained in the subsequent sections.

A. Filtering

Filtering represents one of the simplest, but also most effective ways of eliminating unwanted EMI input signals. The influence of high frequency distortions is decreased, by adding filters to both inputs. In this way EMI signals should not reach the input differential pair at all. Such filters can be implemented in two ways:

- Externally: There are several issues that can arise when using external filters on PCB level. One crucial factor is that the two filter structures cannot be precisely matched, which may lead to a technological offset. Furthermore, the increased bill of material (BOM) leads to higher costs in production.
- Internally: Using internal/on-chip filtering reduces the previously stated problems of matching and BOM. However, due to the need of a low cut-off frequency of the filter, the on-chip area requirement is significantly increased.

The filtering input structure (used internally), that is investigated in this paper is subsequently denoted as structure B and depicted in Figure 2. Its effectiveness is discussed in [2]. The filtering (R_B , C_B) is designed to have a cut-off frequency of about 50 MHz. Keeping the same cut-off frequency, the area of the low-pass filter area can be decreased by increasing R_B , while simultaneously decreasing C_B . By contrast, however, the noise introduced by R_B increases with its value. This leads to a trade-off between area and noise. In this case study the noise contribution of the input transistors and the resistance are made to approximately match, which leads to a resistance of about $R_B = 1 \text{ k}\Omega$ and a capacitance of about $C_B = 3.2 \text{ pF}$.

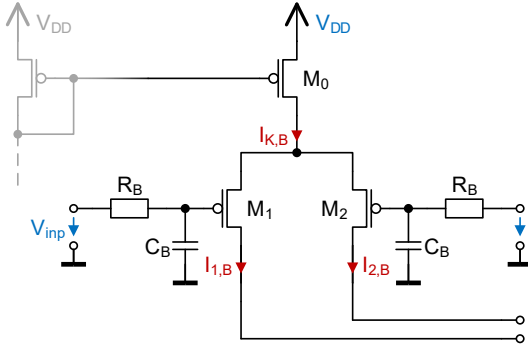


Fig. 2. Structure B: Differential pair with input RC-filter.

B. Linearisation

When filtering is not applicable or practicable, the next measure suggested by [1] is linearisation. In this way the effects of weak non-linear distortions are minimised, making both of the drain currents linearly proportional to the overdrive voltage in a specific input voltage range. Three approaches of linearising the differential input stage are summarised in the following.

1) *Source Degeneration*: Adding a resistor to the input differential pair source is a relatively simple approach, and it already helps in linearising the input stage [8, p. 154], [3]. By this means, however, the transconductance is also lowered, when increasing R_C and therefore the differential gain A_{DM} also decreases. The structure of the source degenerated differential pair is given in Figure 3 as structure C. When dimensioning the resistor R_C a trade-off between obtaining a higher EMI rejection (larger resistor size) and maintaining a higher differential gain (smaller resistor size) has to be found. In this case study $R_C = 1 \text{ k}\Omega$ is used as trade-off.

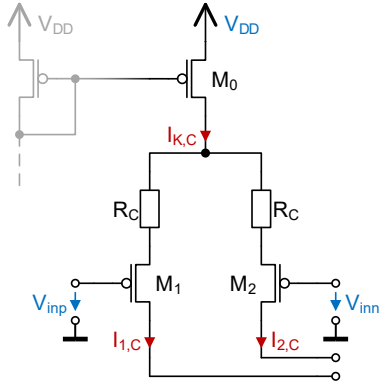


Fig. 3. Structure C: Differential pair with resistive source degeneration.

2) *Cross-Coupled Differential Pair*: Another approach in linearising the transconductance of the input structure utilises a second, cross-coupled differential pair, as shown in Figure 4, structure D. The third-order harmonic of the unfiltered input signal is cancelled out, when equation 1 is fulfilled [4]. In order to maintain the same differential gain, the transistor dimensioning needs to be adapted (increased width), in such a manner that the equations $i_{K,A} = i_{K,D1} - i_{K,D2}$ and therefore $i_{1,D} = i_{1,A}$ and $i_{2,D} = i_{2,A}$ hold true for the small-signal currents.

$$\frac{I_{K,D1}}{I_{K,D2}} = \left(\frac{\frac{W_{1,D1}}{L_{1,D1}}}{\frac{W_{1,D2}}{L_{1,D2}}} \right)^3 \quad (1)$$

The currents $I_{K,D1}$ and $I_{K,D2}$ are chosen to have a ratio of about 3. This leads to width over length ratios of about $\frac{W_{1,D1}}{L_{1,D1}} = \frac{W_{2,D1}}{L_{2,D1}} = \frac{200 \mu\text{m}}{2 \mu\text{m}}$ and $\frac{W_{1,D2}}{L_{1,D2}} = \frac{W_{2,D2}}{L_{2,D2}} = \frac{140 \mu\text{m}}{2 \mu\text{m}}$. However for DC the overall current is consisting of $I_{K,D1} + I_{K,D2} > I_{K,A}$. Therefore M_3 and M_4 of the initial reference design have to be extended by the transistors $M_{3,D}$ and $M_{4,D}$ in order to cope with the increased DC currents $I_{1,D}$ and $I_{2,D}$. The main disadvantage with this concept is the need for proper matching of each of the transistors in the two differential pairs, as well as proper matching among the two differently dimensioned differential pairs.

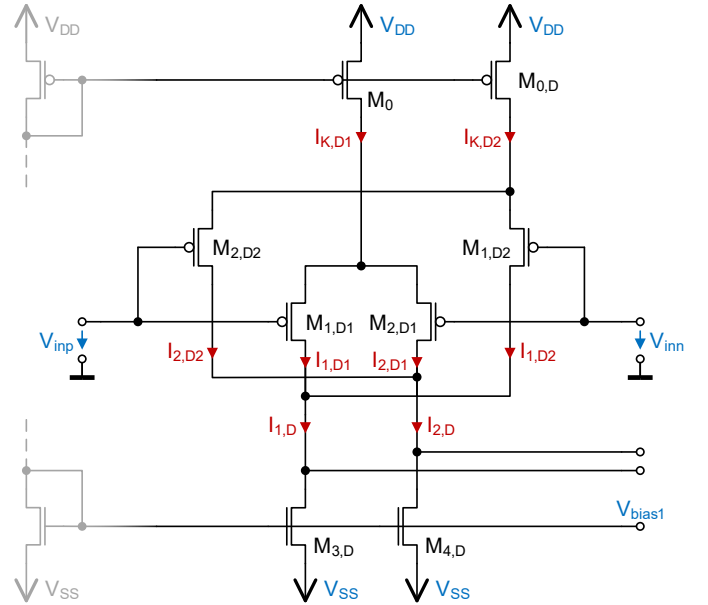


Fig. 4. Structure D: Differential pair with cross-coupled double differential pair.

3) *Combination: Source Degeneration and Cross-Coupled Differential Pair*: Finally a combination of source degeneration and cross-coupled double differential pairs can be investigated as shown in Figure 5 (structure E) and dealt with in [4]. This leads to a wider input range of linear behaviour. However, the differential gain is again decreased, as the transconductance g_m is decreased too. Again the initial transistors M_3 and M_4 need to be extended by the transistors $M_{3,E}$ and $M_{4,E}$ similarly to structure D. The resistors are sized by $R_D = 500 \Omega$, as a trade-off between gain and linearisation.

C. Increasing Bandwidth

Increasing the bandwidth/speed of the amplifier helps in keeping the feedback loop stable at higher frequencies. By this means the offset voltage would intrinsically be partly compensated. However, as the goal of this paper is to maintain the given characteristics of structure A the bandwidth is not subject to change.

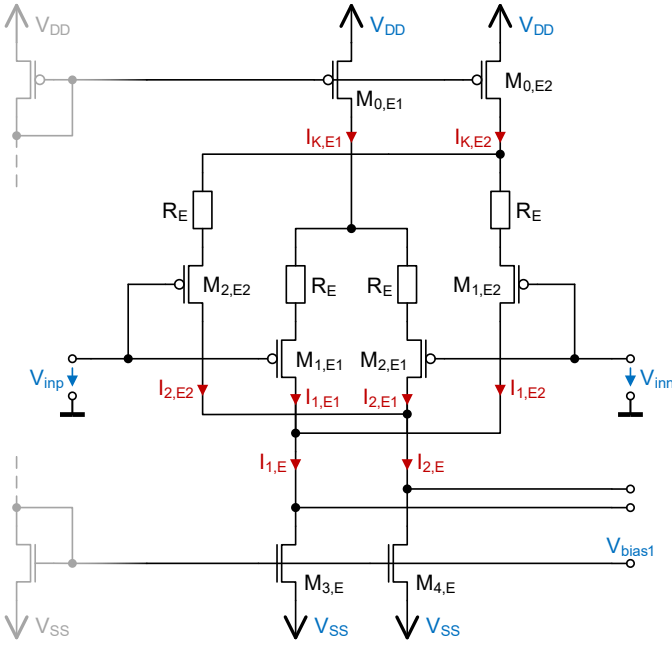


Fig. 5. Structure E: Differential pair with cross-coupled double differential pair.

D. Compensation

The last measure of [1] consists of compensating distortions, that are introduced by EMI, which occur, e.g. if the input filter is not that effective to mitigate an EMI disturbance.

1) *Cross-Coupled Double Differential Pair*: Again a cross-coupled double differential pair can be used for compensation of EMI effects in the input stage. However, in contrast to structure D no linearisation is happening, but the non-linear distortion is occurring first and is subsequently cancelled out [5]. This is done by an equally-sized cross-coupled differential pair ($M_1 = M_{1,F}$, $M_2 = M_{2,F}$), that is only activated at higher frequencies by using high-pass filters, which are designed to have the same corner frequency (and dimensioning due to the same considerations) as the low-pass filters from section III-A. The idea is, that at frequencies above the corner frequency of the high-pass filter, the current difference introduced by M_1 and M_2 is exactly counteracted by the transistors $M_{1,F2}$ and $M_{2,F2}$, such that no current difference is introduced. By this means no high-frequency EMI signal should pass through to the output, since it is now compensated and counterbalanced. The schematic of this input stage is illustrated in Figure 6 and denoted as structure F. Again $M_{3,F}$ and $M_{4,F}$ are added to cope for the higher DC currents through both branches. The bias voltage V_{bias4} is adapted in such a manner that the transistor $M_{1,F2}$ and $M_{2,F2}$ are operated in saturation.

2) *Complementary Double Differential Pair*: A complementary double differential pair can be used similarly to structure F. Again the additional differential pair is only active at higher frequencies (by using high-pass filters), aiming for compensation of the non-linearly distorted differential current [6]. In this case again, the differential pairs are not linearised but the current difference $I_{1,G1} - I_{2,G1}$ is counteracted by the current $I_{1,G2} - I_{2,G2}$ at higher frequencies. To account for the higher currents through M_9 and M_{10} the dimensioning

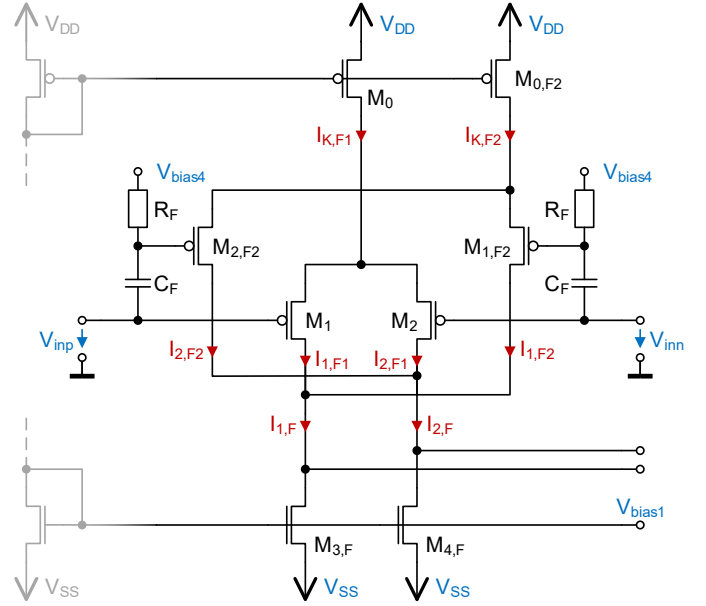


Fig. 6. Structure F: Differential pair with cross-coupled double differential pair for compensating non-linear effects.

has to be adapted by adding the transistors $M_{9,G}$ and $M_{10,G}$ in parallel. This is illustrated in Figure 7 as $M_9 + M_{9,G}$ and $M_{10} + M_{10,G}$, meaning the sum of widths W_9 , $W_{9,G}$ respectively W_{10} , $W_{10,G}$.

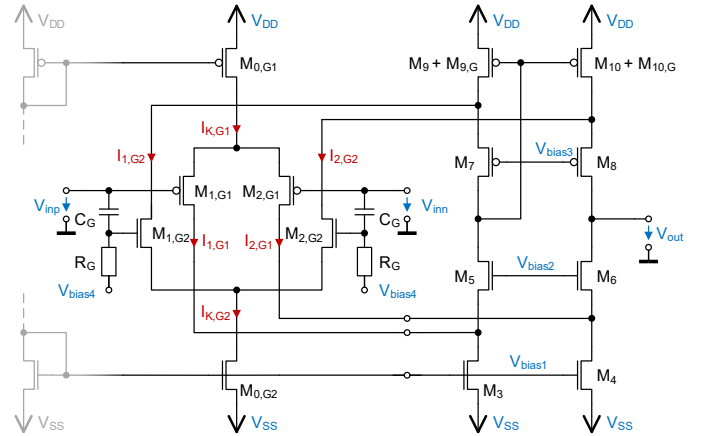


Fig. 7. Structure G: Differential pair with complementary double differential pair for compensating non-linear effects.

3) *Source-Buffered Differential Pair*: In contrast to the previous structures, source-buffering aims at achieving a different type of compensation. In this case the back-gate effect is utilised, as described in [7]. Along with specific dimensioning of the gate-source voltage by adding C_H the common-mode transfer function of the amplifier is forced to zero. The associated circuit is denoted as structure H and is shown in Figure 8. However, in this input pair the problem of needing exact values (not only matching) arises. Deviations from this ideally calculated capacitance have significant influence on the performance of this structure.

IV. SIMULATIONS AND RESULTS

In this section the performed simulations are explained and the results are analysed, by comparing the structures A to H,

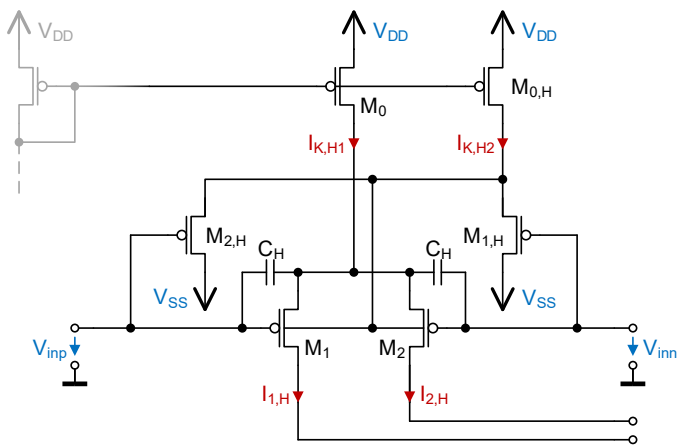


Fig. 8. Structure H : Differential pair with source-buffering.

that were described in the previous section. All characteristics are measured at an voltage of $V_{DD} = -V_{SS} = 1.65$ V, at a nominal temperature of 27°C and for nominal corners.

On the one hand typical amplifier characteristics such as technological DC offset, gain, GBWP, area, power consumption etc. are compared, in order to ensure, that any changes to the input stages do not significantly alter the amplifier's behaviour. On the other hand the structures are compared concerning their EMI robustness. All of these are summarised in Table I and are described within this section. In addition, the table cells are colorised, in order to represent good/bad effects in terms of deviations from the reference specification.

Evaluating the EMI robustness can be done by calculating the so called electromagnetic interference rejection ratio (EMIRR) [11], which is commonly used, despite its flaws [12], [13]. For comparing the behaviour of the folded cascode circuits in closed loop, the EMIRR of the non-inverting input pin (EMIRR IN+) is measured as described in [11, pp. 4, 5]. For this case the DC input voltage is superimposed by a high frequency signal with defined peak voltage. In Table I the EMIRR is calculated at an EMI disturbance voltage of 100 mV (peak voltage) for frequencies, that are commonly used for communication purposes as suggested in [14, p. 2].

Structure B , utilising RC low-pass filters, performs best in terms of EMIRR without changing the other transistor parameters significantly. A major drawback, however, is the significantly increased area requirement (about 8 times larger) for the whole amplifier circuit, assuming poly resistors and capacitances. The area demand is shown in Table I as a percentage of the reference circuit. It was calculated from the dimensioning of the transistors, resistors and capacitances given in the structures including the output branch. As mentioned previously the area can be reduced, but introducing the drawback of increased noise due to larger resistor sizes. The same problem also arises for structures F and G , that use similar dimensioning for the high-pass filters needed. Due to the filters only altering the circuit at higher frequencies (above the unity gain frequency), also the specifications given in section II for structure A are fully met. Similarly the increased area of structure H is depending on the capacitance C_H .

Structures *C*, *D* and *E*, that are adapting the concept of linearisation are much less area-demanding. However, these

also have a lower EMIRR. Furthermore, making the transconductance of the input pair constant over a wider range, comes with the negative effect of simultaneously decreasing the transconductance. Therefore the differential mode gain is decreased by a few dB. In structure *E* source degeneration and harmonics cancellation is applied. The combination of both linearisation techniques shows, that the more linearised the input stage is, the higher the EMIRR that can be reached, but also the lower the transconductance of the input stage becomes. Furthermore the GBWP is also decreased. The output swing and the power consumption are not significantly altered by any structure, but the phase margin might pose a problem for structure *F*, that utilises a cross-coupled differential pair with a high-pass filter.

Another important topic, that needs to be considered when using these structures in integrated circuits is the demand for matching or even absolute values. Starting with structure *A*, the input transistors themselves of course, need to match to the greatest extent possible. The same is true for structures *B* and *C*, and this not only for the input transistors, but also for the resistors and capacitances used. This is quite straightforward and therefore classified "easy". Structures *D* and *E* do not only demand matching two and two transistor pairs, but also the ratio between one and the other differential input pair must be adjusted precisely, requiring "medium" effort. On the contrary, structures *F* and *H* need four equally matched transistors in order to keep the offset voltage low. The greatest design efforts, however, must be concentrated on the structures *G* and *H*, since either the currents of the PMOS and NMOS transistors must be matched (structure *G*) or capacitances must be trimmed to exact values (structure *H*), leading to the classification "hard".

Besides investigating the EMIRR for specific frequencies, another analysis is shown in Figure 9, illustrating the EMI induced offset over a broader frequency range (from 1 MHz to 10 GHz) at a peak amplitude of 500 mV. The behaviour of the different structures is shown as deviation from the technological offset. At frequencies up to 10 MHz all structures behave similarly, as this still lies within the bandwidth of the amplifier. Due to the decreasing gain a negative offset voltage is induced by EMI. However, for higher frequencies the EMI countermeasures start inducing an inverse offset voltage. This works especially well for structures *B*, *C*, *E*, *F*, *H*. By contrast, structures *D* and *G* remain with larger offset voltages at high frequencies, whereas structure *G* performs worst around the corner frequency defined by the high-pass filter, when the NMOS differential pair is about to be turned on. Figure 9 shows, that structure *G* might not be the best choice even though it may have performed acceptably in Table I.

Outlook: The comparison of these different input pair structures was only dealt with on a single topology and dimensioning level as a case study. Further research will be put into the question, of whether different specifications and dimensioning of the nominal reference structure lead to the same qualitative behaviour of the EMI induced offset in respect to the EMI frequency. Additionally it is planned to implement these structures in terms of a test chip and to cross-check the simulated behaviour with the real behaviour.

TABLE I
SUMMARY OF FOLDED CASCODE STRUCTURES WITH DIFFERENT EMI ROBUST INPUT STAGES

Structure	Reference	Filtering	Linearisation			Compensation			
	A	B	C	D	E	F	G	H	
Technological DC Offset	61.77	61.77	200.5	92.29	165.5	82.37	106.8	61.77	μV
Differential Mode Gain	82.46	82.46	75.96	78.81	73.74	79.71	78.3	82.46	dB
Common Mode Gain	-21.5	-21.5	-9.24	-18.13	-17.2	-22.3	-21.6	-21.5	dB
GBWP	10.3	10.1	5.85	8.51	4.53	9.14	21.6	10.3	MHz
Phase Margin	86.0	72.7	86.7	85.4	86.7	57.3	79.7	86.0	$^\circ$
Power Consumption	1.02	1.02	1.02	1.44	1.44	1.48	1.49	1.48	mW
Output Swing	2.65	2.65	2.6	2.54	2.52	2.63	2.65	2.65	V
Slew Rate Ratio (rising/falling)	48.3/51.7	49.5/50.5	50.2/49.8	48.6/51.4	49.6/50.4	50/50	53.9/46.1	49.0/51.0	%
Area Comparison	100	780	102	181	184	842	815	572	%
Matching/Trimming Effort	easy	easy	easy	medium	medium	easy	hard	hard	-
EMIRR @ 100 mV, 400 MHz	37.2	76.3	46.0	44.2	55.6	68.0	51.4	60.0	dB
EMIRR @ 100 mV, 900 MHz	38.5	93.0	47.6	45.6	61.0	75.3	47.7	59.5	dB
EMIRR @ 100 mV, 1.8 GHz	39.0	104.2	48.2	46.2	67.4	90.0	47.2	58.2	dB
EMIRR @ 100 mV, 2.4 GHz	39.1	109.5	48.3	46.1	69.5	80.6	47.3	59.3	dB

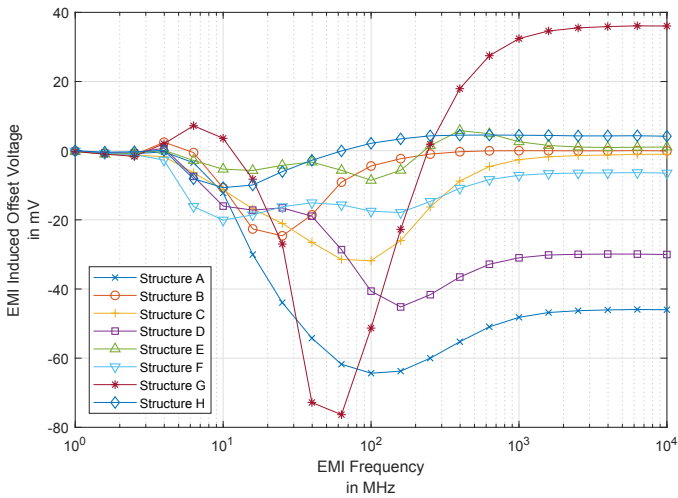


Fig. 9. EMI induced offset voltage over frequency for an EMI amplitude of 500 mV.

Figure 9 shows that the deviation in offset has different directions depending on the structure used. Therefore, it would also be of interest to investigate, whether it is possible to combine structures having a positive EMI induced offset, with structures having a negative EMI induced offset voltage. In addition it should be shown, that comparing the EMIRR on single frequencies may not be the best choice for classifying the EMI robustness of a structure.

V. CONCLUSION

In this paper various EMI robust differential input pair structures have been compared. The goal was to investigate the main advantages and disadvantages when applying different EMI mitigation techniques to a reference folded cascode operational amplifier. The measures applied were filtering, linearisation and compensation, whereas each of these offer well-functioning topologies. Special focus was put on how the specifications of the initial structure are affected by introducing the EMI countermeasures referred to. It was shown that the measures having the highest EMIRR are most area-consuming. By contrast linearisation techniques lead to a decreased differential mode gain. Therefore a trade-off between area, EMIRR and other amplifier specification values has to be made and this document should be a help for designers achieving this aim.

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