

Special Correspondence

A Low-Noise Amplifier for Switched Capacitor Filters

RICHARD D. JOLLY AND ROBERT H. McCHARLES

Abstract—A low-noise CMOS amplifier and a switched capacitor integrator is described along with experimental data on $1/f$ noise. An amplifier for use in switched capacitor circuits was fabricated that achieved an input referred noise of 130 nV per root Hz at 100 Hz in a die area of only 0.12 mm². Using the amplifier we have fabricated a low-noise switched capacitor integrator which has a dynamic range of 110 dB over a 10 kHz bandwidth.

INTRODUCTION

Because of their low cost and the ease of integration with digital logic, MOS devices are being used in many analog applications. However, low-frequency noise is an often cited reason for rejective MOS devices for other analog applications. In this correspondence we will show that properly designed CMOS amplifiers need not suffer from this problem.

We will first look at noise in discrete MOS devices. Next we will describe the design and performance of a low-noise CMOS differential amplifier. Finally, we will look at the performance of a monolithic switched capacitor integrator which we have constructed using this amplifier.

Noise in Discrete MOS Devices

Experimental noise measurements on eight MOS devices are shown in Figs. 1 and 2. These devices were fabricated using a digital silicon gate 6 μ m p-well CMOS process. Oxide thickness was 750 Å. All devices were measured with a drain current of 45 μ A.

At low frequencies the noise voltage density is inversely proportional to the square root of frequency. At high frequencies the noise voltage density is constant. The frequency at which the constant (broad-band) noise density is equal to the low-frequency ($1/f$) noise density is called the corner frequency (f_c).

The $1/f$ noise is due to random fluctuations in the density of charge carriers in the channel. These carriers can enter and leave traps in the oxide close to the silicon-oxide interface. The $1/f$ noise for a saturated MOS device has been modeled as a voltage source connected to the gate with a value of [1]

$$\frac{\overline{v_{eq}^2}}{\Delta f} = \frac{B}{ZL} \frac{1}{f} \quad (1)$$

where B is a constant, Z is the channel width, L is the channel length, and f is frequency.

Comparing Figs. 1 and 2 we see that a 100/5 NMOS device exhibits a noise voltage density of 700 nV per root Hz at 100 Hz, while a corresponding PMOS device has 150 nV per root Hz at the same frequency. Similar results have been reported

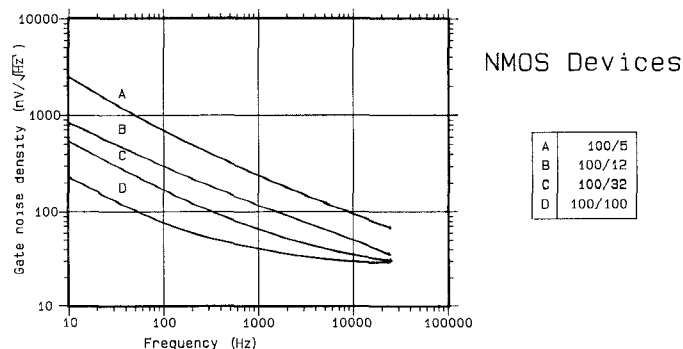


Fig. 1. Experimentally observed equivalent gate noise of four NMOS transistors.

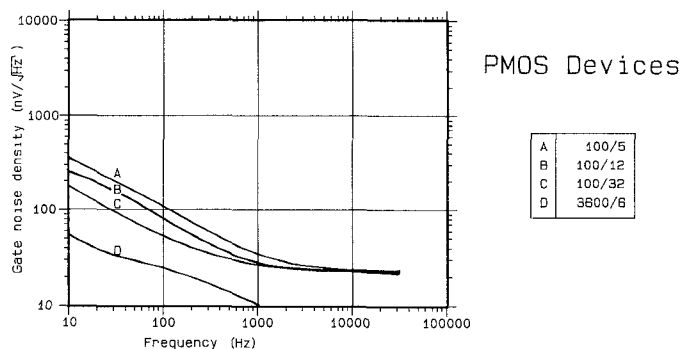


Fig. 2. Experimentally observed equivalent gate noise of four PMOS transistors.

by others [1]–[3]. Any conduction current through an insulator, whether Frenkel-Poole, tunneling, Schottky, or hot carrier injection, decreases exponentially as the potential barrier between the carrier's band in the semiconductor and the corresponding band in the insulator increases [4]. Since the barrier seen by holes in the valence band is greater than the barrier seen by electrons in the conduction band, fewer holes will be injected and trapped in the oxide. The noise relationship between NMOS and PMOS devices can thus be explained.

Figs. 1 and 2 also show that $1/f$ noise decreases with device area. This $1/ZL$ dependence has been observed elsewhere [1], [2], and can be derived from the fact that the autocorrelation of the differential noise along the device width is zero [5]. The factor B in (1) depends on oxide thickness, the silicon-oxide barrier, and the quality of the interface [6]. The observed dependence on bias current is very weak.

The broad-band component of MOS transistor noise is thermal noise from the channel resistance. This noise source can be modeled by including another voltage source in series with the gate whose value is [1]

$$\frac{\overline{v_{eq}^2}}{\Delta f} = 4kT \frac{2}{3} \frac{1}{g_m} \quad (2)$$

where g_m is the transconductance of the MOSFET.

Manuscript received April 12, 1982; revised July 2, 1982.

The authors are with Hewlett-Packard Laboratories, Palo Alto, CA 94304.

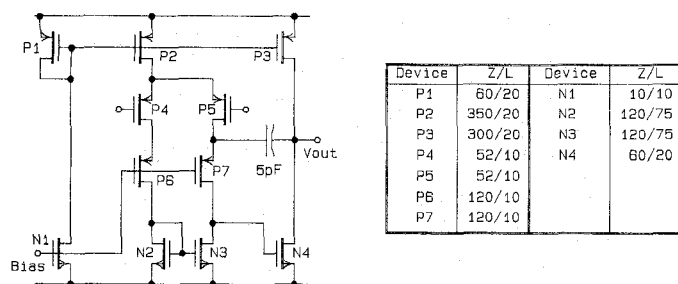


Fig. 3. Schematic diagram of the low-noise CMOS amplifier.

TABLE I
TYPICAL AMPLIFIED PERFORMANCE

SPECIFICATION		UNITS
DIE AREA	(0.35) ²	mM
POWER DISSIPATION	1.2	mW
INPUT DEVICE AREA	1300	μM
1/f NOISE AT 100 Hz	130	nV/√Hz
BROADBAND NOISE	30	nV/√Hz
NOISE CORNER FREQ.	1	kHz
INPUT OFFSET	10	mV
UNITY GAIN BW	1.1	MHz
OUTPUT SWING	+/-4.3	V
OPEN LOOP GAIN	80	dB
SETTLING TIME (1%, 4 VOLT STEP)	2	μs

A LOW-NOISE CMOS AMPLIFIER

A schematic of the low-noise CMOS amplifier is shown in Fig. 3. It uses a straightforward two-stage design. The noise analysis from [3] was important in the design of the width of *P4* and *P5*, the length of *N2* and *N3*, and the ratio of the length of *N2* and *N3* to the length of *P4* and *P5*. The final design parameters were chosen to maximize the amplifier's performance in switched capacitor circuits. The input devices *P4* and *P5* are cascoded with *P6* and *P7* which have no significant effect on the noise performance. These cascode devices improve the gain of the input stage and allow for an unusual connection of the compensation capacitor at the common source-drain node. This node has a gain of less than unity from the amplifier inputs, which ensures that the right-half plane zero caused by feedforward through the compensation capacitor will not cause oscillation. This method of compensation is less sensitive to loading on the second gain stage than other methods. This permits the output to be taken directly from the second stage without the addition of an output stage. It is not intended for this amplifier to drive resistive loads or large external capacitances. Experimental results from this amplifier are shown in Table I.

A LOW-NOISE SWITCHED CAPACITOR INTEGRATOR

Using the low-noise amplifier, we have fabricated a switched capacitor integrator. As shown in Fig. 4 the integrator has been fabricated with capacitor arrays which are programmed to implement filter coefficients. A die photo of the circuit is shown in Fig. 5. The response of the integrator to a square-wave input is shown in Fig. 6. This integrator circuit has been used for constructing switched capacitor filters which will later be fabricated in integrated form. We have used this integrator to construct several state variable and ladder filters of up to tenth order.

Noise measurements from an operating integrator are shown in Fig. 7. These measurements were made with the integrator's input grounded. Parasitic capacitance increased the noise gain from 2 up to 2.7. The integrator's output was fed to a

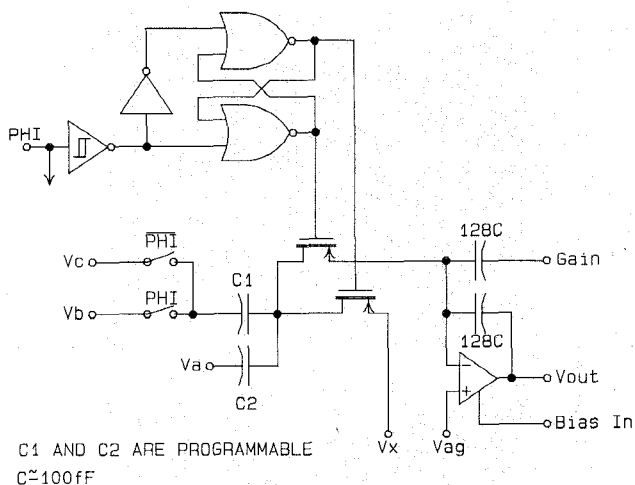


Fig. 4. Schematic diagram of the switched capacitor integrator.

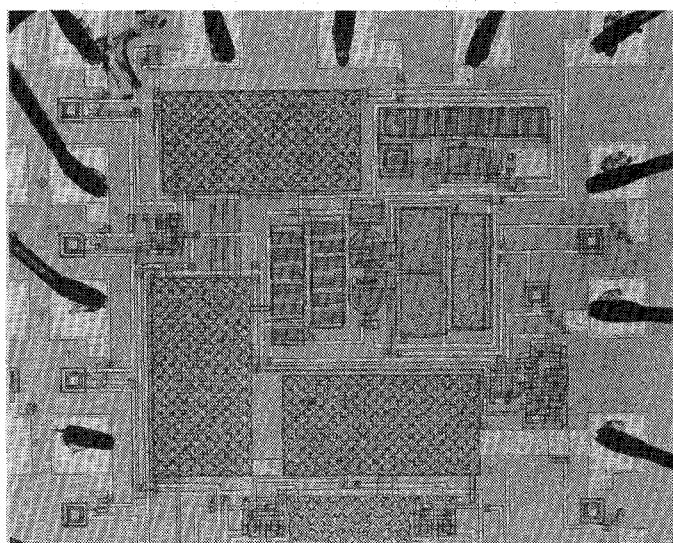


Fig. 5. Die photomicrograph of the switched capacitor integrator.

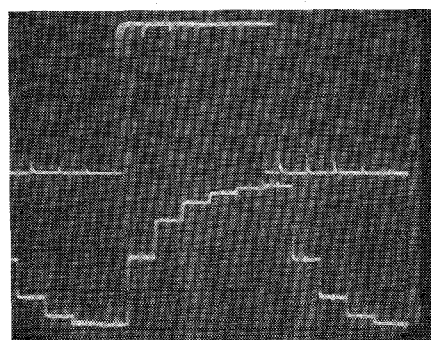


Fig. 6. Scope photograph of the integrator's response to an 8 V square wave. Feedback is used to make a lossy integrator with a time constant of one-half of the clock period. The clock frequency is 30 kHz. The vertical scale is 2 V per division, and the horizontal scale is 50 μs per division.

low-noise buffer amplifier which has a gain of 10. The output of the buffer amplifier is then used as an input to an HP 3582A spectrum analyzer, and the photographs in Fig. 7 are taken directly from its display. These measurements are dominated by thermal (kT/C) noise at frequencies over 250 Hz. The broad-band noise level was 140 nV per root Hz. Over a 10 kHz bandwidth dynamic range is greater than 110 dB. This re-

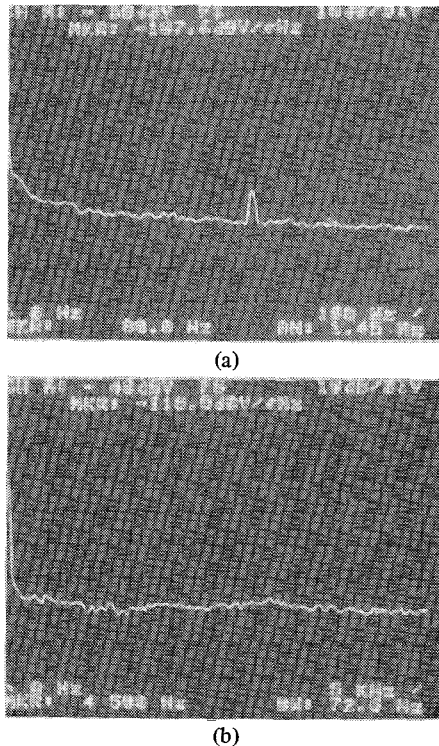


Fig. 7. Experimentally observed noise performance of the integrator through a low-noise buffer amplifier (with a gain of 10). The input referred noise is a factor of 27 lower.

sult compares favorably with the more complex chopper-stabilized techniques which were recently reported [7].

CONCLUSION

Experimental data measured from discrete devices has shown the $1/f$ noise voltage to be inversely proportional to the square root of both frequency and gate area. Also, we see that PMOS devices exhibit 5 times lower $1/f$ noise than equivalent NMOS devices.

Following the analysis given in [3], we have designed and fabricated a low-noise CMOS amplifier using a digital CMOS process. This amplifier has an input referred noise of 130 nV per root Hz at 100 Hz with a die area of only 0.12 mm² and a power dissipation of 1.2 mW.

Using the low noise amplifier we have fabricated a switched capacitor integrator. This integrator has a broad-band noise level of 140 nV per root Hz, and a dynamic range of 110 dB over a 10 kHz bandwidth.

ACKNOWLEDGMENT

The authors would like to thank the many people whose help and cooperation made this work possible. In particular, we would like to thank S. Rung who supervised the initial fabrication, G. Margolieux of Corvallis Division who modified our designs for the production runs, and T. Hubely, also of Corvallis Division, for his help in fabrication.

REFERENCES

- [1] P. Gray, D. Hodges, and R. Broderson, Eds, *Analog MOS Integrated Circuits*, New York: IEEE Press, 1980, p. 28.
- [2] M. Aoki, Y. Sakai, and T. Masuhara, "Low $1/f$ noise of Hi-CMOS devices," *IEEE Trans. Electron. Devices*, vol. ED-29, pp. 296-299, Feb. 1982.
- [3] J. Bertails, "Low-frequency noise considerations for MOS amplifiers design," *IEEE J. Solid-State Circuits*, vol. SC-14, pp. 773-776, Aug. 1979.
- [4] S. Sze, *Physics of Semiconductor Devices*. New York: Wiley, 1969, p. 496.
- [5] R. Rosen, "Silicon on sapphire circuit technology," *Tech. Rep. AFAL-TR-72-401*, Mar. 1973.
- [6] H. Katto, Y. Kamigaki, and Y. Itoh, "MOSFET's with reduced low frequency $1/f$ noise," in *Proc. 6th Conf. Solid-State Devices*, Tokyo, Japan, 1974, pp. 243-248.
- [7] K. Hsieh, P. Gray, D. Senderowicz, and D. Messerschmitt, "A low-noise chopper-stabilized differential switched-capacitor filtering technique," *IEEE J. Solid-State Circuits*, vol. SC-16, pp. 708-715, Dec. 1981.

A Graphical Analysis of the Schmitt Trigger Circuit

ERIC J. DICKES AND DALE E. CARLTON

Abstract—A graphical method for analyzing nonlinear circuits is developed. The method is applied to a common positive feedback example, and leads to an insightful graph of the "voltage gain" of a Schmitt trigger circuit. The closed-form expressions for trip points and hysteresis are found and experimentally verified.

I. INTRODUCTION

The Schmitt trigger is a nonlinear positive-feedback circuit that does not lend itself to linear feedback theory analysis. When solving for the transfer function, one is led to an insolvable transcendental relationship. A graphical expression of this transfer function reveals a path around the impasse by providing a closed-form mathematical description of the trip points.

II. SCHMITT MODEL

Fig. 1 shows the model of the Schmitt trigger circuit in the format commonly found in feedback theory. V_{in} is the input voltage, V_e is the drive voltage, and V_o is the output voltage. As shown,

$$V_e = V_{in} - V_o. \quad (1)$$

Θ is the large signal, nonlinear, inverting gain element of the Schmitt trigger that operates on V_e . Contrary to linear circuit analysis premises, Θ changes with V_e . This dependence upon V_e is accentuated by the positive feedback. [The sign of $\Theta(V_e)$ is negative; see (5).]

$$\Theta(V_e) \triangleq \frac{V_o}{V_e}. \quad (2)$$

The closed-loop transfer function is given by

$$\frac{V_o}{V_{in}} = \frac{\Theta(V_e)}{1 + \Theta(V_e)}. \quad (3)$$

$\Theta(V_e)$ can be expressed in terms of the circuit realization shown in Fig. 2. To start with, V_o and V_e can be related by

Manuscript received April 6, 1982; revised July 19, 1982.
The authors are with Tektronix, Inc., Beaverton, OR 97077.