

6 Gain stages

Negative feedback is effective in reducing low order harmonics and improving linearity at low frequencies, but in general is less effective at high frequencies since stability criteria require loop gain roll-off. Therefore distortion mechanisms that create high order harmonics should be minimized using other means than NFB only. The HF-performance of power amplifiers is often poorly optimized and the distortion level in an amplifier often increases rather steeply with frequency - much more steeply than can be explained by a decrease in the loop gain [80]. The implicit assumption for feedback amplifiers is often that the input error voltage is small and distortion of the input stage negligible. However, distortion remains small only if the input stage signal level remains low, and this is not always the case as shown in Chapter 4.

A steep increase in distortion levels with frequency results from a number of different causes:

- The internal distortion of gain stages increases with frequency because of increasing nonlinear capacitive currents;
- The switching current of a transistor will become more significant and slew-rate induced distortion will increase;
- A decrease in the loop gain will increase signal levels at the input stage.

Whenever HF-performance needs to be optimized or when the loop gain is small, internal linearity will become especially important. Optimization of internal linearity is the best way to construct an amplifier with controlled behaviour at high frequencies when the global negative feedback is much less effective.

This chapter investigates and compares various existing gain stage topologies in order to determine which structures have the best open loop performance. The ways to improve internal linearity as discussed in Chapter 5 are directly applicable to the gain stage topologies presented here.

6.1 *Input stages*

The significance of the input stage is often underestimated in many audio amplifiers - most amplifiers use a simple differential pair as an input stage which have been used for decades. True, the output stage is the main source for low frequency harmonic distortion in many amplifiers, and it also sets limits on maximum output current and power as well

as minimum output impedance related to the loop gain of the amplifier. However, there are several performance parameters which are limited by the input stage performance:

- input impedance;
- dynamic distortion;
- noise;
- PSRR, CMRR;
- slew-rate, bandwidth and loop gain.

When the power stage is properly optimized for linearity, harmonic distortion performance can be limited by the input and VA-stages.

If the amplifier needs to perform well at higher frequencies or if only a moderate amount of NFB is used, the differential input stage should be designed to tolerate a larger input differential. This performance can be improved by using a high tail current, large degeneration resistors and using a cascode or bootstrap topology as presented in Chapter 5. Power consumption and an increase in BJT current noise restricts the use of large bias currents, but maintaining the linearity with lower bias levels would require excessive degeneration that also can lead to increased noise and decreased open loop gain.

There are only a few potential input stage topologies and most of them are well known and have been widely used prior to this work. These topologies are compared here along with a description of some simple design rules. Based on the results of Chapter 5, various improvements to the old topologies are presented along with an analysis of their performance and a comparison with the basic structures.

6.1.1 Differential pairs

The input stage of an amplifier is almost invariably based on the differential transconductance stage. This is true not only in audio amplifiers but also in almost all other voltage feedback amplifiers both integrated and discrete. A differential pair is used even if a differential input is not required, and in amplifiers with or without negative feedback alike.

Only BJT implementations are analyzed in detail in this chapter, but JFET and MOSFET devices can also be used. The BJT has the highest transconductance which can be utilized for local linearization or to achieve a very high gain using relatively simple circuits. The parameters of the two transistors in the differential pair are generally more easily matched when using BJTs than when FET transistors are used. Usually differential pairs can be implemented from discrete BJT devices without matching although significant improvement in offset, input bias current and linearity can be achieved with matching. The BJT input bias current and current noise may become a problem when high input impedances are used, and in such cases FETs perform better, at least close to room temperature where gate current is negligible. One other reason to use BJT transistors is their good availability and low cost, as discrete JFET devices have become obsolete in most applications and discrete MOSFETs suitable for linear audio frequency applications are uncommon.

A differential pair has several advantages over a single transistor. A single transistor amplifier has to be biased with external bias circuitry. This usually requires a DC-blocking capacitor at the input, whereas a differential pair input signal can be referred to ground without DC-offset. CMRR of the differential pair is excellent compared to most other available structures. Earlier amplifiers often had a DC-blocking capacitor at the output of the amplifier, but modern high performance audio power amplifiers have long since been DC-coupled to the speaker and this requires almost zero offset voltage at the output. The differential pair symmetry effectively cancels out offset and thermal drift and this makes it very easy to build DC-coupled amplifiers.

The bias current of the differential pair is defined by the tail current source. This current will create a small base current in the input transistors but the bias current itself does not flow through the feedback network. This simplifies and facilitates feedback network design. High common mode rejection is beneficial if the input signal is differential or if a non-inverting topology is used. Differential pair linearity is superior to single ended structures because symmetry cancels out even harmonics which dominate distortion performance of the single ended amplifier circuits. Finally, the noise performance achievable is excellent because the emitter degeneration resistors can be very small or even omitted.

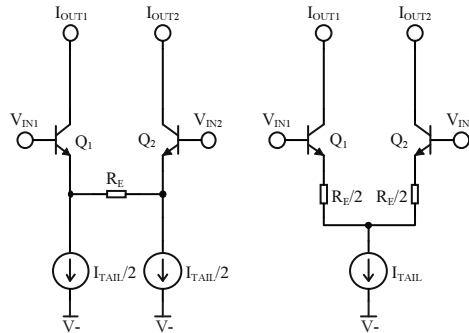


Figure 6.1. Basic differential pair with two or one tail current source.

A basic differential pair is presented in **Figure 6.1** with two current sources and an R_E that, together with transistors, defines the transconductance of the circuit. The two current sources can be replaced with one by doubling the tail current and replacing the one R_E resistor with two resistors with value of $R_E/2$. In the present chapter a single tail current source version will be used throughout.

The differential pair output current $I_{DO} = I_{OUT1} - I_{OUT2}$ without emitter degeneration is related to the differential input voltage $V_{ID} = V_{IN1} - V_{IN2}$ [82] by

$$I_{OD} = I_{TAIL} \alpha_F \tanh\left(\frac{-V_{ID}}{2V_T}\right), \quad \alpha_F = \frac{\beta_F}{1 + \beta_F} \quad (1)$$

where V_T is the thermal voltage (26mV at 25°C), and I_{TAIL} is tail the current. It should be noted that transistor type and current gain have little influence on the circuit performance.

The circuit operates in an approximately linear fashion only when the magnitude of V_{ID} is less than about V_T . When the magnitude of V_{ID} is greater than about $3V_T$, which is approximately 78mV at room temperature, the collector currents are almost independent of V_{ID} because one of the transistors turns off and the other conducts all the available tail current.

A common emitter amplifier's output current is exponentially related to the input voltage, and such a transfer function generates a decreasing spectrum of both odd and even harmonics. A differential pair output current is a hyperbolic tangent of which the Taylor-series expansion is [167]

$$\tanh x = x - \frac{x^3}{3} + \frac{2x^5}{15} - \frac{17x^7}{315} + \dots \quad (2)$$

In this case, assuming that the circuit is perfectly symmetric, only odd order harmonics are generated. This applies only when the exponential relation of collector current and input voltage is assumed, but in practical amplifiers various non-ideal transistor properties, especially early voltage, will cause errors that limit the performance of the differential pair circuit.

6.1.1.1 Emitter degeneration in differential pairs

As noted, a basic differential amplifier works well only if V_{ID} is very small, and this requirement can be met in audio amplifiers only when a high amount of negative feedback is used. Emitter degeneration can be used in a differential pair in the same way as in a single transistor amplifier stage. It reduces transconductance, increases linearity and expands useful input voltage range. However, a simple closed-form equation like (30) does not exist for an emitter degenerated differential pair [82].

The effects of emitter degeneration with different resistance values are presented in **Figure 6.2** and **Figure 6.3**. Figure 6.2 shows the output differential current as a function of input differential voltage; Figure 6.3 is a derivative of Figure 6.2 and shows the transconductance of the same circuit. The linear input voltage range is extended by an amount approximately equal to $I_{TAIL}R_E$, which is of course the voltage across the degeneration resistor [82].

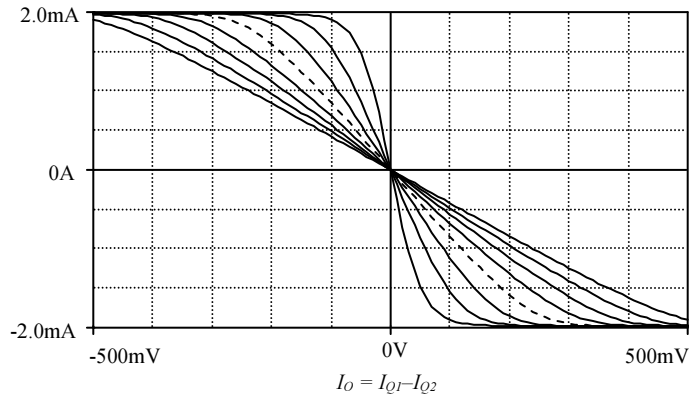


Figure 6.2. Differential pair output current as a function of input differential voltage. Degeneration stepped from 0 to 210 ohms in 30 ohm steps with 2mA tail current. Dashed curve with 120 Ω degeneration resistor.

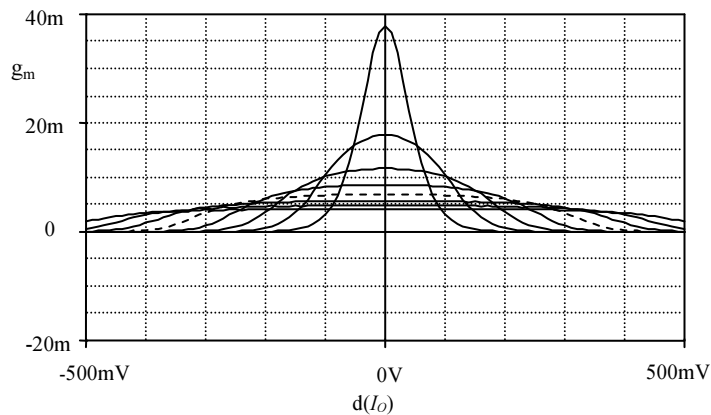


Figure 6.3. Differential pair transconductance vs. input voltage. Degeneration stepped from 0 to 210 ohms in 30 ohm steps with 2mA tail current. Dashed curve with 120 Ω degeneration resistor.

An increase in tail current increases transconductance and makes degeneration more effective, so the same linearity can be maintained with smaller emitter resistors. This can be used to increase the open loop gain of the input stage (and whole amplifier). A higher loop gain means smaller V_{ID} with a closed feedback loop, which further improves input stage linearity. Integrated circuit amplifiers typically use very small tail currents, as in many applications low input bias current and low power consumption are more important than high linearity. **Figure 6.4** shows the variation in transconductance with tail current with a fixed degeneration resistor of 120 Ω .

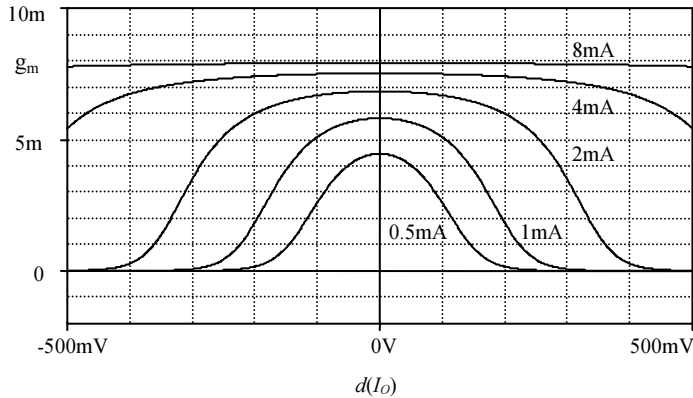


Figure 6.4. Transconductance vs. input voltage for a simple differential pair with different tail currents. Degeneration resistance 120Ω .

Emitter resistance can be the main source of noise in low noise amplifiers, and high tail current is one way to keep emitter degeneration and thus noise small and still maintain high linearity. High tail current increases power dissipation in input stage transistors and for this reason some designers use power transistors in the input stage of their designs. Unfortunately, there are no dual power transistors, so in this case good symmetry requires transistor matching.

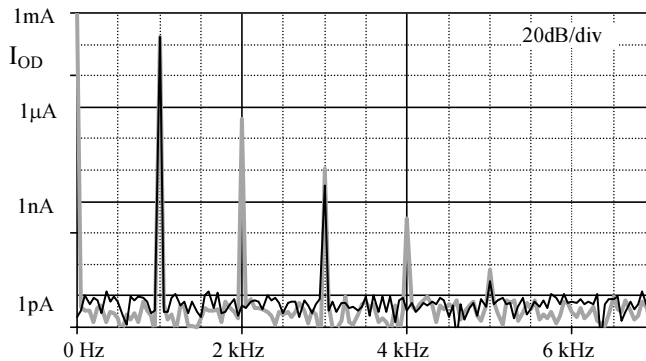


Figure 6.5. Simulation of the BC546B collector current spectrum with single transistor (grey) and perfectly symmetric differential pair (black) with ideal tail current source, constant V_C and differential output.

To a first order approximation, a perfectly symmetric differential stage driven with a voltage source would produce only odd harmonics, as shown in **Figure 6.5**. Here a comparison is made to a single common emitter transistor circuit with the same bias and degeneration as used in the differential pair. Any mismatch in parts spoils this balance of course but nonetheless, with careful design and device matching almost perfect cancellation is possible, especially for low order even harmonics. A differential pair has much less effect on the odd order terms, however. When driven with current or through a source with nonzero output impedance, even order cancellation also takes place, even if

the distortion mechanisms are different. In such a case nonlinear input currents will cause other errors [169].

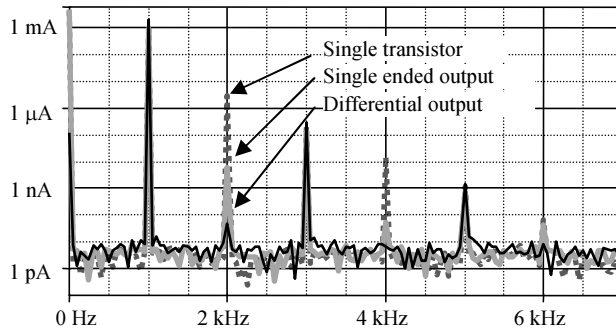


Figure 6.6. Harmonic distortion spectrum with 1kHz fundamental. Single transistor and differential pair with single-ended and differential output signal. 100mV input differential, 8mA tail current and no common mode signal.

The differential pair output signal should also be taken differentially, from the two output branches; however it is often simpler to take only one differential pair branch as an output. In this case total cancellation does not occur, but even harmonics are still reduced compared to the single ended gain stage. Example distortion spectrums are shown in **Figure 6.6**.

6.1.1.2 Differential input impedance of the differential pair

The input impedance of a BJT transistor is in the range of 10 k Ω to 100 k Ω at the usual bias currents of around 1 mA, and decreases as bias current increases. The V_{CE} -voltage also has a small effect on the input impedance. The total differential input impedance of a differential pair can be as low as a few kilo-ohms when used with heavy bias current and without emitter degeneration. This differential input impedance is plotted in **Figure 6.7**. So, to a limited extent, emitter degeneration can be used to increase the impedance. However, when high impedance is essential, JFET or MOSFET devices can be used or the input BJT transistor can be replaced with more complex circuitry.

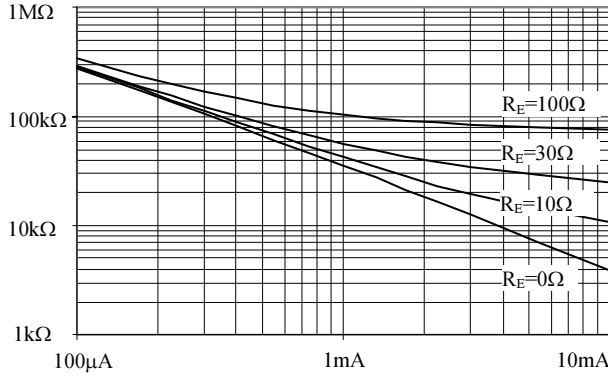


Figure 6.7. Simulated differential impedance between input nodes in a differential pair as a function of tail current.

The input impedance of a feedback corrected amplifier is increased by the loop gain whereas output impedance is decreased by the same ratio. However, the open loop impedances do affect loop gain and distortion. Finite input differential impedance reduces loop gain when the amplifier is not driven from a zero output impedance source as this will attenuate the signal. The decrease in loop gain is approximately the ratio between the source impedance and the impedance between the input nodes and the feedback network resistors should also be included in the calculation when accurate results are required. For example, a volume control potentiometer at the input has typically a value of tens of kilo-ohms and can reduce loop gain from few decibels to 20 dB, which is a radical change. This should be taken into account in designing the loop compensation for the amplifier.

The finite impedance between the two input nodes also creates a path for unwanted signals from the amplifier output back to the input. For example, a nonlinear speaker load will affect the output of the amplifier and its non-linear effect may back-propagate through the previous stages back to the input stage.

6.1.1.3 Common mode voltage and bootstrapping

Although differential pairs are generally biased with one or two current sources, these can be replaced with a simple resistor for simplicity and cost considerations. When the circuit is perfectly symmetrical, the actual tail current source or resistor does not affect differential signal gain or distortion. This is because a differential signal does not affect the voltage across the tail current source/resistor.

A common mode signal on the other hand appears directly across the tail current source. The impedance of the current source can be seen as degeneration or local feedback for common mode signals. With bipolar transistors this can be calculated as [82]

$$A_{CM} \approx -\frac{g_m R_{LOAD}}{1 + 2g_m R_{TAIL}} \quad (3)$$

Since DM gain of the differential pair is

$$A_{DM} = \frac{v_{od}}{v_{id}} = -g_m R_{LOAD}, \quad (4)$$

CMRR can be calculated as

$$CMRR = 1 + 2g_m R_{TAIL}. \quad (5)$$

Supply voltage ripple can also be seen as a common mode signal so that an increase in CMRR will also increase PSRR of the supply where the current source is referenced to. In addition to these small signal effects, large signal parameters, especially Early-voltage, also affect CMRR performance. The Early-effect is dominant, when high impedance current sources are used; it decreases CMRR but also increases distortion since the output impedance is nonlinear.

Any deviation from perfect symmetry decreases CMRR and causes a CM-signal to be converted to a DM-signal, which generates distortion, predominantly 2nd harmonic. Its effect can be minimized by loading the differential pair symmetrically. Resistor loading with a single ended following stage would cause all the CM-signal to be converted to a DM-signal. In addition any source impedance imbalance will also create distortion from both CM-signals and power supply ripple. The topic of CM-signal induced distortion is analyzed in [170].

Common mode voltage is present in differential pair inputs whenever a non-inverting feedback topology is used. A typical line signal level is about 1V_{RMS}. In contrast, an inverting topology creates a virtual ground at the inverting input terminal and zero-feedback inverting amplifiers have a CM output signal only if there is a CM-error at the input. Even if the amplifier is intended to be used in the inverting configuration, degraded performance in the presence of a common mode signal may be a symptom that the circuit topology in question has thermal problems.

Certain amplifiers suffer from common mode signals much more than others. Analog Device's AD797 operational amplifier is an exceptionally low distortion amplifier as long as there is no common mode input voltage. But a CM-signal at the input decreases the performance more than it does with most amplifiers [171].

The Early-effect in a transistor is most effectively reduced with bootstrapping. Cascoding (**Figure 6.8 a**) has no effect here since it does not decrease CM-signal voltage across the input transistor. In many cases, however, cascoding is beneficial in keeping input transistor dissipation low and in allowing the use of more suitable high speed, high gain devices which would not otherwise necessarily tolerate the high supply voltages of the circuit. A common mode bootstrap circuit is presented in **Figure 6.8 (b)**. The differential mode voltage remains constant across the tail current source, and only the common mode input voltage is bootstrapped. The impedance of the current source is much higher than the emitter degeneration, thus the emitter degeneration resistor has very little effect on the CM-bootstrap operation.

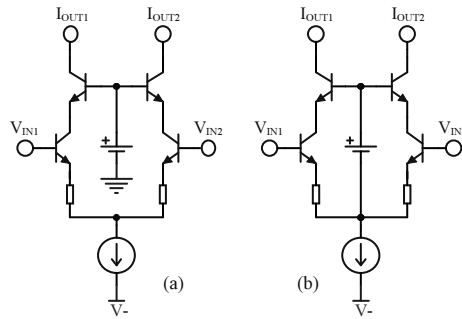


Figure 6.8. Cascode (a) and common mode bootstrap circuit (b) in differential pairs.

The effect of a CM-input signal on the distortion performance is shown in **Figure 6.9**. Even if even order harmonics are not perfectly cancelled with a simple bootstrap circuit, the residue is usually small enough to be masked by the distortion from the balance error. Clearly bootstrapping does not affect the third harmonic since the CM-signal creates only even harmonics.

When only the common mode signal is considered to be a problem, CM-bootstrapping is effective. When both transistors are bootstrapped separately, the Early-effects from both differential and common-mode signals are cancelled, and differential bootstrap circuits are presented in **Figure 6.10**. Differential bootstrapping is applicable to all the bootstrapped single transistor circuits presented in the previous section. But differential signal compensation will make only a marginal improvement to performance if the amplifier is designed to have high loop gain and low input differential at all times, as in a wideband feedback amplifier.

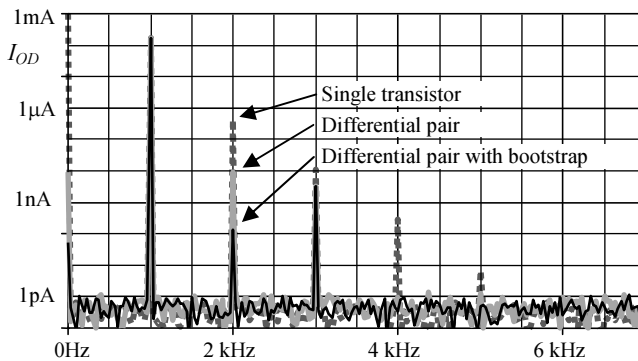


Figure 6.9. 2V CM- signal and 20mV DM-signal in a differential pair with perfect symmetry and ideal tail current source. Comparison is made to a single transistor common emitter circuit with 20mV input signal.

CM-bootstrapping is quite simple to bias and has much less effect on differential signal or gain. Since the voltage across the tail current source remains constant with a

differential input signal, CM-bootstrapping can be directly connected to the current source as in Figure 6.8 (b). If the bootstrap circuit bias current is not perfectly constant, the error is common mode and has little effect on amplifier performance. Usually the bias current supply can be simplified as one high value resistor connected to the supply line. DM-bootstrapping on the other hand requires much more attention to filtering and matched bias currents - a difference in bias currents between the two input branches will create an offset voltage and partially transform a CM-error into a DM-signal. A high value matched resistor pair connected to a filtered reference voltage or matched current sources should be used for optimal performance.

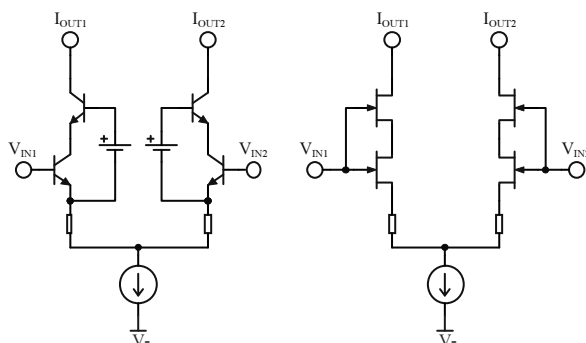


Figure 6.10. Differential bootstrap circuit examples.

When CM-bootstrapping is used, the base current will cause an error with a BJT implementation. In a differential mode bootstrap, the bootstrap transistor base current is subtracted from the emitter of the common emitter transistor, as discussed in Chapter 5. The effect of the base current is cancelled at the collector of the common base transistor. In CM-bootstrapping this cancellation does not occur. So to be effective, in this case the base current has to be minimized.

A single BJT can be replaced with a Darlington-circuit. Also, JFET and MOSFET devices are both suitable since they draw negligible gate current although they have lower transconductance than BJT devices, making them less effective as buffers.

JFET circuits do not necessarily need any extra biasing components unlike BJT and MOSFETs. The best-suited component to create a bias voltage is a high brightness LED which has low noise and a low dynamic impedance. Biasing of the LED could be done with a resistance tied to a reference voltage or some current source circuit of which the simplest one is a single JFET.

In **Figure 6.11**, the CM-signal performance of a simple differential pair and the common mode bootstrapped version is compared, with various tail current source impedances. Bootstrapping cannot compensate tail current modulation thus the CM-current remains almost the same with and without bootstrapping. As is clear from Figure 6.11, bootstrapping reduces direct capacitive feed-through and Early-voltage errors of the input transistors, improving performance at high frequencies when a high impedance tail current source is used.

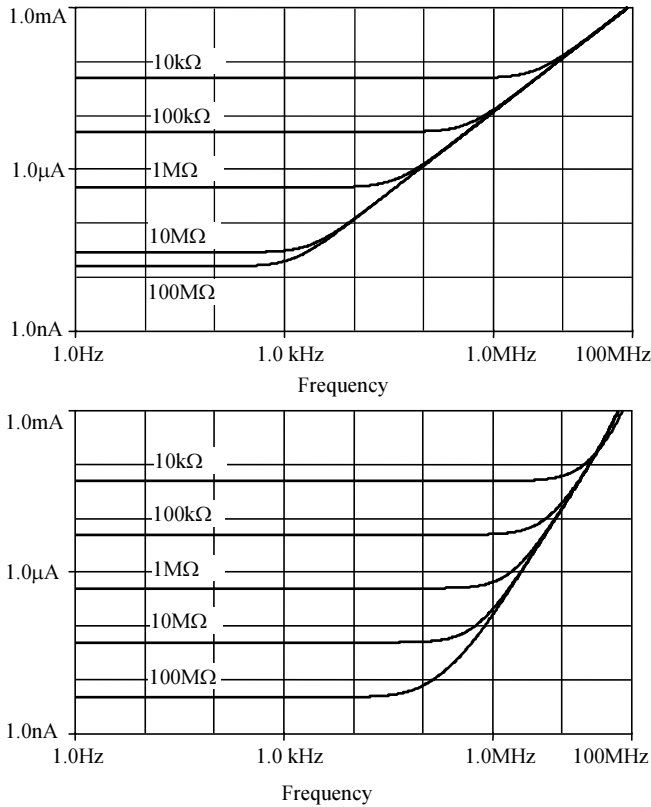


Figure 6.11. Effect of common mode input voltage on collector current with different values of tail current source output impedance. Basic differential pair in upper graph and common mode bootstrapped version in lower graph.

6.1.2 Device matching

Differential pair performance is mainly based on symmetry, and a mismatch in any parameter like V_{BE} , temperature, collector current, degeneration, current gain, output voltage etcetera degrades performance. In many analog applications DC-performance is important and close tolerances are required for small offset voltages and currents, but in audio applications even 100 mV offset voltage at the power amp output can be tolerated. The effect of component mismatch on offset voltage has been discussed extensively in the literature on analog electronics and analog IC-design, such as [82].

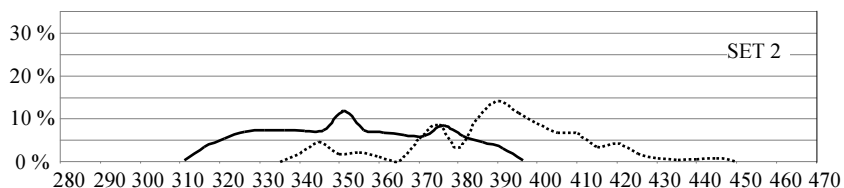
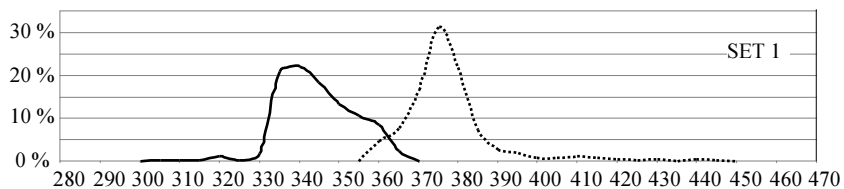
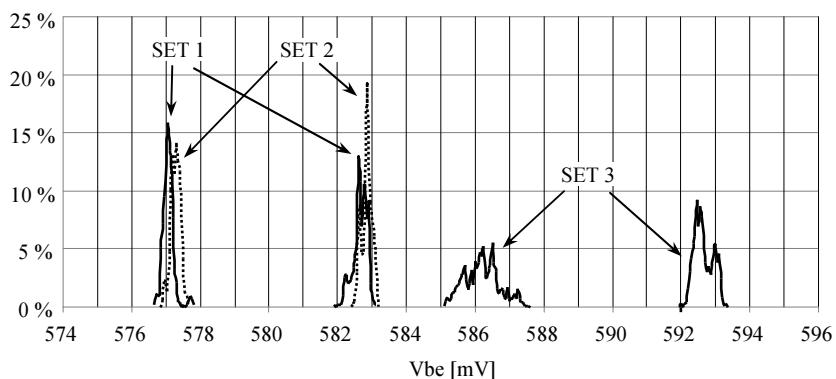
Cancellation of even order terms is roughly proportional to the achieved balance. The second harmonic is decreased about 20 dB when balance error is 10% and 40 dB when balance error is 1%. CMRR in differential pairs is not based on a balance condition, however, common mode voltage conversion to differential mode voltage is a mismatch-induced problem. In addition, thermal errors and thermal DC-drift are effectively

cancelled when input transistors are kept at same temperature and have similar parameters.

It is virtually impossible to reach the same symmetry using discrete components as can be achieved with single chip dual matched transistors. Unfortunately there is a somewhat limited selection of dual transistors and they are very expensive compared to general purpose single transistors. A high quality matched transistor pair can cost as much as all the small signal active devices together in a cost optimized discrete power amplifier.

Discrete transistor matching is usually done to V_{BE} -voltage and possibly to current gain. By using a transistor from the same batch V_{BE} -voltages are usually within few millivolts whereas matched dual transistors are available with less than 0.1mV V_{BE} difference. Since the PN-junction temperature coefficient is about $-2\text{mV}/^\circ\text{C}$ the matching process should be performed at a very accurately controlled temperature. As temperature coefficients are similar between devices it is not necessary to match them at the same temperature at which they eventually will operate.

To achieve the same symmetry that is available with matched pair transistors, the temperature during the matching measurements should be within 0.05 degrees, and this requires equipment that is special-built to analyze transistor performance.



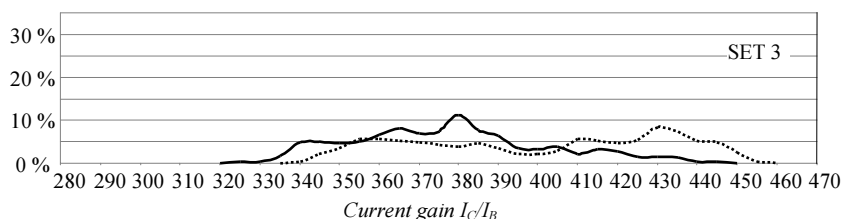


Figure 6.12. Histograms of V_{BE} -voltage (top) and current gain (lower three graphs) of three sets of BC546B/BC556B transistors. Each set contains about 500 transistors; measured at $V_{CE} = 3V$ and $I_C = 1\text{ mA}$

A few sets of transistor measurements are shown in **Figure 6.12**. Each set contains approximately 500 transistors, which are measured at a calibrated constant temperature with 1 mA collector current and 3 V_{DC} collector-emitter voltage. The transistors were acquired from various dealers. Two of the sets are clearly very similar and both have very similar V_{BE} and current gain histograms. The third set, however, has a very different V_{BE} compared to the other two, and also very different current gain variation. Transistors within the same batch can be rather similar, with V_{BE} typically within 1 mV based on the measured transistor sets. Greater variation is, however, possible as can be seen from the third set. When new amplifiers are designed, it should be validated that the performance of amplifier remains within specification whenever the transistor batch is changed. Transistor matching may be impossible with some transistor sets while there are other sets containing plenty of transistors with close to identical parameters.

6.1.3 Methods to improve differential pair linearity

Many discrete audio amplifiers rely on high feedback to keep input stage distortion low, but as noted before, this may result in poor dynamic behavior and high distortion at high frequencies where the effectiveness of the NFB diminishes. Poor internal linearity also increases the amount of high order complex distortion products in the system output, which are also less effectively decreased by NFB.

Internal linearity can be enhanced simply by using a large bias current and/or by using degeneration resistors. Degeneration comes at the expense of the noise factor but a small increase in noise level is acceptable in most cases. In simple amplifiers, degeneration may reduce loop gain more than it improves inherent linearity, so when only THD is analyzed in such amplifiers, increasing degeneration may result in an increase in both noise and THD.

Any unbalance and mismatch in differential pair currents or voltages will produce even harmonics. These can be effectively reduced by using matched transistors and passives with tight tolerances as discussed earlier.

More complex input stage circuits are uncommon in discrete amplifiers but are widely used in integrated circuits. High speed circuits, in particular, require inherently more

linear topologies since it is not possible to use high amounts of feedback to correct the errors.

6.1.3.1 Error Feed Forward and Error Feed Back (EFF, EFB) correction in differential pairs

Input stage linearization circuits based on local feedback or error correction feedforward techniques can provide effective stage linearization with an acceptable increase in noise and with little effect on input stage speed. Hawksford has listed several circuits that use error feedforward and error feedback topologies to cancel V_{BE}/I_E -nonlinearity [172]. Two of these are the Cascomp and the Cross-quad, and are presented in **Figure 6.13**.

Cross-quad circuits can often be found in HF and multiplier circuits [173]. The assumption in these circuits is that the paired transistors have near identical I_C/V_{BE} nonlinearities. This type of linearization can be considered a form of error feedforward. If the base current is assumed to be zero, $I_{C1}=I_{C2}$ and $I_{C3}=I_{C4}$ resulting in $V_{BE1}=V_{BE2}$ and $V_{BE3}=V_{BE4}$. It follows that the voltage difference across the emitter degeneration resistors is always the same as the input differential voltage, whatever values I_{C1} and I_{C3} may have.

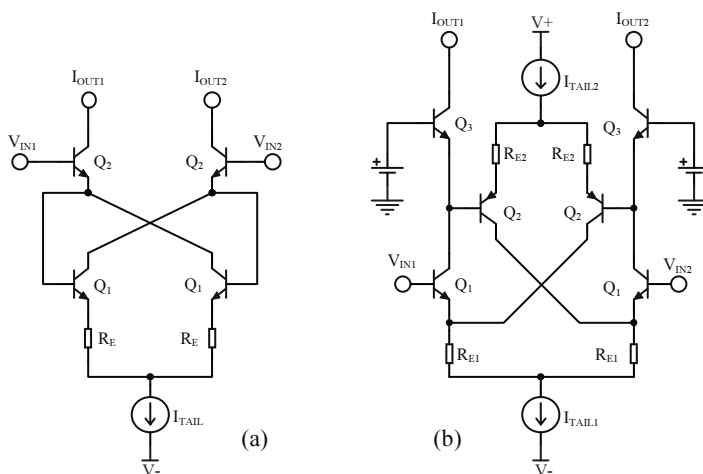


Figure 6.13. Cross-quad circuit (a) and cascomp circuit (b).

The Cascomp circuit assumes an identical I_C/V_{BE} performance of the paired transistors, but uses an external error amplifier to measure the V_{BE} -difference. Since the current of $Q_3 \approx Q_1$ the error can be measured at the emitters of Q_3 . This error signal can be added to I_C -currents to make it error feedforward or summed with the emitter current as a form of error feedback correction. The cross-quad circuit requires no extra bias current sources, but the cascomp requires at least one extra current source and at least four extra transistors. For proper operation, gain should be adjusted to unity. The exact value of the error amplifier's emitter resistors depends on the bias current since it has an effect on transconductance. Also, attention should be given to the exact value of the bias current

and its temperature stability; if the current source is designed to be accurate, resistor trimming is unnecessary even in discrete amplifier applications.

The cross-quad circuit may have stability problems if the input impedance level is high. In IC-applications transistor matching is of no concern but in discrete amplifiers transistor matching is necessary to some extent for improved performance, but transistors selected from the same batch will usually be adequately matched.

6.1.3.2 Using the CFP in differential amplifiers

A Complementary Feedback Pair (CFP) is based on local NFB. This has some advantages over error correction methods that are based on balance, as transistors need not be matched. Source impedance does not affect operation nor do temperature differences, at least to the same extent as it does not affect operation with the error correction methods that are based on balance. Input bias current is very constant and when used with bootstrapping, power dissipation also remains constant, and the impedance between the input nodes also remains very high. This makes it possible to drive the amplifier through relatively high source impedances without a significant decrease in loop gain or without propagating nonlinearities at the amplifier output back to the preceding stages.

The linearity of a simple CFP structure is not as good as that of a cross-quad or a cascomp. However, it is simpler to design than a cascomp and does not have the input impedance problems of a cross-quad. With the enhancements described in Chapter 5, a CFP can be made very linear. The basic differential pair input with CFP is presented in **Figure 6.14 (a)** and the principle of one possible enhanced CFP circuit is shown in **Figure 6.14 (b)**.

For proper operation, the CFP circuit should always be well biased. Especially when a current source version is used, the input voltage difference should not decrease either branch currents near zero since this can upset bias voltages and lead to a long recovery time. A CFP is a high speed feedback structure so oscillations are possible and even likely if the circuit is not properly designed. Small capacitances over the current source are usually necessary and it is advisable to keep output voltages constant with a cascode or with a constant voltage current mode intermediate stage.

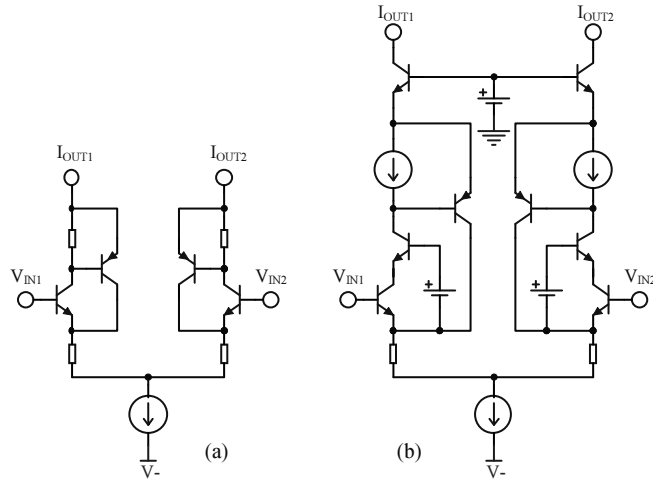


Figure 6.14. Using a CFP in a differential pair. Basic CFP structure and novel high feedback version with bootstrapping and current sources.

The linearity of various input stage topologies are presented in **Figure 6.15**. The basic differential pair, even if heavily degenerated and with an uncommonly high bias current, has poor linearity compared to the enhanced topologies. Enhanced CFP structures are very linear until the signal is clipped.

In systems where the input signal level always stays below a few millivolts or a few tens of millivolts, any linearization method can be used to improve input stage linearity. However, if the circuit is intended for use without global negative feedback or with very low loop gain, the current source enhanced CFP is especially useful.

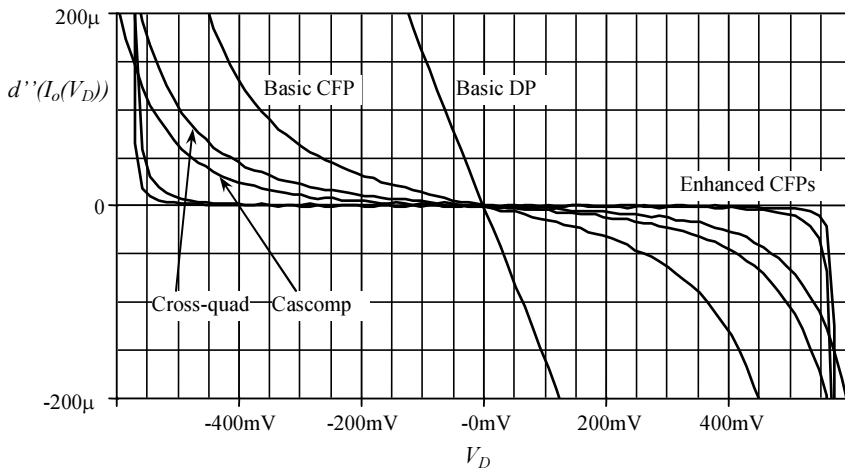


Figure 6.15. Second derivative of the output current. All circuits have 8mA tail current and 100Ω degeneration. The Enhanced CPF utilises current source biasing and bootstrapping as in Figure 6.14 (b).

6.1.3.3 Using JFETs in differential amplifiers

JFETs have significantly lower transconductance and their parameters vary over a much broader range than those of BJTs. It is often assumed that JFET differential amplifiers are more nonlinear than BJT amplifiers - that may be true in certain cases but the difference is small, at least when matched transistors are used. In the experimental input stages tested here, the JFET input stage produced about 10 dB lower THD than the corresponding BJT input stage. The result was, therefore, the very opposite of what was expected; the noise level was also considerably lower. In addition, because JFETs do not draw gate current, there are no DC offset errors caused by differences in input impedances. However, there are only a few JFETs that can drive more current than a few milliamps so JFETs are useful only in input stages.

In some input stage topologies a JFET topology might produce a smaller component count because a BJT topology always requires current sources that may be omitted in JFET applications allowing higher current driving ability and symmetric high slew rates.

A JFET has much lower current noise than a BJT. However, for normal audio use, the output impedance of the preceding stage is typically less than 1k Ω . In these circumstances noise voltage generated from current noise is typically significantly less than thermal noise from the resistances of the amplifier, but with high input impedance a JFET input device may result in lower noise.

6.1.4 Complementary symmetric input topologies

The input stage symmetry can be further improved with a complementary symmetric structure. The linearity of the input stage sections themselves is not significantly improved; however, improved symmetry does make it easier to implement linear push-pull voltage amplifier stages (VAS). The structure is essentially two complementary differential pairs connected together as shown in **Figure 6.16**. Simple input stages require that the input stage is loaded differentially. However, most circuits load the input stage asymmetrically. Since complementary differential pairs work in opposing directions, asymmetric errors are effectively cancelled even if the individual differential pairs are not loaded symmetrically. The PSRR of the amplifier is also improved when a complementary input stage is used.

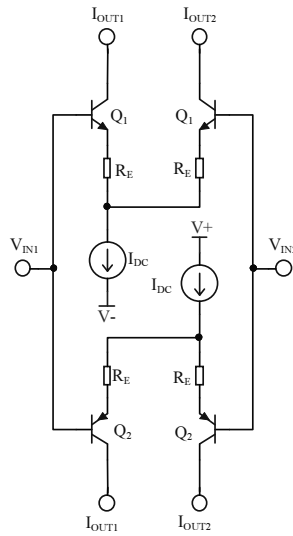


Figure 6.16. Complementary symmetric differential input stage using BJT transistors.

Offset is partially cancelled because of improved symmetry and partially because of decreased input bias currents: When BJTs are used and their current gain is matched between NPN and PNP pairs, the base currents flow between the transistor bases and the input current becomes zero as $I_{IN} = I_{BQ1} - I_{BQ2}$. When the transistors are matched $I_{BQ1} = I_{BQ2} \rightarrow I_{IN} = 0$. For example: 10 k Ω input impedance mismatch would create about 30 mV input offset voltage in a single differential pair amplifier when $\beta = 330$ and $i_C = 1$ mA. With the same input mismatch, a complementary symmetric structure with a 1% mismatch in PNP and NPN betas would produce only 0.3 mV offset.

Mirrored differential pairs can also be connected together using a resistor R_D between them as shown in **Figure 6.17**. This topology was proposed by Stochino as a means of increasing slew rate [174]. Whereas the tail current sets the limit for maximum output current of the single differential pair, the added resistor allows current to flow between the upper and the lower pair and the circuit will then operate in class-AB instead of class-A like the conventional differential pair. Slew rate is improved without increasing tail current and since the output is not clipped with high input levels, transistor saturation is prevented reducing recovery time from amplifier overdrive [176].

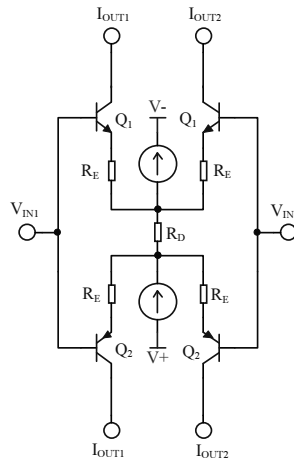


Figure 6.17. Mirrored input stage can be converted into a class-AB push-pull stage with a resistor R_D [174]. The resistor prevents transistor saturation with large input differentials.

Proper biasing of the differential pair transistors can also be achieved by inserting bias voltages at the transistor bases. In that case current sources can be excluded and the differential pairs can be connected together directly from the emitters as shown in **Figure 6.18 (a)**. Biasing is usually performed with two emitter followers as shown in **Figure 6.18 (b)** or with diode connected transistors. The circuit in Figure 6.18 (a) is sometimes called a diamond differential circuit [175]. In this case R_D is usually omitted and R_E degeneration is adjusted so that the desired transconductance is achieved. Even if the circuit has no tail current sources it still has excellent common mode rejection and linearity.

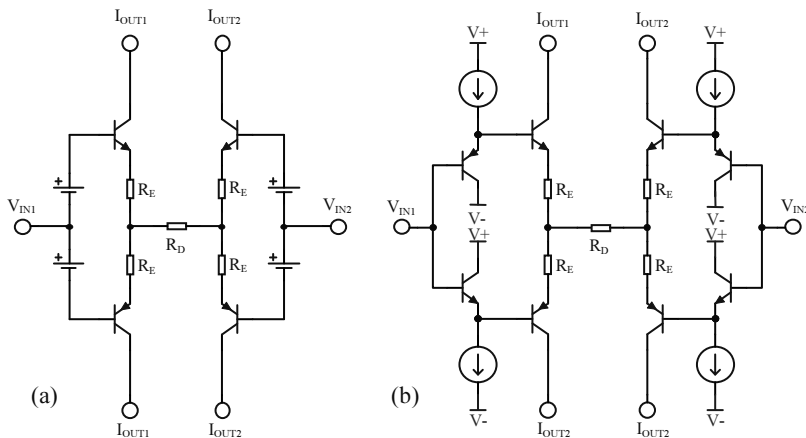


Figure 6.18. Class-AB complementary symmetric input stage.

The extra biasing is not needed when JFET devices are used in a complementary symmetric structure. If suitable low current JFETs are chosen, they can even be directly connected as shown in **Figure 6.19 (b)**. By selecting higher current JFET devices transconductance and maximum output current can be increased. In this case source degeneration has to be used to adjust quiescent bias current (**Figure 6.19 (a)**). Degeneration also improves device matching [177], which is usually poor with JFET devices.

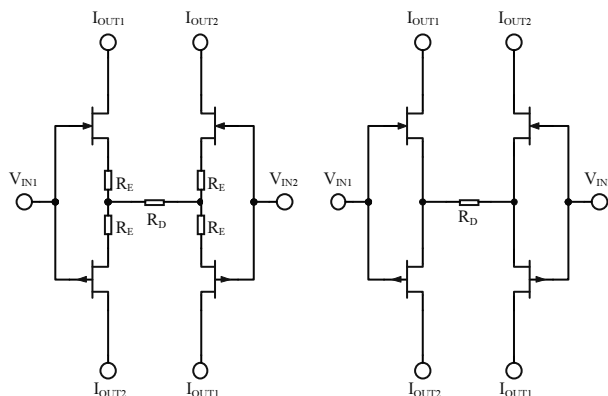


Figure 6.19. Symmetrical JFET input stages. The JFET structure does not need biasing because of the negative gate to source voltage. Bias can be set by the degeneration resistor value or by selecting FETs which have suitable zero gate voltage quiescent drain current.

A differential pair can be thought of as two single ended buffers connected together from the emitters; this is especially evident with the differential pair version with two current sources like that in Figure 6.1 (a). A diamond circuit can be seen as two push pull emitter followers connected together from their outputs. While a normal differential pair can be loaded from one branch only, the push-pull input setup has two push-pull outputs. Either of the two opposite collectors can be used as push-pull output or all four collectors as a differential push-pull output. A single push-pull-stage is conventionally used as an input stage in current feedback operational amplifiers as, for example, in [178]. Resistor R_D in Figure 6.17 converts the conventional complementary symmetric circuit to a push-pull circuit.

A Miller-compensated NFB amplifier will require rather high currents from the input stage to avoid slew rate limiting. In diamond-type circuits, the tail current is not limiting the maximum output current and the input stage is not clipped with high input amplitudes, so slew rate is increased and input stage transistor saturation is prevented.

A diamond differential pair is often used with four equal-sized degeneration resistors with no R_D . The circuit is thus used as if it were two interconnected differential pairs. However, distortion performance is not optimal this way and linearity can be further enhanced. This is done by minimizing R_E and maximizing R_D (Figure 6.19 a). The reason for this is that the push-pull stage is most linear when the emitters are directly connected. Any extra impedance between the emitters will decrease transconductance

and cause distortion, commonly called g_m -doubling distortion; this is analysed in greater detail in Chapter 7.

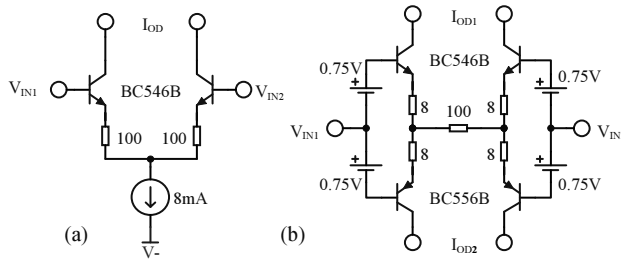


Figure 6.20. Circuits used in the simulations for Figure 6.21 and Figure 6.22. I_C in both circuits is 4mA.

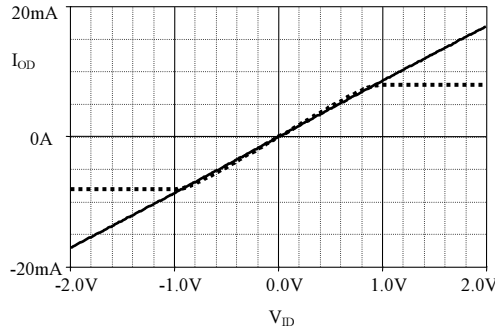


Figure 6.21. Output current vs. input voltage in a conventional differential pair (dotted) and in a class-AB symmetric differential pair (solid).

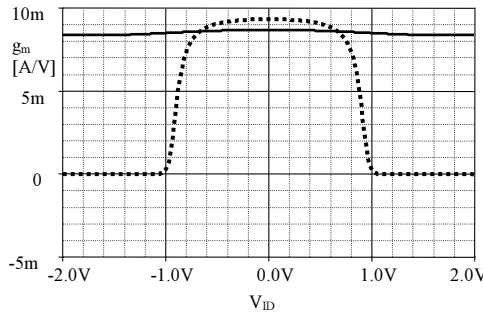


Figure 6.22. Transconductance of the conventional differential pair (dotted) and the class-AB symmetric differential pair (solid).

Simulation results of the circuits in **Figure 6.20** are presented in **Figure 6.21** and **Figure 6.22**. Small signal performance is similar with push-pull input stages and conventional differential pairs. With high input differential levels the contrast becomes clear. The differential pair is saturated at around 1V peak whereas the push-pull will continue to

work with only a shallow bend in the transfer curve at the point where it ceases to operate in class-A. Moreover, at lower signal levels the push-pull stage usually also outperforms a differential pair in linearity. In the case of perfect symmetry and zero CM-signal, both input stages can totally cancel even harmonics though the push-pull input stage is clearly superior with odd order harmonics, **Figure 6.23**.

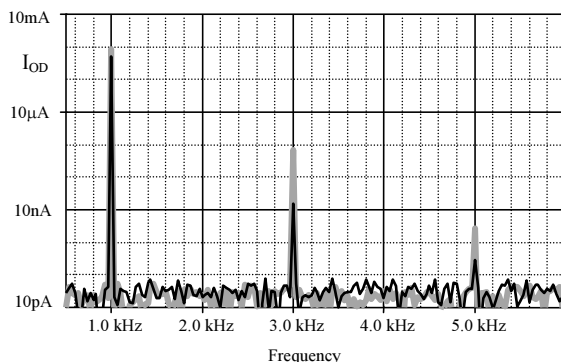


Figure 6.23. Comparison between complementary symmetric differential pair (grey) and diamond connected input stage of Figure 6.20 (black). Both have 2mA branch current and largely equal transconductance. Input signal level 50mV with no common mode signal.

Figure 6.24 shows the changes in the transfer characteristic with various R_E/R_D ratios. Transconductance remains the same provided that the sum $R_E + R_E + R_D$ remains constant. While both transistors are conducting, transconductance is twice as large as it is with large signals when only one transistor from the push-pull stage is conducting. The input stage usually operates in the region where all transistors are conducting, in other words in class-A. The g_m -doubling problem in the push-pull case is minimized by increasing its transconductance and using as large a load as possible between the two branches. Quiescent current stability must be considered when selecting R_E . The variation in push-pull transconductance with R_D can be seen in **Figure 6.25**.

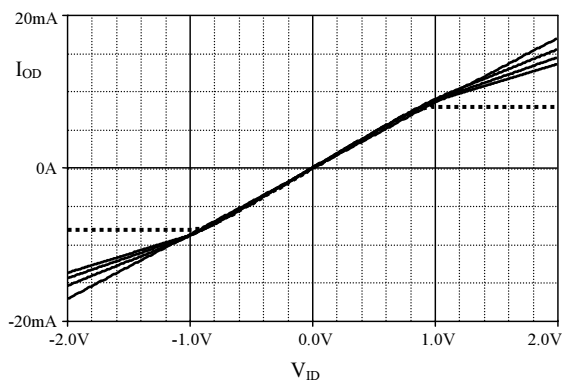


Figure 6.24. Transconductance of the circuit of Figure 6.20 (b) with 4mA I_C with following (R_E , R_D) values: (100Ω, 0Ω), (75Ω, 25Ω), (50Ω, 50Ω), (8Ω, 100Ω). Dotted reference curve with standard differential pair with 8mA tail current and 100Ω emitter resistors. The most linear curve is achieved with the $R_E = 8Ω$ and $R_D = 100Ω$

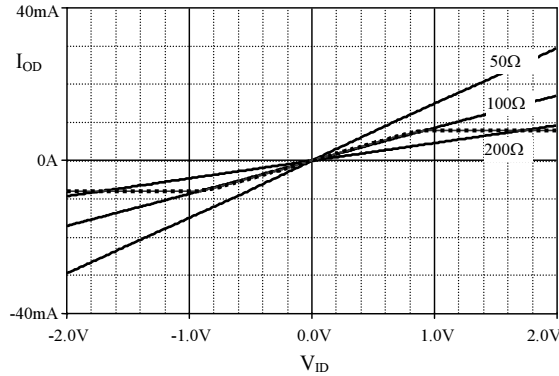


Figure 6.25. Transconductance with $R_D = 50\Omega$, 100Ω and 200Ω , $R_E = 8\Omega$, $I_C = 4.0\text{ mA}$. Dotted reference curve for standard differential pair.

A diamond-connected push-pull input stage is especially suited for amplifiers using low or zero feedback. The use of JFETs in a diamond circuit is attractive because the input biasing structures that are required with a BJT circuit can be omitted, which is an advantage as it is difficult to maintain high linearity and low noise with complex input bias structures. When JFETs are used, the output current is limited by the JFET maximum current. This problem can be eliminated by using a CFP where the JFET current is kept small and relatively constant as in **Figure 6.26**. The enhanced constant power transistor circuits presented in Chapter 5 are especially well-suited for diamond circuits and for use in zero global feedback amplifiers.

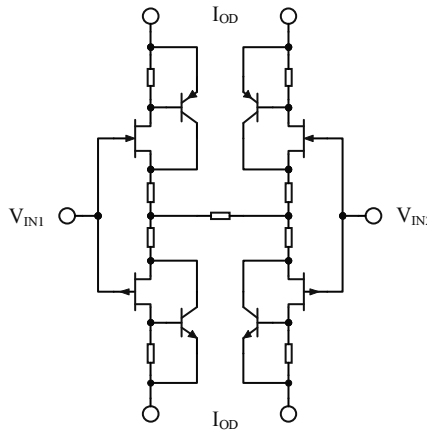


Figure 6.26. Push-pull JFET input stage with CFP.

6.2 Intermediate stages

A conventional audio power amplifier consists of an input stage, an intermediate stage and an output stage. The input stage is conventionally the transconductance stage. The intermediate stage is either a voltage amplifier or a transresistance amplifier. Most of the