4.3.3 Alternative Simple Circuit Level Macromodel

The general transistor level architecture of the CFOA is shown in figure 3(a). The design is typical of most CFOAs and the main sections can be identified as two dual complementary common-collector voltage-followers, linked by two complementary current-mirrors, shown schematically in figure 3(b). The primary source of errors in the simplified macromodels shown in figure 2 are associated with the idealised unilateral input and output buffer stages. In reality these stages of the CFOA are both 'Darlington like' dual common-collector emitter-followers, as seen from figure 3(a). Thus a more realistic but still relatively simple circuit level macromodel than those shown in figure 2 can be constructed using a T-equivalent circuit to represent each common-collector buffer stage. This proposed new macromodel is shown in figure 4.

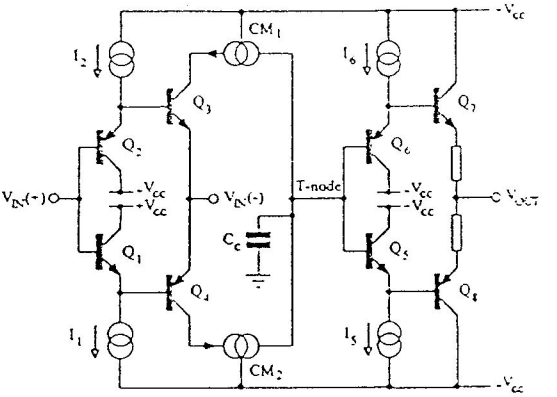

Figure 3(a) Transistor level schematic of the CFOA

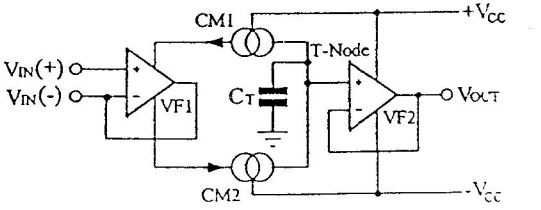

Figure 3(b) Simplified schematic of the transistor level CFOA