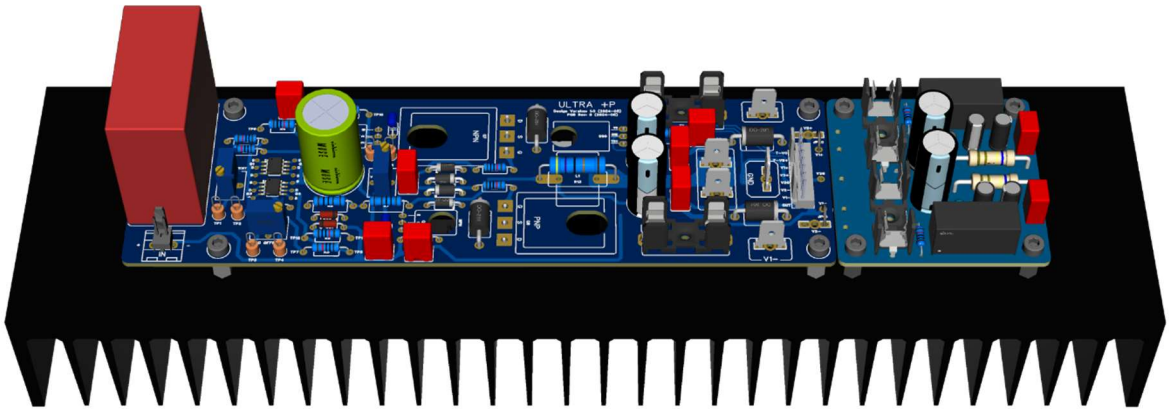
ULTRA +P Power Amplifier

Build Guide
Version 2
(2024-09-20)



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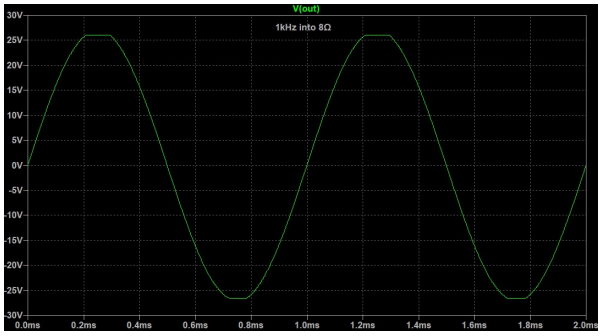
1. Introduction

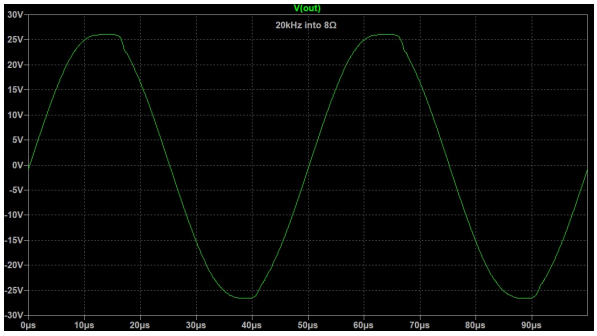
The Ultra +P is a three-stage audio power amplifier running in class AB with a large class A region. It features a simple complementary topology with a JFET input stage, and a lateral MOSET output stage driven directly from the VAS.

This design was introduced by diyAudio user lineup and further refined by user Brian92fs with input from user Benpe. The thread discussing the design can be found on DIYAudio [1]. The changes implemented from lineup's original design all intended to increase stability and address issues with device selection. The stability changes specifically address thermal, and DC offset stability. The results have been confirmed with bench testing, resulting in an observed DC offset drift of less than 5mV and bias drift of less than 10% from cold to hot states. In addition to these changes, this version of the design allows for the IPS/VAS stages to run at higher rail voltages (V2 PSU). The advantages of this are discussed in section 5.1.2.

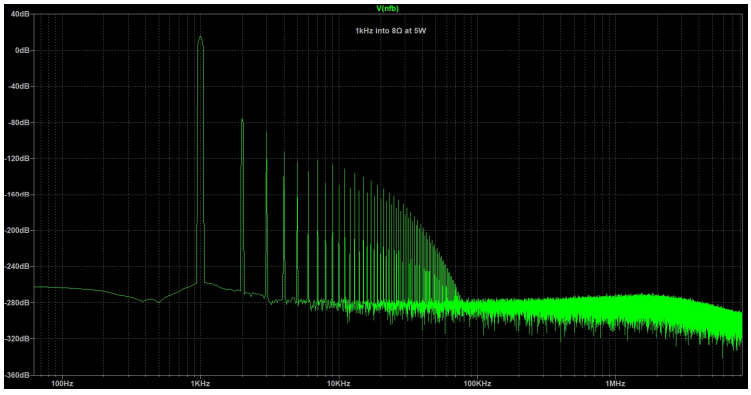
The "+P" suffix to the "Ultra" name describes the higher rail voltages this design utilizes, versus Lineup's original design. Additional power is also obtained from boosted IPS/VAS rails that allow the lateral MOSFETs to swing closer to the rails without incurring additional dissipation that higher main rails would produce.

The single pair complementary VAS produces a clean clipping effect with minimal rail sticking. Not as soft as a triode, but "softer" than other solid state VAS topologies with more devices and more open loop gain.





The distortion spectrum is low order with second and third order being most significant. Second-order distortion is dominate at lower power levels with third order taking precedence as power levels increase.



At the recommended 600mA of bias from 30V main rails, this amplifier will produce approximately 40 watts of output into 8Ω loads with the first 6 watts in class A. Refer to section 5.6 for further discussion on output stage bias settings.

The boards have been designed to work within a Modushop Dissipante 2U 300mm deep chassis.

Note that the gain of this amplifier is relatively low at 15.6dB. A preamp with gain may be needed to drive it.

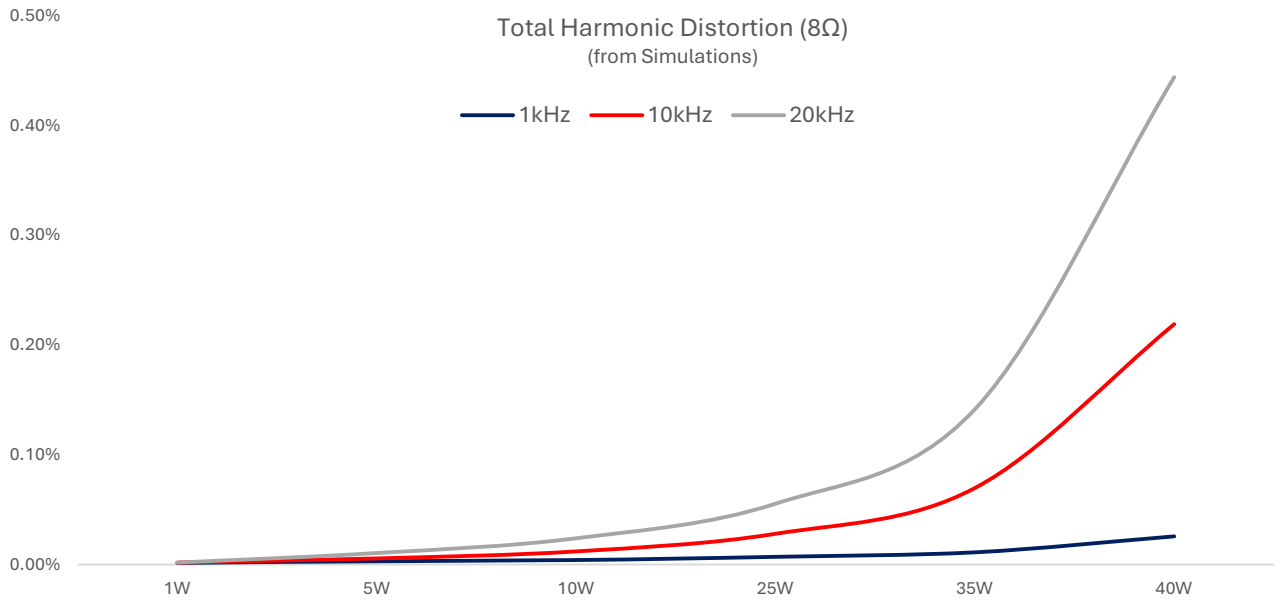
2. Specifications *(simulated – replace with actuals once measured)*

Class	A/AB
Input Impedance	Unbalanced 100KΩ
Input Sensitivity	0.47V_{RMS} for 1W (8Ω) 2.97V_{RMS} for 40W (8Ω)
Gain	15.5dB (6.0 x)
Frequence Response	15Hz to 740KHz (-0.1dB) 2.5Hz to 2.0MHz (-3.0dB)
Slew Rate	+34/-31 V/µs @ 10kHz, 4V_{peak} output (1W equivalent) +82/-46 V/µs @ 10kHz, 15V_{peak} output (14W equivalent)
PSRR	-82 dB @ 50 Hz -105 dB @ 1 kHz -106 dB @ 100 kHz

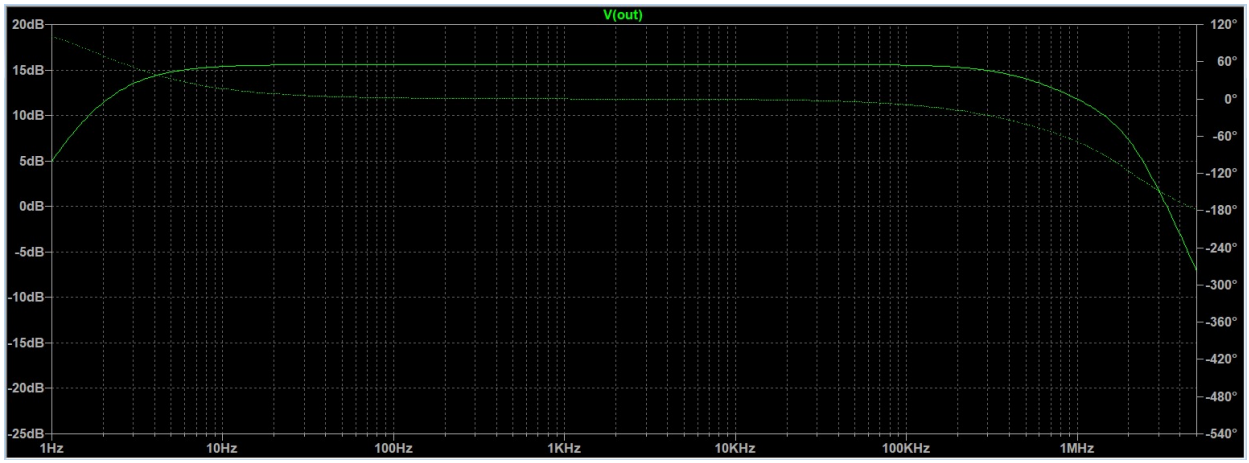
Specifications measured in simulation using the following options:

- PSU: V1 ±30V / V2 ±36V with 100mΩ /10,000µF RC filter
- IPS: LSK489 / LSJ689 with matched Idss of 5.5mA
- VAS: 2SC3503E / 2SA1381E matched for gain.
- OPS: ECX10N20 / ECX10P20

2.1 Distortion

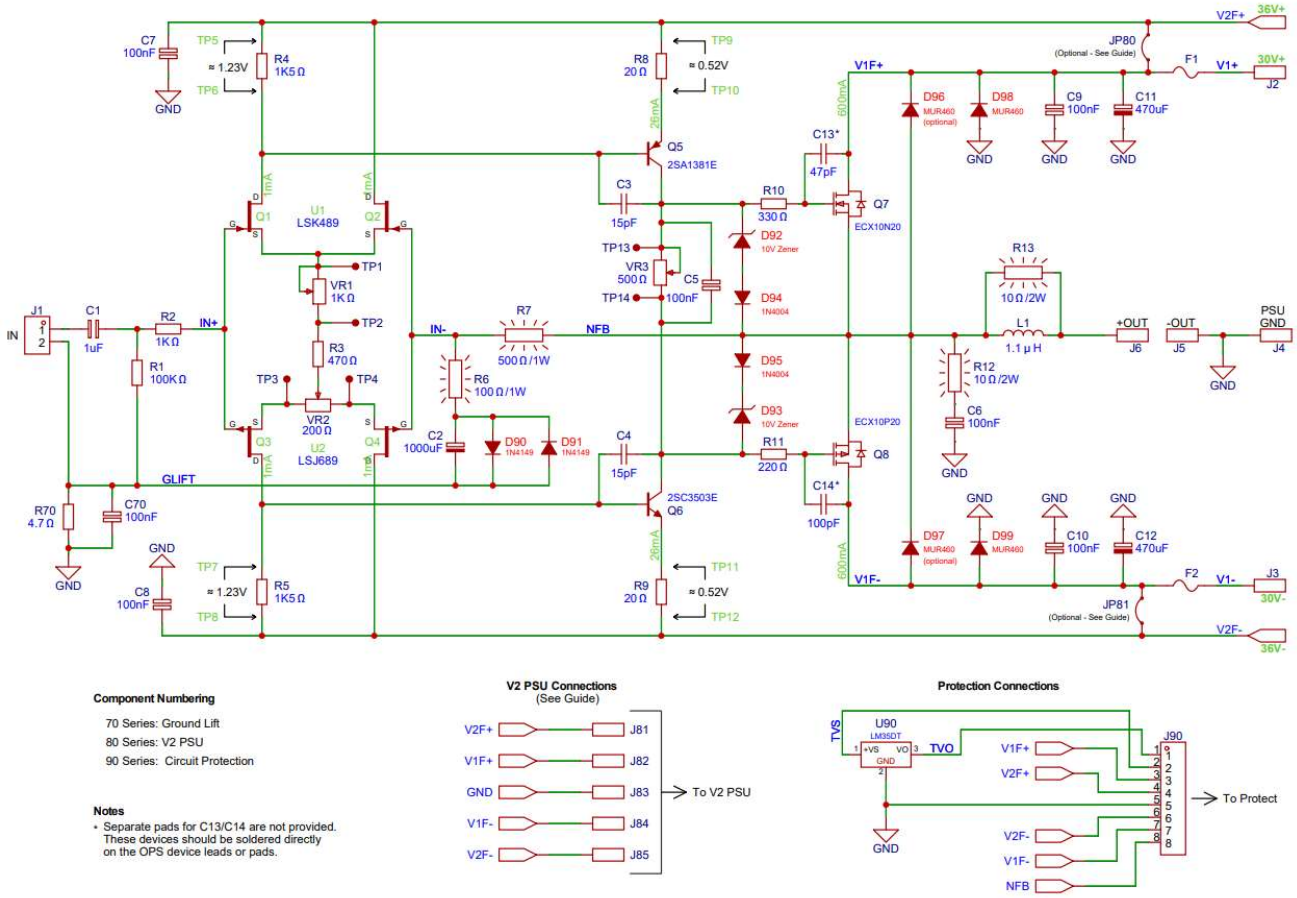


2.2 Frequency Response

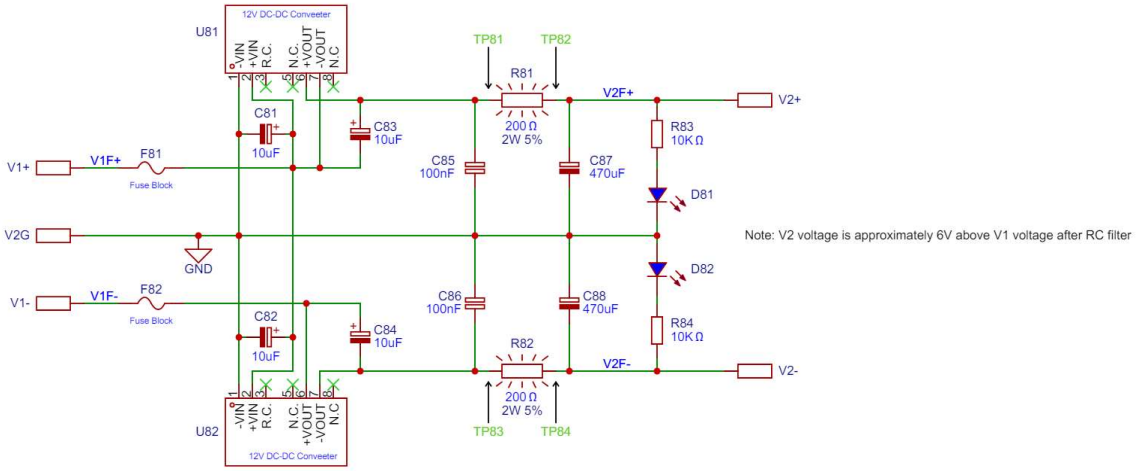


3. Schematic

3.1 Amplifier



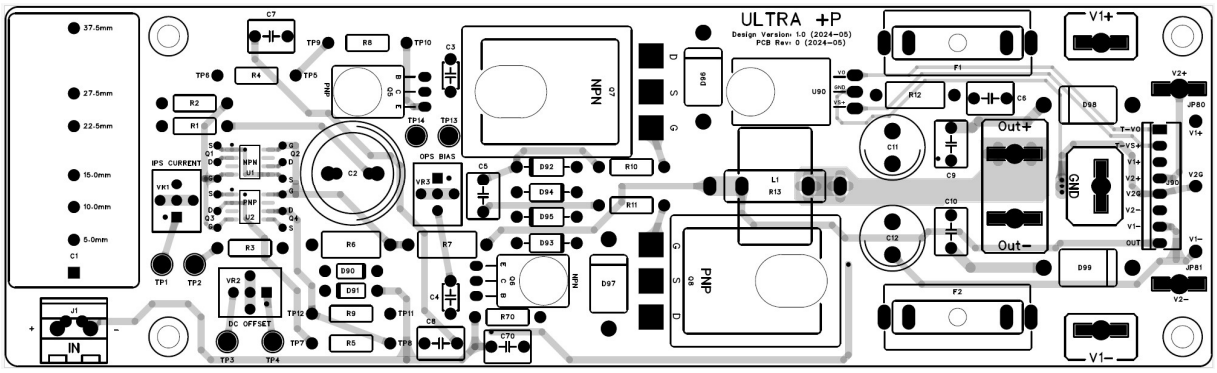
3.2 V2 PSU

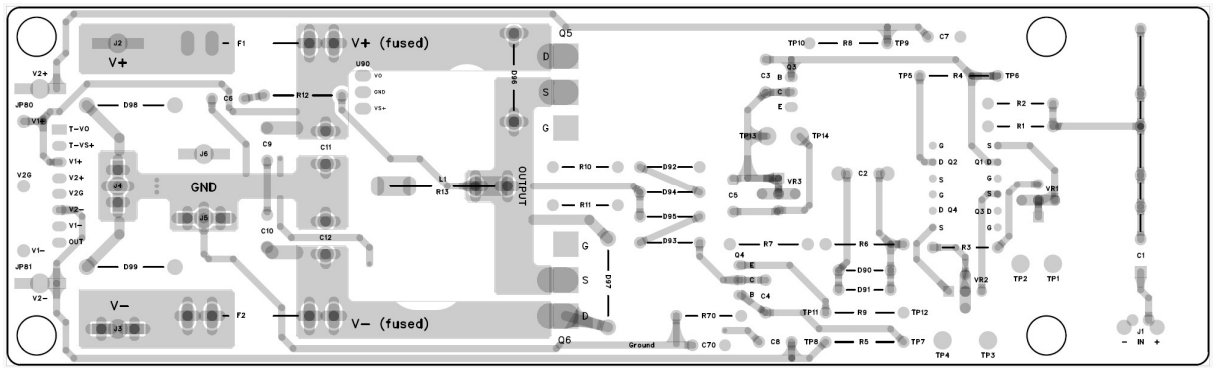


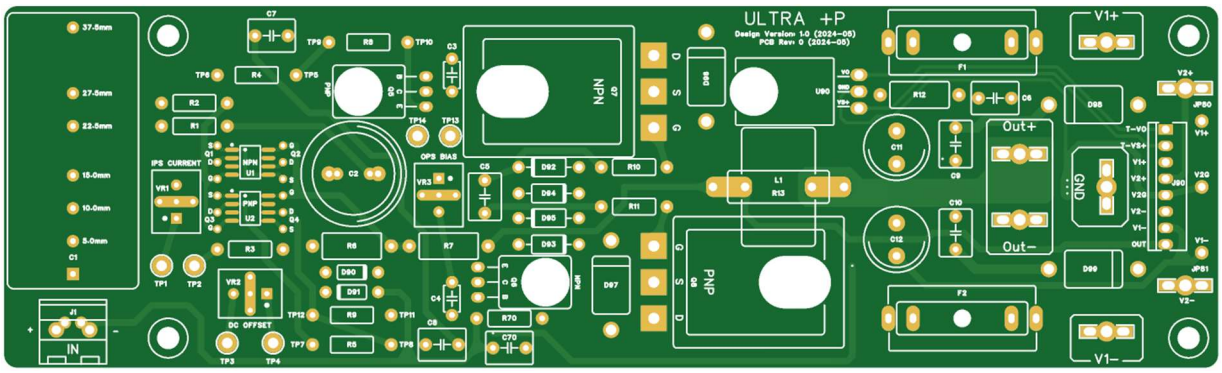
4. PCBs

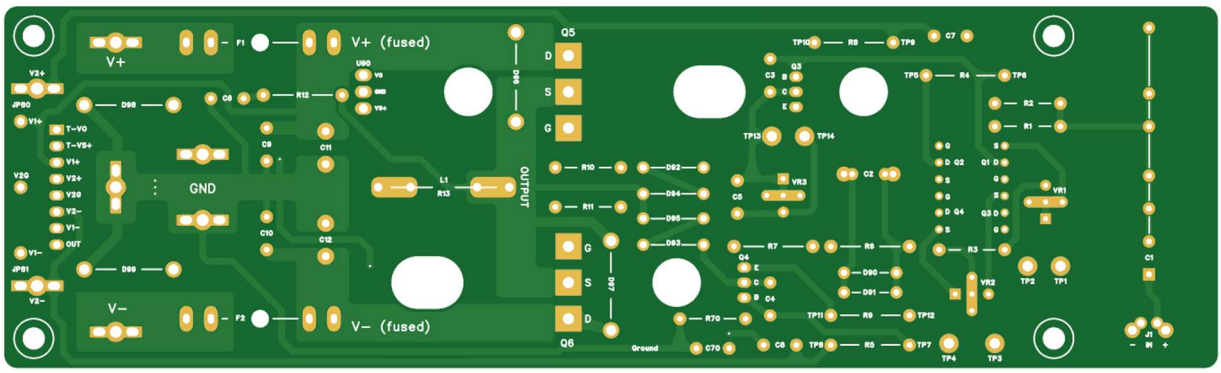
4.1 Amplifier

The amplifier board measures 185mm x 55mm.



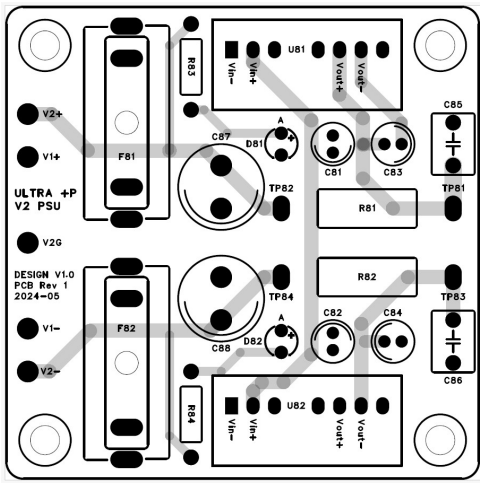


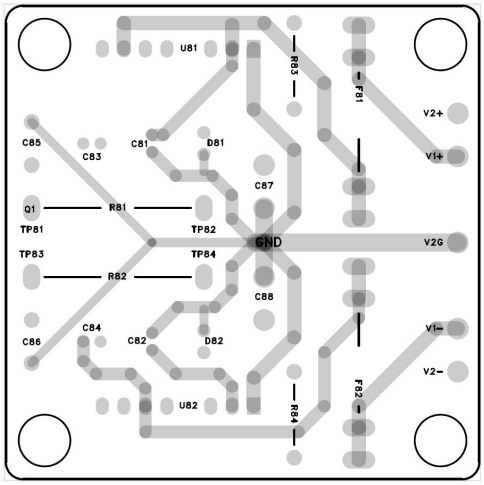


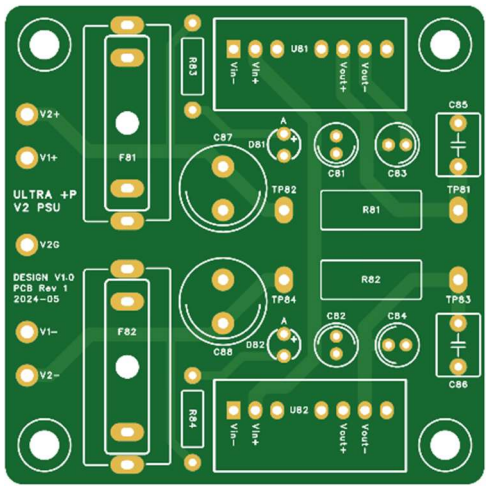


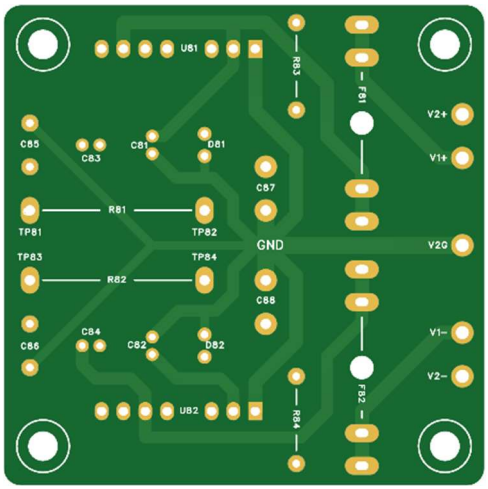
4.2 V2 PSU

The V2 PSU board measures 55mm x 55mm.









5. Components and Options

5.1 Power Supply

This design is intended to run on ±24V to ±30V main rails (V1 PSU) with the IPS/VAS rails boosted by 6V above the main rails (V2 PSU). The V2 PSU boost is supplied by isolated DC-DC converters running off the V1 main rails (this is explained further in section 5.1.2). This design allows for separate IPS-VAS rails without requiring an additional transformer or a custom transformer with multiple windings.

5.1.1 V1 PSU Options

The recommended power range for the main (V1) PSU is ±24V to ±30V. The table below outlines power transformer options. The estimated output assumes V1 rails will drop by 5% under full load.

Transformer Options

Secondaries (AC)	(V1) Main Rails (DC)	(V2) IPS-VAS Rails (DC)	(per channel) Transformer	Estimated Output *	Main Rail Fuses **	
					8Ω	4Ω
18-18	±24V	±30V	60VA - 110VA	25W into 8Ω / 45W into 4Ω	2A	4A
20-20	±27V	±33V	80VA - 140VA	32W into 8Ω / 55W into 4Ω	2.5A	4A
22-22	±30V	±36V	100VA - 175VA	40W into 8Ω / 70W into 4Ω	2.5A	4A
30-30	±41V	Up to ±50V ***	200VA - 350VA	80W into 8Ω / 140W into 4Ω	4A	7A

* Estimates assume TO-247 devices for 8Ω loads, TO-264 for 4Ω loads and use of the V2 PSU.

** Slow-Blow fuses recommended.

*** Theoretical max. This configuration is not supported by the V2 PSU as described in the schematic in section 3.2.

The table above assumes the V2 PSU will be used which derives its base voltage from the V1 PSU. If you plan to drive the IPS-VAS rails directly from the main rails (no boost), the maximum recommended voltage is ±41V from 30-30 secondaries. This is recommended to stay within the limits of the LSJ689 JFETs which have a max rating of 50V.

Note: If using a 2U chassis, ensure that the transformer height, including mounting hardware will fit without risk of a shorted-turn if the mounting hardware contacts the chassis top cover.

5.1.2 V2 PSU Description

The V2 PSU uses DC-DC converters (U81/U82) to boost the voltage on the IPS-VAS rails by 6 volts above the main rails (V1). This is done using isolated DC-DC converters with their Vout pin referenced to the main rails which results in a 12V boost. The 200Ω resistors (R81/R82) in the RC filter that follows will drop six volts for a final boost of six volts.

The boosted IPS/VAS rails provide several benefits

1. The boost allows for an aggressive RC filter to substantially improve PSRR. In simulations, PSSR at 50Hz improved by 12 dB, with the gap improving with increasing frequency.
2. For the recommended 2SC3503/2SA1381 devices, simulations suggest that distortion was reduced by 5 or more volts of boost.
3. Boosted IPS/VAS rails allow the lateral MOSFETS to swing closer to the V1 PSU rails, allowing for more output potential with less idle dissipation. For example, without boost the ±36V/±30V setup is

equivalent (in terms of output potential) to running a single ±34V PSU. This will increase dissipation in the MOSFETS from 18W each to 20W each at 600mA of bias.

The recommended DC-DC boosters are isolated SIP-8 (7 lead) devices with a 24V nominal input in a 2:1 range. This is a standard format available from numerous manufacturers. The 2:1 input range allows the DC-DC converter to be driven by an 18V to 36V source. The recommended ±24V to ±30V V1 PSU falls within this range and provides a 20% variance to account for mains and transformer regulation issues and/or voltage drop under heavy loading.

When selecting DC-DC convertor devices, three factors must be observed:

1. The RC filter that follows the DC-DC converter represents a capacitive load to the converter. The devices selected need to be rated for this load (470µF from C7/C8).
2. The power and current rating should allow for worse case current under fault conditions. For this reason, 2W or greater devices are recommended.
3. The maximum current rating must consider inrush current. Inrush can be up to 170mA at turn-on.

The following table identifies several DC-DC converters that have specifications compatible with this design.

Manufacturer	Part	Max Capacitance	Availability	Tested	C87/C88	Fuses (Slow-Blow)
MicroPower Direct	MD624S-12RW	1,600µF	Manufacturer	Yes	470µF	250mA
Recom	RS3E-2412S/H3	1,000µF	DigiKey, Mouser	No	470µF	250mA
Traco Power	TEC 3-2412	1,000µF	DigiKey, Mouser	No	470µF	250mA
aimtec	AM3G-2412S-NZ	680µF	DigiKey	No	470µF	250mA
XP Power	IZB0324S12	680µF	DigiKey, Mouser	No	470µF	250mA

Note that the input voltage for the DC-DC converters is isolated from the output voltage and powers from the positive V1 rail. Therefore, these devices will place an asymmetric load on the main V1 PSU. This is reflected in the asymmetrical V2 PSU fusing recommendations.

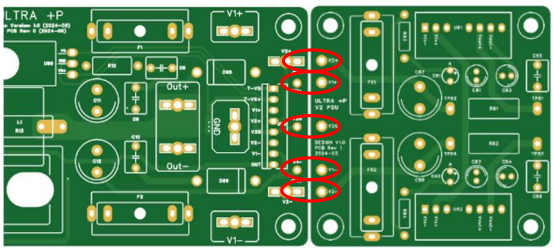
Inspiration for this approach comes from Winfield Hill's AMP-70 laboratory amplifier. This design has been discussed on diyAudio [2].

5.1.3 V2 PSU Options

The IPS-VAS boosted rails are intended to be supplied by the separate "V2 PSU" PCB. However, other build options are available:

Option 1: IPS-VAS boosted using V2 PSU PCB

This is the default option using the V2 PSU PCB. The V2 PCB mounts on the main heatsink alongside the amplifier PCB. Wire links are soldered between the boards to connect them.

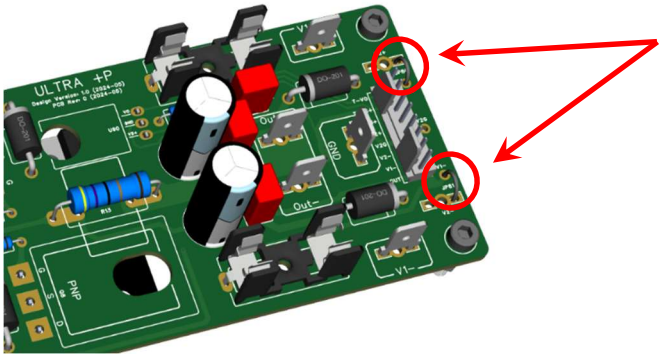


Option 2: IPS-VAS supplied by separate external PSU

For this option, the V2 PSU PCB is not utilized. The amplifier PCB has provisions for quick connectors in a 5.08 mm pitch, which can be used to connect to an external PSU to the V2 rails. If using this option, the IPS voltage should be higher than the V1 PSU voltage and be limited to under 50V to account for maximum ratings of the JFETs. If the PSU is unregulated, allow a safety margin to account for possible voltage fluctuations. Using a regulated V2 PSU will allow for voltages closer to the 50V max.

Option 3: IPS-VAS running off main rails (no boost).

The V2 PSU can be omitted, and the IPS-VAS can power from the main rails. Jumpers J80 and J81 allow the V2 rails to source power from the V1 rails.

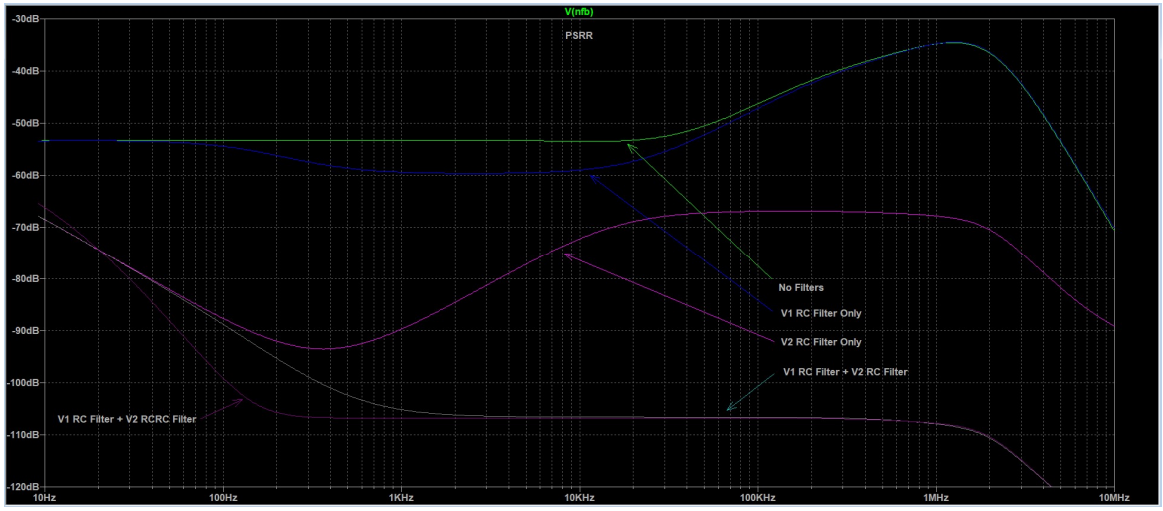


Note that in simulations, the KSC3503 / KSA1381 were most sensitive to a lack of voltage boost. If not using a rail boost, the TTC004B / TTA004B devices performed better.

Note that without the V2 PSU the RC filter on the rails is removed. This drops the PSRR (in simulations) to approximately -59dB.

5.1.4 PSRR

Filtering on the V1 and/or V2 rails will improve the PSRR of the amplifier. The plot below from AC simulations shows the impact of various PSU filtering options. The V1 RC filter used in these simulations was 0.1Ω followed by 10,000µF. The V2 filter dampens mains frequencies and the V1 filter dampens higher frequency noise.



Simulated AC response showing PSRR

The V2 RCRC is a proposed improvement to the existing V2 PSU. Splitting the RC network into a RCRC network provides approximately 6 dB of improvement at mains frequencies.

A capacitance multiplier circuit like that used on the Wolverine was explored for the V2 PSU. However, the inrush current from this approach exceeded the current handling capabilities of most SIP-8 DC-DC converters. It may be explored again in the future, however the DC-DC converters provide enough voltage boost to counter the voltage drop from the simple "brute force" RC filter, while still providing reasonable results.

5.2 Resistors and Capacitors

None of the resistors or capacitors in this design will benefit from precise targeting of stated values. Resistors with 1% tolerance and ceramic/film capacitors with a 5% tolerance are reasonable.

Resistors R4 and R5 establish the current for the VAS. Their values depend on the VAS devices in use. Refer to section 5.4.

Resistors R10 and R11 are gate stoppers for the lateral MOSFETs. Their values depend on the device used. Refer to section 5.5.

Capacitors C1 and C2 establish the lower frequency response and phase shift. At the stated values, phase deviation is less than 2 degrees down to 80Hz. These can be increased to 4.7µF / 4,700µF if low frequency phase shift is important to your build. With these values, phase shift will be less than 2 degrees down to 20Hz.

Capacitors C13 and C14 do not mount on the PCB. These should be installed on the transistor leads themselves or across the pads of the output devices. See section 6.3. These capacitors are recommended as an abundance of caution to guard against parasitic oscillations in the output devices. Simulations do not suggest that they are necessary, but simulations also indicate they do little harm. These may be omitted at your discretion.

Resistor R12 is part of the output Zobel network and should be non-inductive.

5.3 Input Stage

The input stage is based on the LSK489 and LSJ689 monolithic dual matched JFETs running at 1.0 mA of bias current. This bias level is near the zero tempco point for these devices which aids in temperature related stability.

The board footprint supports through hole TO-71 and surface mount SOIC-8 devices. Hole spacing for the TO-71 devices is set at 2.54mm allowing for the use of 3 pin sockets for the TO-71 devices if desired (DigiKey part Z8777-ND).

Bob Cordell discusses JFET device selection and the impact of I_{DSS} matching between the N and P channels in his update to the Hafler DH-220 (The DH-220 has a similar IPS and VAS topology). Details can be found in his *Complementary JFET Offset Mismatch* paper on his website [3]. There are three key takeaways:

- The I_{DSS} value of the devices is not critical.
- Matching between the N and P channels is not necessary.
- The monolithic devices are not perfectly matched, and some offset will result from this. If the direction of the offset between the P and N channels is opposed, it will increase offset. The TO-71 package allows the devices to be "flipped" to reduce the impact of this. See section 7.2 for more information.

The P-Channel LSJ689 pair has degeneration of 100Ω to account for their higher transconductance over the LSK489. This degeneration is implemented as a trimmer potentiometer to allow for trimming of DC offset.

The 470Ω resistor R3 is used to limit the maximum current the IPS can source if the trimmer VR1 is incorrectly set to its lowest value.

5.3.1 Amplifier Gain

The stated value of 500Ω for R7 produces as overall gain of 15.6dB (6x). For a build using a ±30V V1 PSU, an input of 2.97V_{RMS} will be required to fully drive it to 40W of output. For most sources, this requires the use of a preamp.

This gain level will produce the lowest distortion, but other options are available. The gain can be increased at the expense of higher overall distortion by increasing the value of R7. The table below shows various options and their simulated impact on distortion:

Gain	Input for 40W output	R7	C3 / C4	Simulated 1kHz Distortion *				
				1W	5W	10W	25W	40W
15.6 dB	2.97 V_{RMS}	500Ω	15.0pF	0.0011%	0.0020%	0.0028%	0.0049%	0.0662%
20.8 dB	1.63 V_{RMS}	1,000 Ω	4.7pF	0.0017%	0.0034%	0.0048%	0.0086%	0.1165%
24.0 dB	1.13 V_{RMS}	1,500 Ω	1.5pF	0.0023%	0.0049%	0.0068%	0.0122%	0.1629%
26.4 dB	0.86 V_{RMS}	2,000 Ω	Omit	0.0030%	0.0064%	0.0089%	0.0159%	0.2076%

* Simulations performed with KSC3503D / KSA1381E & ECX10N20 / ECX10P20 into 8Ω with 600mA bias

5.4 Voltage Amplification Stage

The design specifies the VAS devices running at 26mA. The actual current is not critical. No adjustments are needed if the current measures approximately 24 mA to 28 mA. At these levels, the devices will dissipate between 500mW to 1W of heat each. The PCB accommodates TO-126 devices mounted under the board on the main heatsink to manage dissipation.

Due to the simple nature of this design, the VAS is sensitive to mismatches in the gain between the N and P channels. This mismatch will lead to excessive DC offset. DC offset can be trimmed with VR2, though this trimming should ideally be at a minimum. In addition, the gain of the VAS devices has a direct impact on the values for R8 / R9. Refer to the chart below for recommended values.

The ideal devices for this design should be high gain, with matched gain between N and P devices, low capacitance and robust. Based on devices available today, KSC3503D / KSA1381E and TTC004B / TTA004 are the best candidates. The capacitance of KSC3503D / KSA1381E is lower, but the gain and gain matching of

TTC004B / TTA004 is superior. Simulations suggest that KSC3503D / KSA1381E performs slightly better than TTC004B / TTA004.

If we consider out-of-production devices, 2SC3503E / 2SA1381E are very attractive (assuming you can reliably source them). The gains from these devices are more closely matched between N and P channels and many of these are available with exposed metal mating surfaces, rather than full encapsulation. This should theoretically result in lower junction temperatures.

Consult the table below for values of R4/R5 and R8/R9. These values were chosen to set the VAS current to 26mA and to stabilize the DC operating conditions against temperature variations between cold and hot states. For KSC3503D / KSA1381E, R8 / R9 are specified as different values to account for typical gain mismatches between the N and P channels.

			Test Voltage			
Device	**R4 / R5**	**R8 / R9**	**R4 / R5**	**R8 / R9**	**Notes**	**Testing**
2SC3503E / 2SA1381E	1.5KΩ	20Ω	1.23V	0.52V	Out of production. May be difficult to source.	Tested
KSC3503D / KSA1381E	1.58KΩ	22Ω / 18Ω	1.23V	0.52V	R8/R9 values account for differences in gain. KSA1381E is end-of-life in early 2025.	Simulated
TTC004B / TTA004B	2.0KΩ	47Ω	1.80V	1.19V		Simulated
BD139 / BD140	2.15KΩ	52Ω	1.93V	1.33V	Close to other options at lower power levels.	Simulated

Note, BD139 / BD140 worked in simulations and are footprint compatible but are not recommended. If you wish to experiment with them, recommended values are provided based on simulations.

The test voltages across R4/R5 are used to set the IPS current. At the values stated, IPS current should be around 1.0 mA. The stated ratios of R4/R5 to R8/R9 establish the VAS current. Increasing the values R4/R5 and R8/R9 will increase stability against temperature changes, at the cost of an increase in distortion. The values specified strike a balance between stability and performance.

5.5 Output Stage

The output stage is designed for use with Exicon Lateral MOSFETs. These can be purchased directly through Profusion (UK) as well as secondary suppliers such as ELTIM (Netherlands).

The TO-247 package is recommended for 8Ω loads and the TO-264 package is recommended for 4Ω loads. The table below illustrates the advantages the double die TO-264 devices provide when driving 4Ω loads.

The different values for R10 and R11 are to account for differences in the input capacitance between N and P channels. The change in values between TO-247 and TO-264 is to maintain the same RC filter pole frequency.

Capacitors C13 and C14 aid in preventing parasitic oscillation. These should be mounted on the package leads as close to the plastic body as possible.

The 8Ω Load and 4Ω Load values represent the output power potential.

Device	**Package**	**8Ω Load***	**4Ω Load***	**R10**	**R11**	**C13**	**C14**	**Testing**
ECX10N20 / ECX10P20	TO-247	40 W	55 W	330Ω	220Ω	47pF	100pF	Tested
ECW20N20 / ECW20P20	TO-264	45 W	70 W	220Ω	150Ω	68pF	150pF	Simulated

* Based on ±30V Main Rails (V1) and 600mA of bias per device

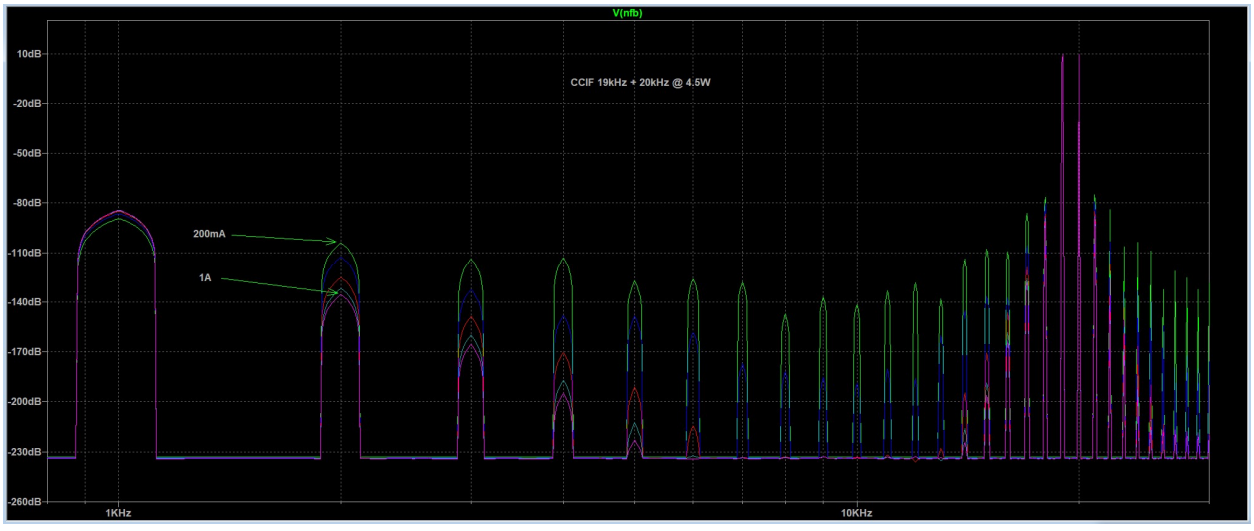
5.6 Output Stage Bias & Heatsinks

The design was tested with 600mA of bias with ±30V Main Rails and 2U 300mm deep heatsinks. With this configuration, the output devices will dissipate around 18W at idle and the heatsinks should operate at 30°C to 35°C above ambient.

Bias affects the Class A region, with performance improving as the Class A region increases. The table presented below details options for selecting a bias settings based on various V1 PSU voltage and heatsink combinations (this assumes an 8Ω load). The bias values indicated should result in a 30°C to 35°C heatsink temperature rise above ambient at idle. The heatsinks will be warm to very warm to the touch at these levels. Modeling was performed using the Heatsink Calculator tool at heatscape.com [5]. Results of modeling were validated with bench testing using ±30V main rails and 3" x 12" raw aluminum heatsinks.

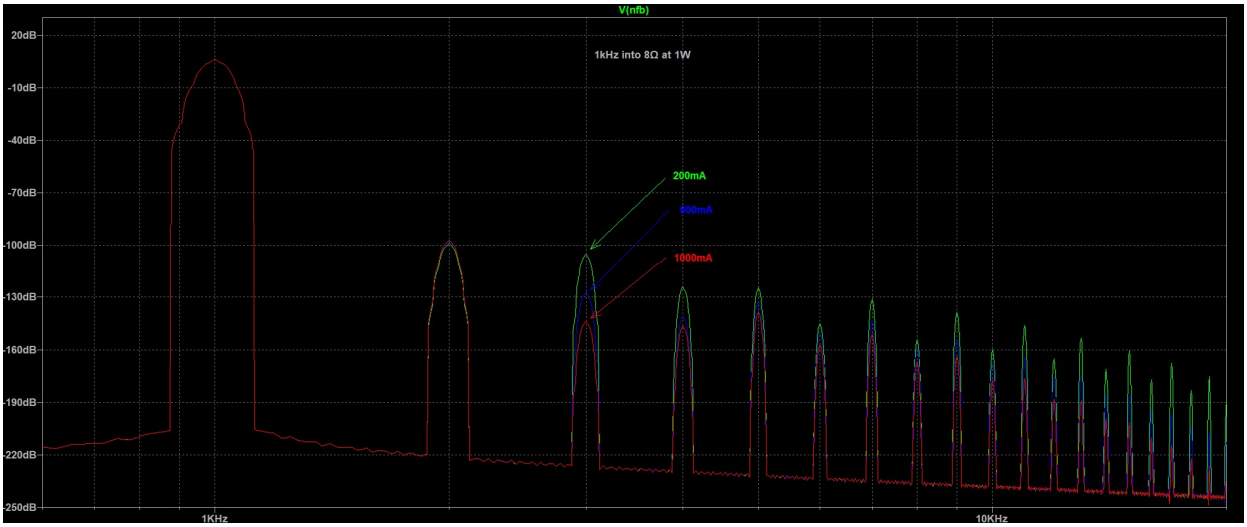
Transformer Secondaries		**Heatsink Size**					
		(18 W Dissipation) **2U**		*(22.5 W Dissipation)* **3U**		*(27 W Dissipation)* **4U**	
AC	**DC**	**Bias**	**Class A**	**Bias**	**Class A**	**Bias**	**Class A**
18	24	740 mA	8.75 W	920 mA	13.50 W	1120 mA	20.00 W
20	27	665 mA	7.00 W	830 mA	11.00 W	1000 mA	16.00 W
22	30	600 mA	5.75 W	750 mA	9.00 W	900 mA	13.00 W

Increasing the Class A region provides at least two measurable benefits based on simulations. First, as bias increases intermodulation distortion decreases. This can be illustrated with CCIF distortion which produces intermodulation components at the difference of the primary signals. For example, a two tone 19kHz and 20kHz signal produces intermodulation components at 1kHz. Higher OPS bias will cause these components to decay faster. This is illustrated in the simulation shown below. The 1kHz component is slightly elevated at higher bias levels, but the rate of decay increases with increasing bias. This plot shows bias at 200mA, 400mA, 600mA, 800mA and 1000mA.



Simulated FFT plot of CCIF test of 19kHz and 20kHz at 4.5W into 8 Ω

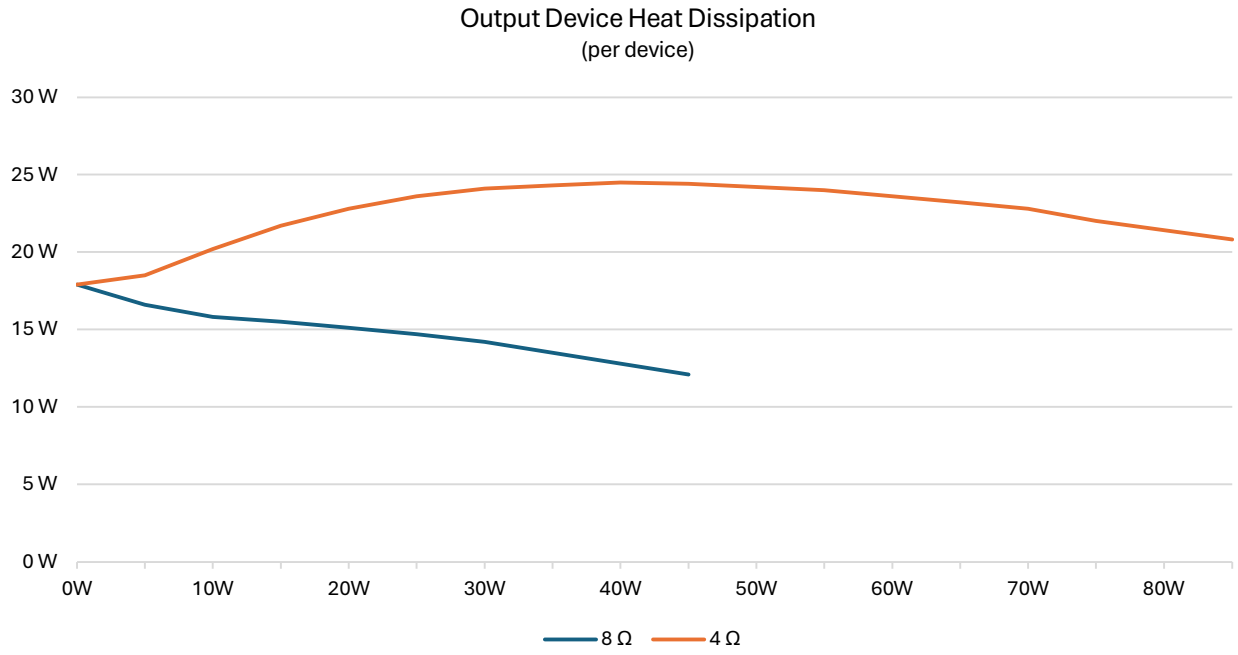
Second, as bias increases overall measurable harmonic distortion drops slightly. However, the harmonics impacted are primarily third order and above. The FFT plot below illustrates this impact and shows how second order distortion is minimally impacted.



Simulated FFT plot of 1kHz sine wave at 1W into 8 Ω

The key observation is that more bias is better. The design was tested with 600mA of bias, though you can run higher bias if your heatsinks can accommodate it.

As mentioned above, at 600mA of bias each device will dissipate around 18 watts at idle with ±30V main rails. With 8Ω loads, dissipation will drop as power levels increase. For 4Ω loads, it will increase and peak at 24.5 watts of dissipation at 40 watts of output. See the chart below for dissipation differences between 8Ω and 4Ω loads.



5.7 Output Inductor

The output inductor can be formed from nine to ten turns of 18-gauge enameled copper wire around a 5/8” diameter (15mm to 16mm) former. The exact value of the inductor is not critical. Anything 1uH or over is acceptable.

If you would rather purchase this component, the board footprint will accommodate Neurochrome's 1.1uH inductor (https://neurochrome.com/collections/chassis-parts/products/output-inductor).

5.8 DC Offset

Capacitors C1 and C2 are included to mitigate DC offset. DC offset derives from mismatches between the N and P devices in the VAS and OPS. The DC Offset is trimmed using the VR2 trimmer potentiometer. The NULL point of this trimmer will vary with temperature, specifically between the cold and hot states. C1 and C2 will assist with dampening this effect. Gain grade mismatches between VAS devices will increase DC offset. With devices and component values recommended, DC Offset should vary by 10mV or less between hot and cold states.

5.9 Board Standoffs

The recommended standoffs in the BOM are specified to avoid problems with the depth of blind mounting holes. If using Modushop drilling services, holes will be threaded to a depth of 5.0 mm to 6.0 mm. Most readily available male standoffs have a threaded depth of 6.0 mm and therefore may have problems seating fully. The recommended RAF Electronics standoffs have threads measuring 4.76 mm in length (DigiKey 1772-4180-ND or Mouser 761-M2105-3005-B)

The recommended between-board-height for the standoffs is 9mm to 10mm. This is to avoid interference with the transistors and mounting hardware, while being short enough for the bent TO-126 leads to reach the PCB pads for soldering.

5.10 Protection

The 70 series (R70 and C70) provide an isolating ground lift for input devices. This lift is not required. If the builder does not wish to implement this, C70 can be omitted and R70 can be replaced with a wire link.

Connector J90 provides outputs for protection circuits. This includes temperature sensor U90 (LM35DT) in a TO-220 package. The C90 connector provides outputs that a typical protection circuit will need. These parts are optional. The related protection circuits are outside of the scope of this guide. If you are interested in exploring this further, Bob Cordell's book *Designing Audio Power Amplifiers* is an excellent resource. Chapter 4, *Building an Amplifier*, includes descriptions of his approach to protection circuits.

The remaining 90 series components on the amplifier board are all protection devices. None of these are required for the amplifier to function. They can be omitted at the builder's discretion.

D90, D91: These clamping diodes limit voltage across C2 in the event of a fault condition on one of the rails.

D92, D93, D94, D95: The diode and zener combination limits the maximum gate voltage and provides basic overload protection.

D96, D97: These diodes prevent the lateral MOSFETs from being reverse biased. If your devices have integral protection diodes, these are redundant and can be left unpopulated.

D98, D99: These reverse diodes prevent the rail voltage from going to the reverse polarity in the event of a fault to one of the rails.

6. Assembly

The general build process involves inspection, cleaning, and trial fitting first followed by assembly. When assembling, follow best practices of beginning with low profile parts first and finishing with the largest/highest profile parts.

While assembling, it is recommended to periodically clean the boards of flux before proceeding to larger parts.

WARNING: The JFETs and MOSFETs used in this design are very sensitive to static discharge. Use of a grounding strap or touching a grounded surface before handling these devices is recommended. Failure to do so could result in permanent damage.

6.1 Inspect and Clean

Clean the boards with isopropyl alcohol and inspect for any defects. Trial fit components to ensure everything fits.

6.2 Resistors, Diodes and Small Devices

If using SOIC-8 package for the JFETs, consider soldering these first due to their small size. As the board gets populated, it may be difficult to solder these later. In addition, the trace clearances for the JFETs are tight. Carefully check your work to ensure that no solder bridges have been created. You can use your DMM to check for continuity between pins. If using SOIC-8 devices, use the TO-71 pins for a continuity check and vise-versa for TO-71 devices.

For resistors that will be used as a test point and resistors rated above 0.25 watt, consider installing these slightly elevated. This will allow for easier connection of test hook clips and will aid in heat dissipation.

It is recommended to measure the value of resistors just prior to installation. The color banding can be difficult to interpret.

For diodes, ensure they are installed with the correct polarity.

It is recommended to clean the board of flux at this point. This will reduce the amount of cleaning needed later, which will become more difficult as bulkier components are added.

6.3 Capacitors and Connectors

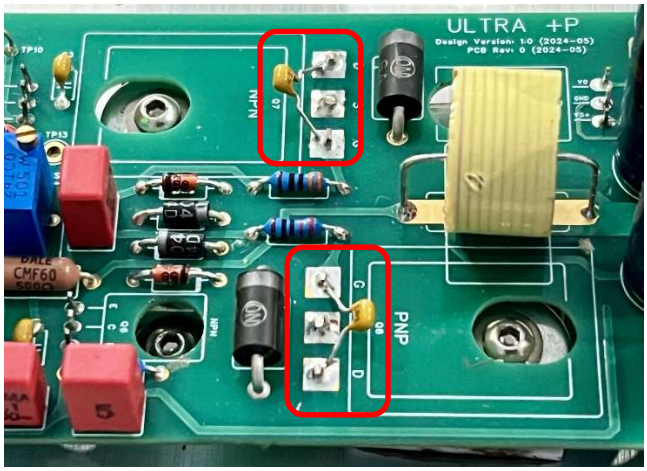
The recommended quick-connect spade connectors can be tricky to solder, as they don't have a mechanical method to hold them in their pads when the board is turned upside down. These connectors are 10mm in length, which is the same height as the recommended standoffs. A trick to holding them in place is to place the board upside down on the standoffs with the connectors in place. This will hold them in place against the heatsink, allowing them to be soldered.

For connector J1, determine if you will use the 5.08mm terminal blocks or 2.50mm headers.

For jumpers 80 & 81, only populate these if you are not using boosted IPS-VAS rails (refer to section 5.1.3).

Begin with smaller ceramic and film capacitors, then move onto larger components. Ensure electrolytics are installed with the correct polarity.

Note that capacitors C13 and C14 mount on the transistor leads or in the same pads as the output devices. For the test build, these were installed in the pads for the drain and gate alongside the MOSFET leads. If using this approach, be careful not to create a short to the MOSFET source pad.



Clean the board again to remove flux and contaminants.

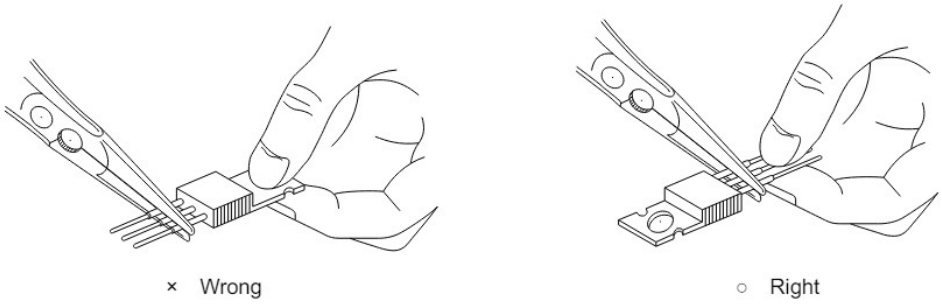
After cleaning, thoroughly inspect the board before proceeding to mounting of transistors. Look for incomplete solder joints, solder bridges and missing components.

6.4 Transistor Lead Forming and Heatsinks

For the input JFETs, bend the leads on the TO-71 package devices to match the footprint on the boards. Install the 3-pin sockets if using (as described in section 5.3).

For the VAS and OPS transistors and Protection Temp Sensor, the devices will mount under the board on the main heatsink. The bending-point of the leads should be where the leads transition from narrow to wide.

When bending/forming leads, secure the leads (with pliers for example) and bend against this secured point, not against the transistor body.



(Image taken from Renesas Application Note R07AN0005EJ0100)

Test fit the transistors after lead forming and adjust if needed. To prepare for soldering, temporarily fasten the transistors to the heatsink without insulators or grease, then solder the leads. Remove mounting screws and complete a final cleanup and inspection.

6.5 Transistor Mounting

Carefully inspect the heatsinks to look for any burrs or raised surfaces. Any defects can compromise the insulators causing shorts with the heatsink. Just prior to applying the insulators, thoroughly clean the surface with isopropyl alcohol.

The VAS, thermal sensor and lateral MOSFETs must be mounted to the main heatsinks with screws. If using Modoshops drilling services, these will be threaded for M3 screws. Care must be taken when selecting screw lengths to ensure the thread penetrate deeply enough, but do not bottom out on the blind holes. In addition, the screw should penetrate deep enough to hold properly; ideally about 4mm to 5mm. The following table is an example of conditions to consider when selecting mounting screw lengths.

Package	Washer Thickness		Average Package Thickness	Insulator Thickness	Total Height	M3 Screw	
	Belleville	Flat				Length	Penetration
TO-126	N/A	0.6 mm	3.25 mm	1.6 mm	5.45 mm	10.00 mm	4.55 mm
TO-247	0.8 mm	1.2 mm	5.00 mm	2.0 mm	7.10 mm	12.00 mm	4.9 mm
TO-264	0.8 mm	1.2 mm	4.90 mm	2.0 mm	7.00 mm	12.00 mm	5.00 mm
TO-220	N/A	0.6 mm	1.25 mm	1.6 mm	1.95 mm	8.00 mm	4.55 mm

When using blind holes to mount power transistors, it is critical that the screw is adequately tightened and not simply bottoming out. A screw that has bottomed out due to being too long can give the false impression that it has been properly tightened.

When mounting transistors, insulator pads must be used if the transistor is not fully insulated. Some TO-126 devices are offered in full-pack fully insulated package. For these devices, using an insulator is unnecessary and will degrade thermal conductivity to the heatsink, increasing junction temperatures. However, thermal grease should still be used to ensure optimal heat transfer.

For the lateral MOSFETs and temp sensors, insulators must be used. The Exicon devices have an insulated mounting hole, so insulated shoulder washers are not required.

Insulator materials are commonly 1mil Kapton/polyimide tape with silicon adhesive backing, mica pads, silicon pads (such as Keratherm Red), and aluminum oxide ceramic pads. Thermal grease must be used with mica (both sides), Kapton/Polyimide (non-silicone side), and aluminum oxide ceramic (both sides).

There are suggestions from builders on diyAudio that thin insulators can form capacitive coupling between the MOSFET source pins and the heatsink, leading to parasitic oscillation [4]. The suggested fix for this is the use of 2mm thick aluminum oxide ceramic pads for the insulator (such as Aavid Thermalloy 4180).

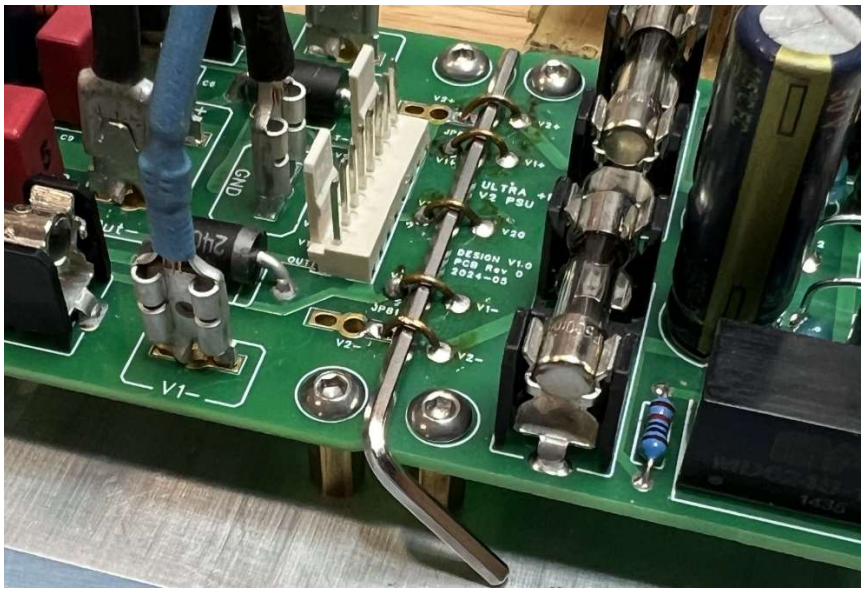
For the output devices consider using spring or Belleville conical lock washers and/or thread-locker (Loctite 222 Purple) to ensure a tight bond that will not loosen over time. If using mica or aluminum oxide ceramic, ensure you don't overtighten and crack the insulator.

Exicon does not provide recommended mounting torque for the fasteners. However, technical bulletins for other devices in TO-247 package will typically recommend 0.5 to 1.1 newton-meters (5 to 10 inch-pounds) of mounting torque. Nelson Pass recommends 8 inch-pounds [6].

After securing VAS and OPS transistors, use a DMM to perform a continuity check between the transistors legs and the heatsink. There should be no continuity. If any continuity is found, correct before applying power.

6.6 Connecting the VS PSU

If you are using the V2 PSU, mount the board to the heatsink and solder in links as described in section 5.1.3 to connect the VS PSU board to the amplifier board. Consider installing these links slightly elevated to allow test hook clips to easily attach. A small hex wrench can be used to elevate the links while soldering:



6.7 Final Inspection

Refer to the schematic and BOM and ensure all devices are installed before proceeding to testing.

Wipes can be used to clean any remaining flux that was not removed in earlier cleanings.

7. Setup and Testing

7.1 Initial Setup Before Initial Power-On

Verify all components are populated.

Verify that a continuity check has been completed for transistor shorts with the heatsink.

Use a short piece of wire to short the inputs (connect In+ to In-). No signal will be applied at this stage.

VR1: Use TP1 and TP2 to set VR1 to its maximum resistance. This sets the IPS current to its lowest point. It will be trimmed later.

VR2: Use TP2, TP3 and TP4 to set VR2 to its midpoint. This equalizes the source degeneration of Q3/4. This will be trimmed later.

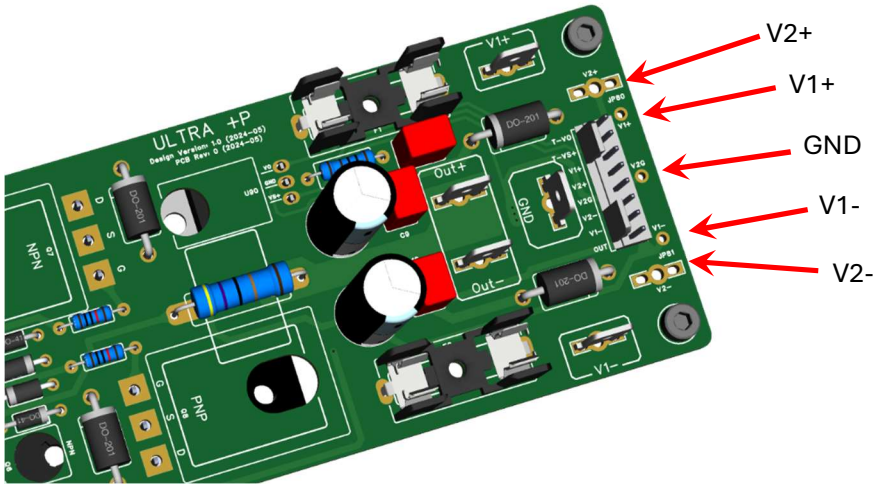
VR3: Use TP13 and TP14 to set VR3 to its minimum resistance. This sets output bias to its lowest. It will be adjusted later.

7.2 Initial Power-On

For the initial power-on, the IPS current will be adjusted, and the initial trimming of the DC offset will be made. During these steps, the current draw will be minimal. If desired, an adjustable bench power supply can be used, provided it can supply at least ±20 volts (minimum needed for the V2 PSU DC-DC converters to function).

Fuses: 100mA slow blow fuses for the V1 PSU can be used for the initial power on. These will limit any potential damage if a construction error has been made.

Verify Rail voltages: Apply power and verify the rail voltages at the fuse blocks. If using V2 PSU. Verify that the V2 rails are approximately 6V higher than the V1 rails.



Trim IPS Current: Measure voltage across R4 using TP5 and TP6 and across R5 using TP7 and TP8. Adjust VR1 until the target voltage is reached (See table in section 5.4). There may be an imbalance between R4 and R5 that may be trimmed later.

VAS Current: Verify the VAS current is within expected ranges. At operating temperature, it should run between 24mA and 28mA. Refer to the table in section 5.4 for test voltages. There will be a difference in readings between cold and hot states, but this variance should be small.

To measure, use your DMM to measure the voltage across R8 (using TP9 and TP10) and R9 (using TP11 and TP12).

Trim DC Offset: Adjust VR2 to NULL DC offset on the output. DC offset will drift as the devices heat up and will need re-adjustment. This drift should be under 10mV.

If using sockets for the JFET TO-71 devices, you can try flipping one of the devices to determine which direction minimizes offset. Then use VR2 to trim the resulting DC offset.

Remove power.

7.3 Second Power-On

For the second power-on, the output bias current will be set. Current draw will be less than 1A. We will let the heatsinks warm up and re-check, VAS current, OPS current and DC offset.

Fuses: If 100mA fuses V1 PSU were used for the initial power-on, these will need to be increased. 1A slow blow fuses can be used for the second power-on to limit power draw if desired.

VR3: Adjust VR3 to set the output bias. As the design lack source resistors on the outputs, you will need a mechanism to measure the OPS current draw. A power supply with a CRC topology is likely the easiest way to accomplish this. Before making an adjustment, measure the current being drawn by the IPS. Take this into account when setting the OPS bias. Slowly increase VR3 until OPS bias reaches 600mA per device. Measure again as the heatsinks warm and adjust further if needed.

If you are concerned about the heatsinks running too hot, you can adjust this up in steps. Set to 200mA and observe the heatsink temperature. Once they stabilize, increase bias further until 600mA is reached, or the temperature reaches a level you are comfortable with.

Remember, due to the large class A region, dissipation will likely be highest at idle. Because of this, we can perform these tests without needing a dummy load or test signal.

Adjusting setting the bias, recheck VAS current and DC offset. Adjust as needed.

7.4 Final Setup

When ready to test with speakers, replace fuses with 2.5A slow-blow and remove the wire shorting the input.

Note that this design does not provide short-circuit protection. DO NOT short the outputs.

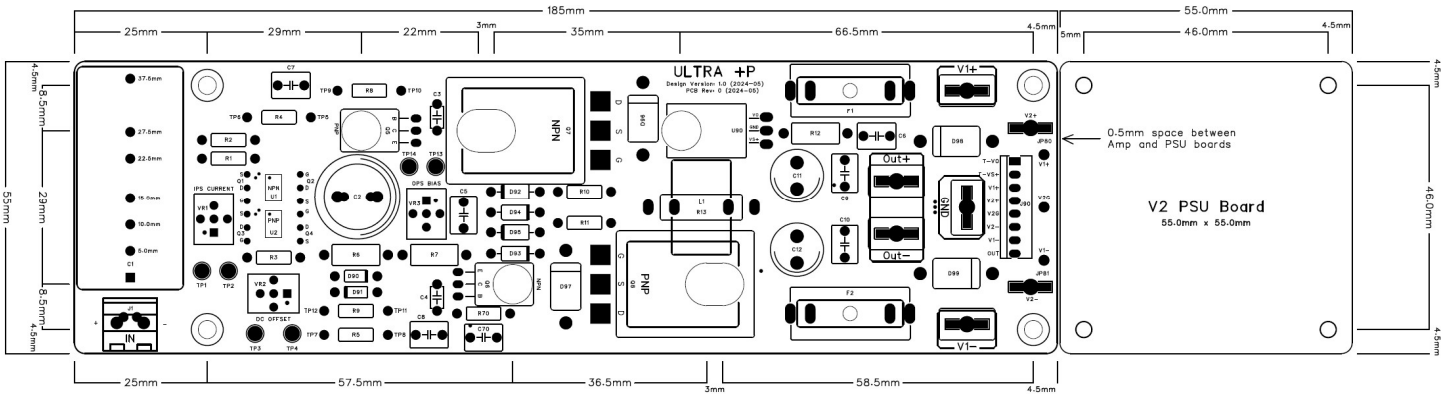
If you have an oscilloscope, you can connect a test signal and dummy and check the outputs for any signs of parasitic oscillation, before testing with speakers.

If you perform square wave testing and/or capacitive load testing, note that the zobel network resistor (R12) and Theile network resistor (R13) are rated at two watts. It is recommended to keep test signals at 10kHz or less and 2 V_{RMS} or less. If these are exceeded, R12 and/or R13 may fail.

There should be no large DC transients on the output at startup. However, a start-up mute and DC protection mechanism is recommended.

8. Heatsink Drilling

For the output devices, tap holes for the TO-247 or TO-264 spacing, but not both.



9. Additional Resources

The Wolverine Build Guide from diyAudio is an excellent resource for general building tips, as well as diyAudio in general. Many of the tips from this guide are sourced from the Wolverine Guide. It can be downloaded from this thread:

DIY Class A/B Amp The "Wolverine" build thread
https://www.diyaudio.com/community/threads/diy-class-a-b-amp-the-wolverine-build-thread.385920

Rod Elliott's website is also an excellent resource for DIY Audio projects. His project pages for the P3A, P3B and P101 have very good general construction tips.

The Audio Pages
https://sound-au.com

P3A: https://sound-au.com/project3a.htm
P3B: https://sound-au.com/project3b.htm
P101: https://sound-au.com/project101.htm

Hifisonix has numerous articles including several on groundings loops and wiring best practices. This site is run by user Bonsai on diyAudio.

Hifisonix
https://hifisonix.com/

10. Change History

10.1 Schematic

AMP		
Version 1	2024-05-20	Original
Version 2	*Not Yet Released*	Consider removing D96/D97 Add indicator LEDs & resistors to aid draining caps.

V2 PSU		
Version 1	2024-05-20	Original
Version 2	*Not Yet Released*	Consider splitting RC network to RCRC network for improved PSRR at mains frequencies.

10.2 PCB

AMP		
Rev 0	2024-05-20	Original
Rev 1	*Not Yet Released*	Corrections: Position of U90 corrected by 0.25mm. Enlarged pad hole size for C1 from 0.9mm to 1.1mm Correct bottom silkscreen for Q5/Q6 incorrectly labeled as Q3/Q4/. Changes: Consider removing JFET SOIC-8 footprint to increase trace spacing. Consider removing D96/D97 Add indicator LEDs & resistors to aid draining caps. Considering increasing component silkscreen font size for readability

V2 PSU		
Rev 0	2024-05-20	Original
Rev 1	*Not Yet Released*	Silk screen errors corrected (Components were not labeled as 80 series). Position of V2 pads corrected to align with Amp PCB pads. Considering increasing component silkscreen font size for readability

10.3 Build Guide

V1	2024-09-15	Original
V2	2024-09-17	Corrections: Section 5.4: R8 / R9 values corrected for KSC3503 / KSA1381 row. Changes: Section 5.3.1 added for changing amplifier gain. Section 5.4: Added a note about KSA1381E being end-of-life.

11. References

[1] lineup, (2024, February 28), “Ultra Amplifier with JFET input and Lateral MOSFET out”, DIYAudio.com, https://www.diyaudio.com/community/threads/ultra-amplifier-with-jfet-input-and-lateral-mosfet-out.409798/

[2] Winfield Hill [winhill2], (2017, June 15), “Winfield's 100W DC-10MHz 1000V/us amplifier”, DIYAudio.com, https://www.diyaudio.com/community/threads/winfields-100w-dc-10mhz-1000v-us-amplifier.287023/#post-5108799

[3] Bob Cordell, “Complementary JFET Offset Mismatch”, https://www.cordellaudio.com/poweramp/Complementary_JFET_Matching.pdf

[4] Transistorlegacy, (2021, December 28), “Revisiting lateral MOSFET stability”, DIYAudio.com, https://www.diyaudio.com/community/threads/revisiting-lateral-mosfet-stability.381147/

[5] Heatsink Calculator, https://heatscapecal.com/natural

[6] Nelson Pass, (2002, December 5), “Proper mounting of TO-247 Devices”, DIYAudio,com, https://www.diyaudio.com/community/threads/proper-mounting-of-to-247-devices.8319/#post-91527